KESRX01

290 - 460MHz ASK Receiver

Advance Information

DS3968 5.0 March1998

The KESRX01 is a single chip ASK (Amplitude Shift Key) Receiver IC. It is designed to operate in a variety of low power radio applications including keyless entry, general domestic and industrial remote control, RF tagging and local paging systems.

This single conversion super–heterodyne receiver offers an exceptionally high level of integration and performance. The unique architecture enables data rates up to 50Kbits/sec to be supported. All low power radio regulations, including ETSI–ETS 300 220, and FCC, part 15, can easily be met. Local oscillator generation is performed by an on–chip PLL which uses an external crystal reference oscillator (4.5 to 7.2MHz). All popular radio frequencies (315MHz, 433.92MHz, etc) can then be supported by simply choosing the appropriate crystal frequency.

Particular emphasis has been placed on low current consumption, with pulsed ON/OFF operation allowing <1mA average current consumption to be achieved. The on–chip VCO and IF significantly minimise the external components needed thus reducing any re–radiation effects.

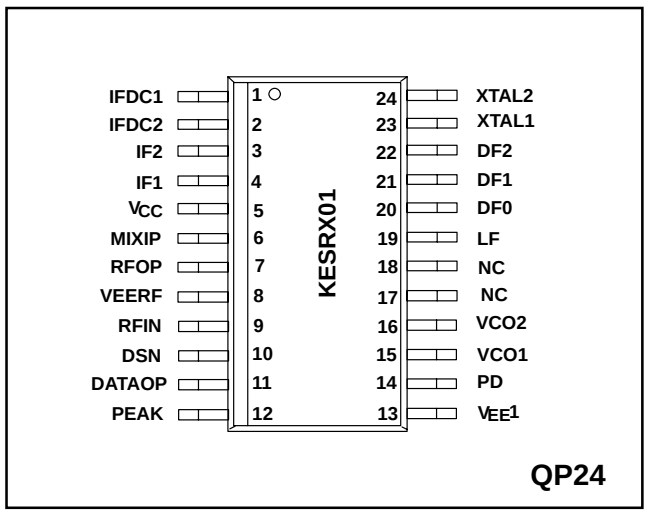


Fig. 1 Pin connections - top view

FEATURES

- Very low supply current (2.30mA typical)
- Low external part count
- –105dBm sensitivity (typical 315MHz)
- Integrated VCO and IF Filters.

ORDERING INFORMATION

KESRX01/IG/QP1T (Tape and Reel)
KESRX01/IG/QP1S (Tubes)

ABSOLUTE MAXIMUM RATINGS

All voltages relative to V_{EE} (0V)

Junction temperature, Tj	–55 to +150°C
Storage temperature, Tstg	–55 to +150°C
Supply voltage, V_{CC} max	V_{CC} –0.5 to +8.0 V
Voltage on any pin, Vshort	–0.5 to +8.0V

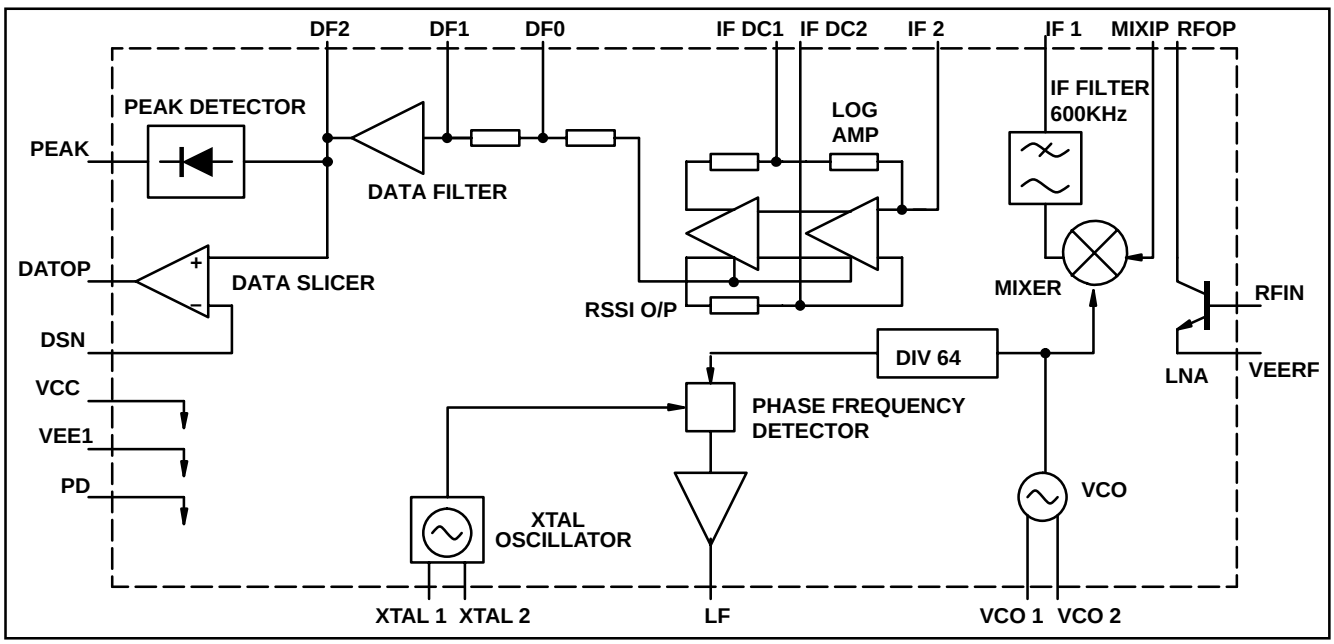


Fig. 2. Block diagram

ELECTRICAL CHARACTERISTICS D.C.

T_{amb} = -40 to + 85°C, V_{CC} = 4.75V to 7.0V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Supply current	I_{CC1}		2.30	3.00	mA	Vcc = 5V, all
Supply current (PLL powered down)	I_{CC2}		1.90	2.60	mA	V_{CC} = 5V, all
Power down pin input logic high	V_{ih}	V_{CC}-0.5		V_{CC}+0.5	V	
Power down pin input logic low	Vil	V_{EE}-0.5		V_{EE}+0.5	V	
Peak detector source current	I_{pk}		500		µA	
Peak detector leakage	I_{IK}			250	nA	
Data output Logic High	V_{oh}	0.7V_{CC}			V	Iload = 10µA
Data output Logic Low	V_{ol}			0.3V_{CC}	V	Iload = 10µA

Electrostatic discharge (ESD) protection (human body model) 2KV minimum, all pins.
NOTES: Care must be taken not to power up the device with pins 7 and 8 shorted by a solder bridge, as operation with pin 7 grounded can damage the device and result in low sensitivity.

ELECTRICAL CHARACTERISTICS A.C.

T_{amb} = -40 to + 85°C, V_{CC} = 4.75V to 7.0V. These characteristics are guaranteed by either production test or design. they apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Sensitivity See Note 1			-103	-100	dBm	R_S = 50Ω, 434MHz, 2KB/s
Signal handling See Note 2		-23.5			dBm	R_S = 50Ω, 434MHz, 2KB/s
LNA input impedance Parallel combination R_{11}/C_{11}		2.65//2.2		3.61//2.2	KΩ//pF	V_{CC} = 5V; 25°C ambient; 434MHz Also see note 5
Mixer input impedance Parallel combination R_{11}/C_{11}		1.15//1.1		1.21//1.62	KΩ//pF	V_{CC} = 5V; 25°C ambient; 434MHz Also see note 5
Crystal oscillator input impedance		-0.77	-1.8	-2.1	KΩ	C5 = C4 = 18pF
Integrated IF filter -3dB low pass cut off frequency	IF_{3dB}	450	550	750	KHz	All
Spurious reverse isolation to RFIN See Note 3			100		µV (rms)	R_S = 500Ω
Adjacent channel rejection See Note 4	ACR		65		dB	10MHz offset from receiver VCO

Notes:

1. Sensitivity is defined as the minimum average signal level measured at the input necessary to achieve a bit error ratio of 10^{-2} where the input signal is a return to zero pulse (RZ) with an average duty cycle of 50%. The RF input is assumed to be matched into 50Ω.
   Measured in test circuit Fig. 6 with data filter bandwidth of 5KHz as shown and for a 2Kbit/s, 50% duty cycle signal.
2. Signal handling is defined as the maximum input signal capable of being succcessfully de-modulated. It is assumed the input is ASK modulated with an extinction ratio of a least 40dB. The combination of this specification together with the sensitivity specification gives a minimum signal handling range of 76dB. The RF input is assumed to be matched into 50Ω.
   Measured in test circuit Fig. 6. with data filter bandwidth of 5KHz as shown.
3. -67dBm in 50Ω measured with the RF input matching network.
4. Adjacent channel rejection is defined for an interfering tone (ACR) dB above threshold and 10MHz offset from the carrier giving a 3dB reduction in sensitivity i.e. the interfering tone is 4.74mV (rms) @ Fc ± 10MHz and to achieve the specified sensitivity the wanted signal will have to be increased to 2.2µV (rms)
5. Please refer to Smith charts Fig.8 through to 10 covering frequency range 250-500MHz.

PIN LISTING

Pin	Symbol	Description
1	IFDC1	IF amplifier – decouple point
2	IFDC2	IF amplifer – decouple point
3	IF1	Mixer output
4	IF2	IF amplifer input
5	VCC	Positive power supply
6	MIXIP	RF mixer input (tank)
7	RFOP	RF amplifier output (tank)
8	VEERF	RF amplifier ground
9	RFIN	RF input (antenna)
10	DSN	Bit slicer comparator negative input
11	DATAOP	Bit slicer comparator output
12	PEAK	Peak detector output

Pin	Symbol	Description
13	VEE	Negative power supply (0V)
14	PD	PLL power down
15	VCO1	VCO maintaining amplifer
16	VCO2	VCO maintaining amplifier
17	NC	Not connected, unless to GND
18	NC	Not connected,unless to GND
19	LF	PLL loop filter O/P output
20	DF0	Data filter – external connection
21	DF1	Data filter – external connection
22	DF2	Data filter – external connection
23	XTAL1	Crystal oscillator
24	XTAL2	Crystal oscillator

FUNCTION

Phase locked loop

The phase locked loop generates the local oscillator by frequency multiplication of a crystal referenced oscillator.

Dividers

A divide by 64 prescaler is present in the PLL feedback loop. The local oscillator frequency is then $Fo=64xF_{ref}$. A system operating at 433.92MHz (RFIN) with a 270KHz IF frequency would require a reference of 6.77578MHz (assuming mixer low side injection). Alternative choice of crystal and tank components permit operation at specific frequencies in the range 290 – 460MHz.

Phase detector

The phase detector used is a phase frequency detector (PFD) with a current (charge pump) output.

This phase detector has a triangle characteristic for an input phase error in the range $-2\pi < \theta < +2\pi$ and has the benefit of being a true frequency detector (as well as a phase detector) and hence will always achieve lock for any initial VCO frequency.

The charge pump provides an output current in the range $\pm 30\mu A$ and hence gives a phase detector gain of $4.8\mu A/rad$.

The PLL loop characteristics such as lock-up time, capture range, loop bandwidth and VCO reference sideband suppression are controlled by the external loop filter.

For the intended application a 2nd order loop should be sufficient as shown in the test circuit Fig. 6.

VCO

A balanced configuration is used with the LC tank connected externally across VCO1 and VCO2 Fig. 3.

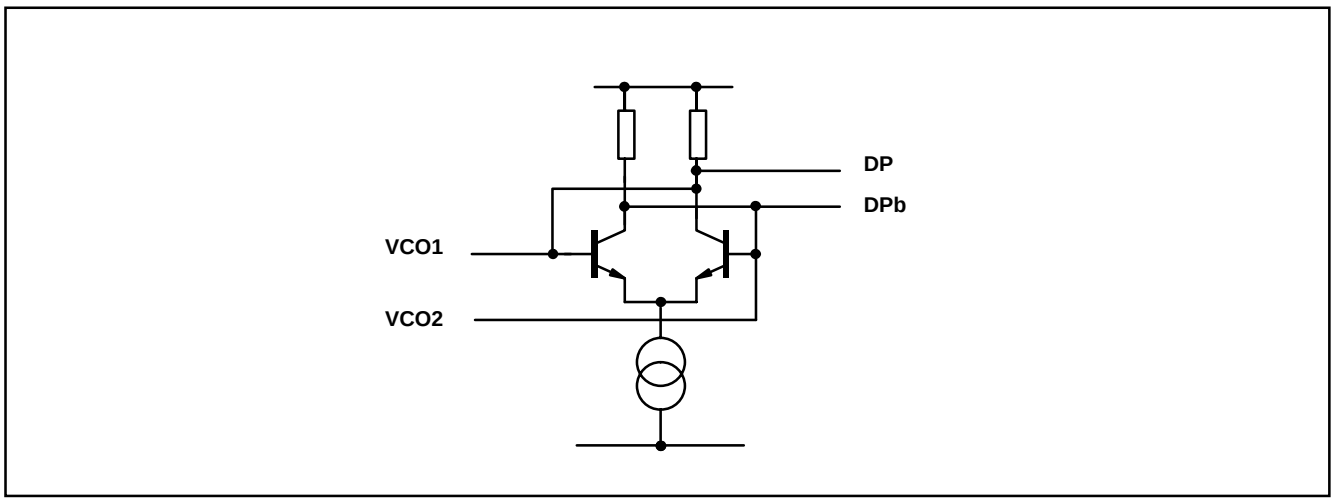


Fig. 3 Input circuit of VCO and divider chain

External SAW resonator

For reduced power the PLL based oscillator can be replaced by a SAW based oscillator. If pin PD is tied low (VEE) the crystal oscillator, dividers and phase detector/charge pump are powered down. The VCO can then be used as a maintaining amplifier for an external SAW based oscillator. The normal mode of operation is with PD set high (VCC) or alternatively left unconnected. Note: the power down facility is intended to be hard wired (either to VCC or VEE) and hence the PD pin is not specified for operation with normal CMOS or TTL logic levels.

PD	MODE
V_{CC} /NC	PLL Enable
V_{EE}	PLL Disable

Reference crystal oscillator

A crystal stabilised oscillator provides a reference clock for the PLL. The oscillator is configured for parallel resonant operation in the fundamental mode (typical operating frequency of 4–7MHz). The crystal is connected between pins XTAL1, XTAL2 with external components as shown in Fig. 6. Note that this is a single transistor Colpitts oscillator where the external load capacitors must be taken into account in specifying the crystal. See Application Note AN207.

RF amplifier

The RF amplifier consists of a low noise transistor in a common emitter configuration. A separate emitter connection is provided (VEERF) to reduce sensitivity to any common impedance in this path. The amplifier is current source biased so the signal (RFIN) should be a.c. coupled. The collector is open circuit so that the gain can be set with an external tuned load, Fig. 6. Its input impedance is given in Fig. 9 and output impedance in Fig. 10.

Down converting mixer

The RF input is a.c. coupled into a doubly balanced mixer configuration. Its input impedance is given in Fig.8.

IF filtering

The IF filter has a (nominal) bandpass response from 25KHz to 550KHz. The single high pass section is provided by the combination of the external a.c. coupling capacitor between IF1 and IF2 and an on chip resistor (nominal value 12kΩ). The low pass section is entirely on chip and to meet the selectivity requirements (adjacent channel rejection) this filter has 4 low pass poles with a Butterworth response.

IF amplifiers and demodulator

The majority of the receiver gain is provided in the form of an IF limiting strip. These amplifiers are all d.c. coupled and hence differential d.c. feedback is required. This is decoupled externally at pins IFDC1 and IFDC2. The IF amplifier stages also combine to provide a Received Signal Strength Indicator (RSSI) function. Since the modulation is ASK and the RSSI output has
a linear output for a logarithmic change on its input then the RSSI output is the demodulated data. The only uncertainty is the d.c. level.

Data filter

Prior to the data slicer the demodulated data passes through a low pass filter. This filter is a 2nd order Sallen–Key section using an on chip voltage follower. External capacitors set the cutoff frequency and filter Q. The value of the on chipresistors is 100KΩ (nominal). See Fig. 4.

The cut-off frequency of the data filter, f_o, should be set to reduce high frequency noise into the data slicer without distorting the wanted signal. Normally this would be at least three times the data frequency.

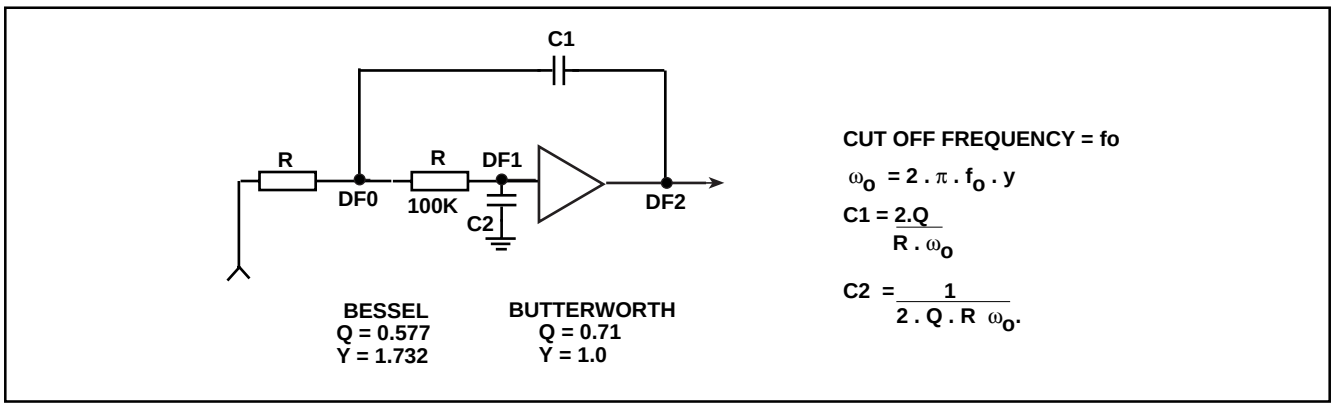


Fig. 4 Choosing data filter components

Example
To implement a Bessel response filter with a 10KHz 3dB cutoff
C1 = 106pF C2 = 80pF

Bit slicer and Peak Detector

To provide maximum flexibility an independent data comparator is provided. External circuitry must be provided to obtain the bit slicer threshold level. Two basic approaches are supported.

1. For coding schemes with no d.c. content (e.g. Manchester coding or 33% / 66% pulse width encoding) this can be based on the integrated d.c. level (using a series R and C). See Application Note AN207.

2. For coding schemes with d.c. content (e.g. low duty cycle pulse width modulation) an active peak detector is included. The output at pin PEAK represents the peak level at the data filter output (as shown in Fig.5). An external RC time constant at this pin determines the maximum attack and decay times of the peak detector. Typical values for the leakage and diode current source capability are shown in the specifications. The comparator has relatively low drive capability (push/pull current source output of 20μA) and hence DATOP should not be excessively loaded. On chip positive feedback around the comparator provides a nominal hysteresis level of 20mV.

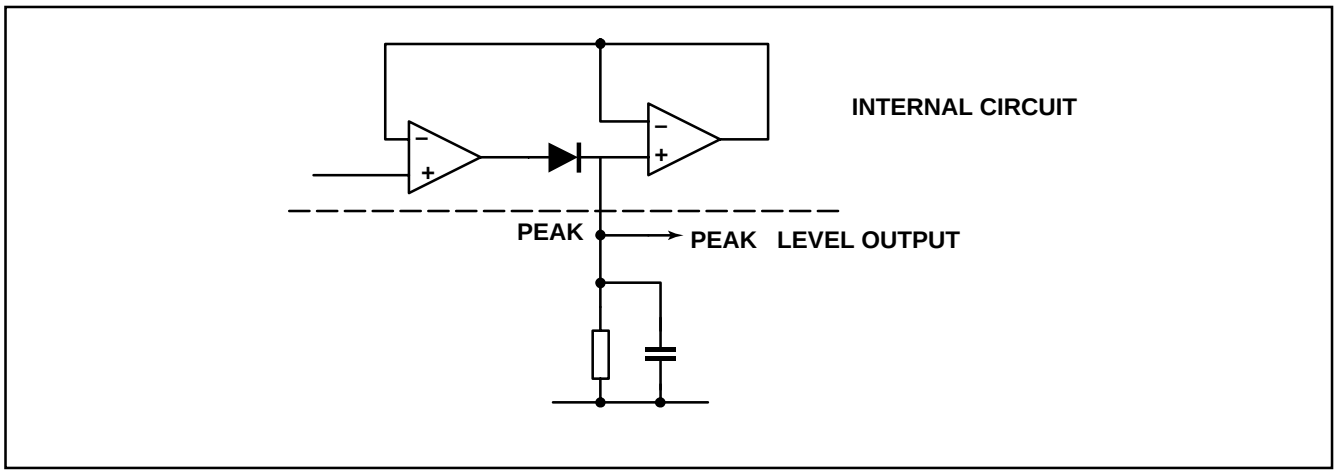


Fig. 5 Peak detector output

Sensitivity

In digital radio systems, sensitivity is often defined as the lowest signal level at the receiver input that will achieve a specified Bit Error Ratio (BER) at the output. The sensitivity of the KESRX01 receiver, when used in the 434MHz application shown in Fig. 6, is typically –103dBm average power (ASK modulated with 2kHz, 50% duty cycle square wave) to achieve a 0.01 BER. The input was matched for a 50Ω signal source. At 315MHz, –105dBm average power is typically achievable. Consult the Applications Notes refered to at the end of this Datasheet for detailed PCB design issues to secure perfomance.

Choice of IF frequency and IF bandwidth

The IF frequency is selected to be nominally 270KHz with the low frequency cut-off at 25KHz and the high frequency cut-off at 550KHz (nominal). For worst case tolerances the transmitter frequency may be 433.92MHz ± 100KHz. i.e from 433.82MHz to 434.02MHz (see transmitter design specification application notes)

The local oscillator frequency is set at 433.65MHz with a required accuracy of at least ± 100kHz (see section below) i.e 433.55MHz to 433.75MHz.

This guarantees that the IF (70KHz to 470KHz) falls within the acceptance bandwidth of the IF filter.

The frequency of operation for such products in Europe is 433.05MHz to 434.79MHz. The choice of such a low IF frequency ensures that any image falls within the regulatory band. This in turn ensures that the receiver cannot be blocked by the image response of an unwanted signal outside of this band.

Frequency Accuracy

The stability of the local oscillator is equal to that of the crystal reference oscillator. Therefore to obtain a final output accuracy of ± 100KHz at 433MHz would require a crystal with a tolerance specification of ± 230ppm. This tolerance should encompass all causes e.g. initial accuracy, temperature stability and ageing. Choose a tighter tolerance crystal for increased frequency accuracy.

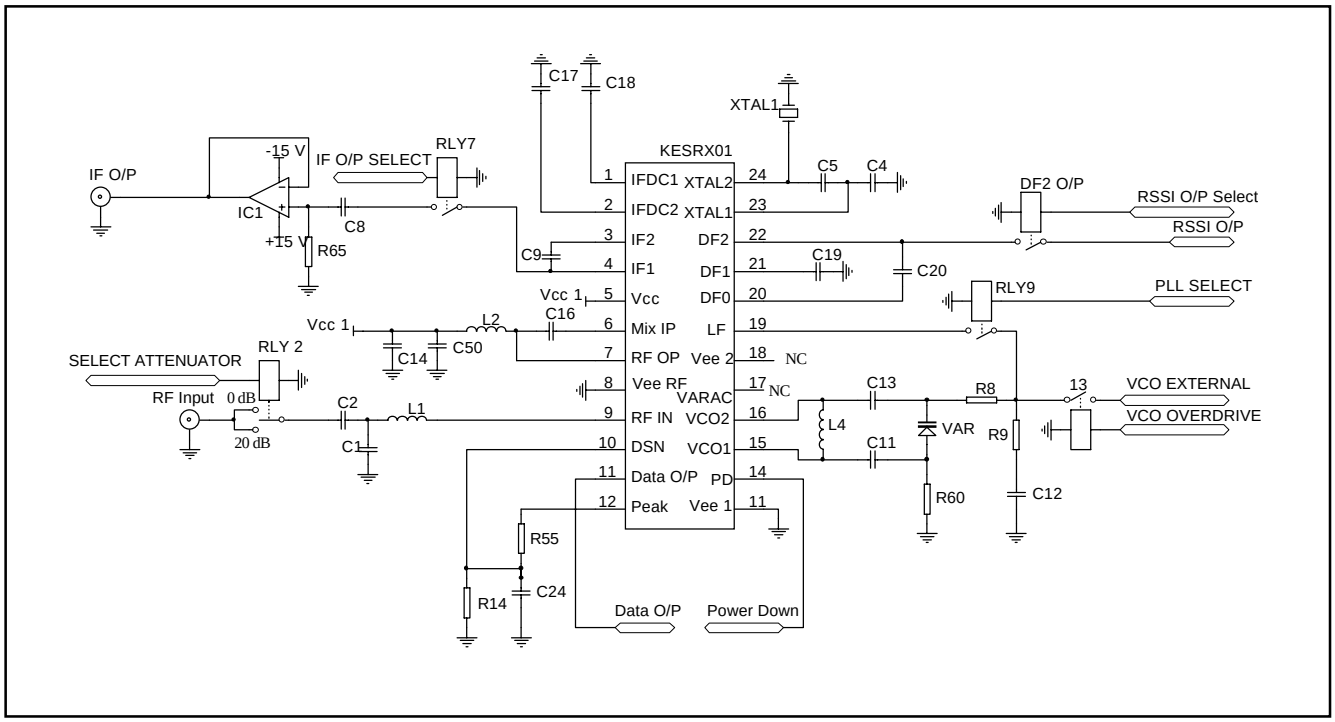


Fig. 6 KESRX01 Test circuit at 434MHz (peak detector slice mode)

Component	Function	Value	Units
C1	Input Matching circuit	4.7	pF
C2	Input Matching circuit	1	pF
C4, C5	XTAL feedback capacitors	100	pF
C8	DC decoupling capacitor	470	pF
C9	IF filter high pass	220	pF
C11, C13	VCO decouple	33	pF
C12	PLL loop filter	560	pF
C14	V_{CC} decoupling capacitor	1	µF
C16	RF amplifier load	56	pF
C17, C18	IF amplifier decouple	100	nF
C19	Data filter	150	pF
C20	Data filter	220	pF
C24	Data slicer time constant	1	µF
C50	V_{CC} decoupling capacitor	100	pF
R8	Varactor bias	47	KΩ
R9	PLL loop filter	18	KΩ
R14	Data slicer threshold circuit	1	MΩ
R55	Data slicer threshold circuit	4.3	KΩ
R60	Varactor bias	47	KΩ
R65	IC1 bias	1	MΩ
L1	RF amplifier input matching	47	nH
L2	RF amplifier/Mixer matching network	27	nH
L4	VCOtank circuit	39	nH
VAR	VCO tank circuit varactor	SMV-1104-35	4 to 11pF
XTAL	Reference frequency	6.775	MHz

Table 1. Component values for test circuit

If required, the reference signal to the PLL can be driven externally from a stable signal source as shown in Fig. 7.

Typically a 200mVp clock signal is ac coupled to produce differential output on OP and OPb. (C=10nF, Rs (source) < 5kΩ)

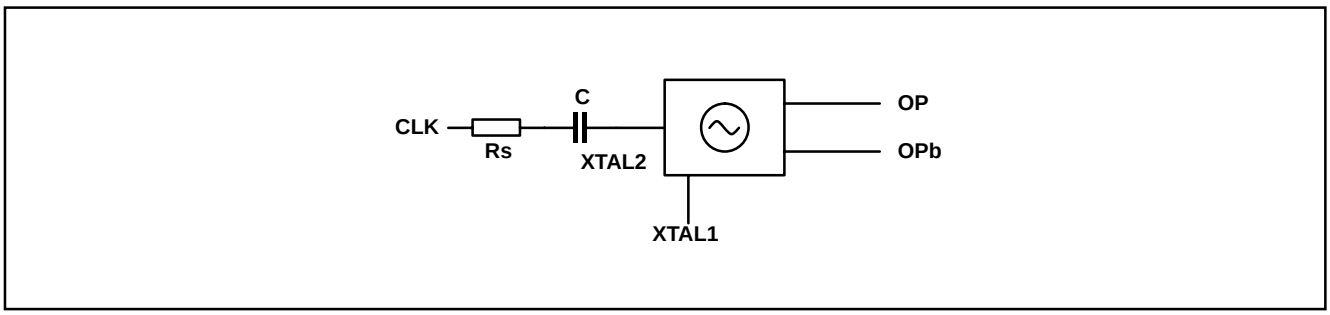


Fig. 7 Direct drive of crystal oscillator

Applications

For detailed applications support material consult the following Application Notes.

AN207	KESRX01 Demonstrator Receiver - A practical Application
AN4561	KESTX01/02 Demonstrator Transmitter

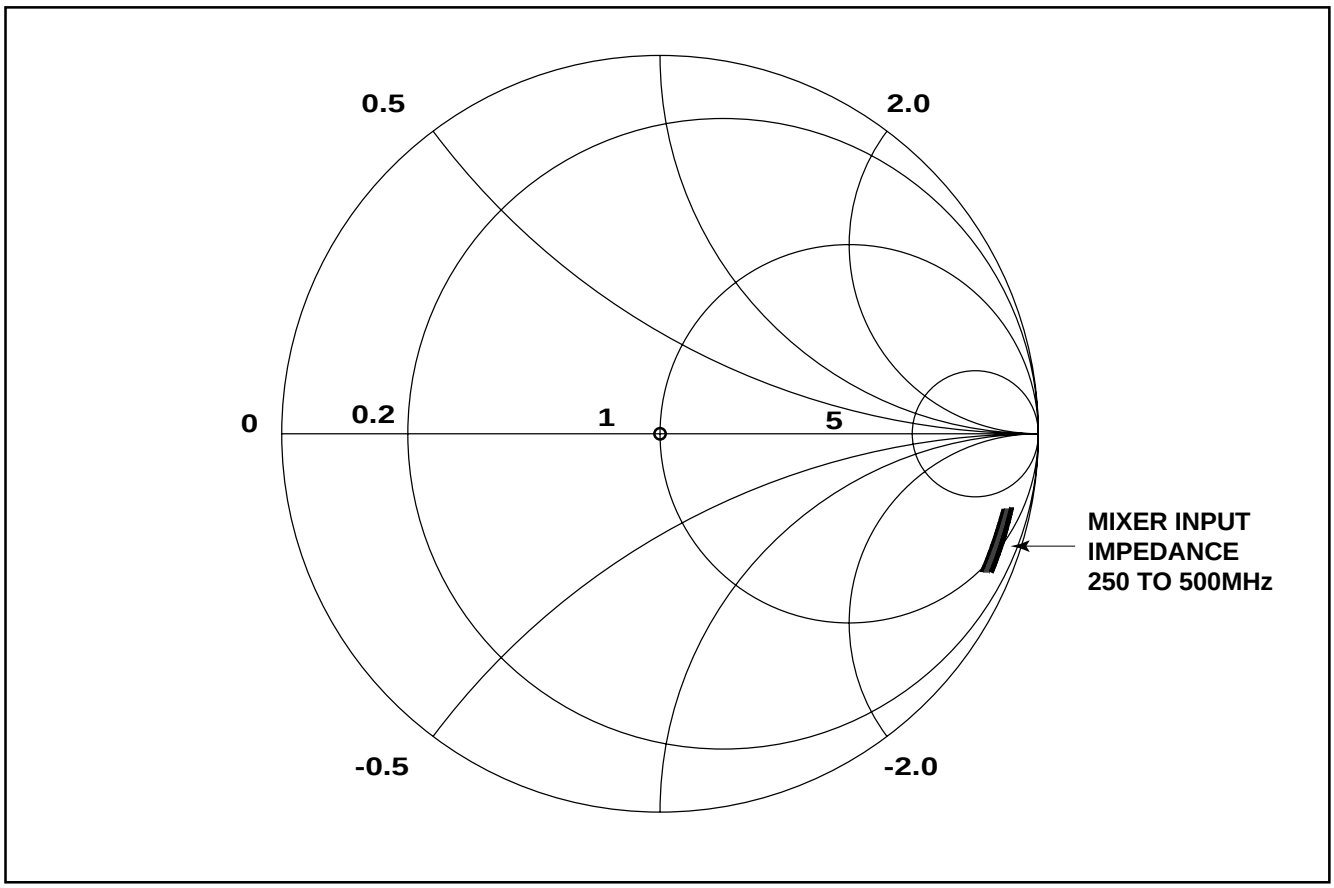


Fig. 8 KESRX01 mixer input impedance at -40, 27 and + 85 degrees

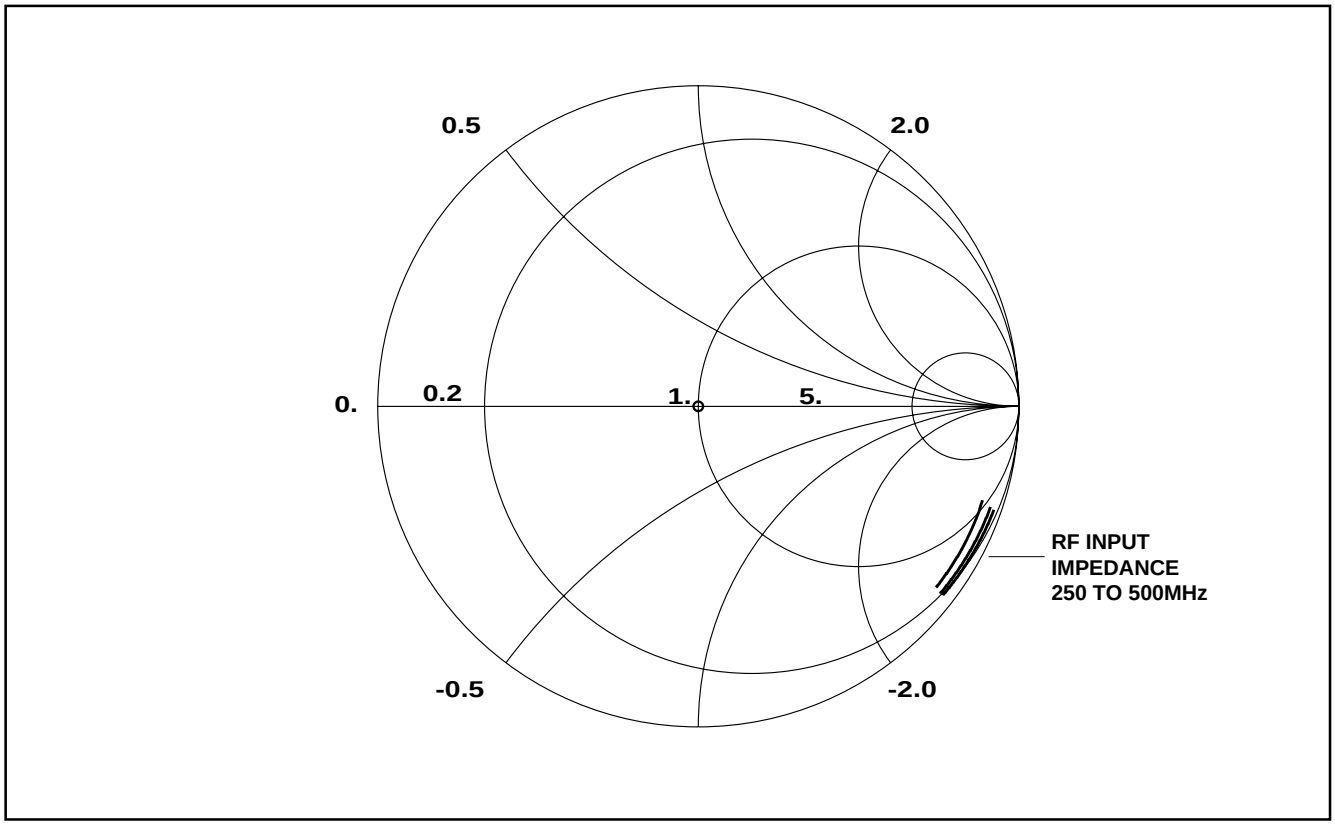


Fig. 9 KESRX01 LNA input impedance at -40, 27 and +85 degrees

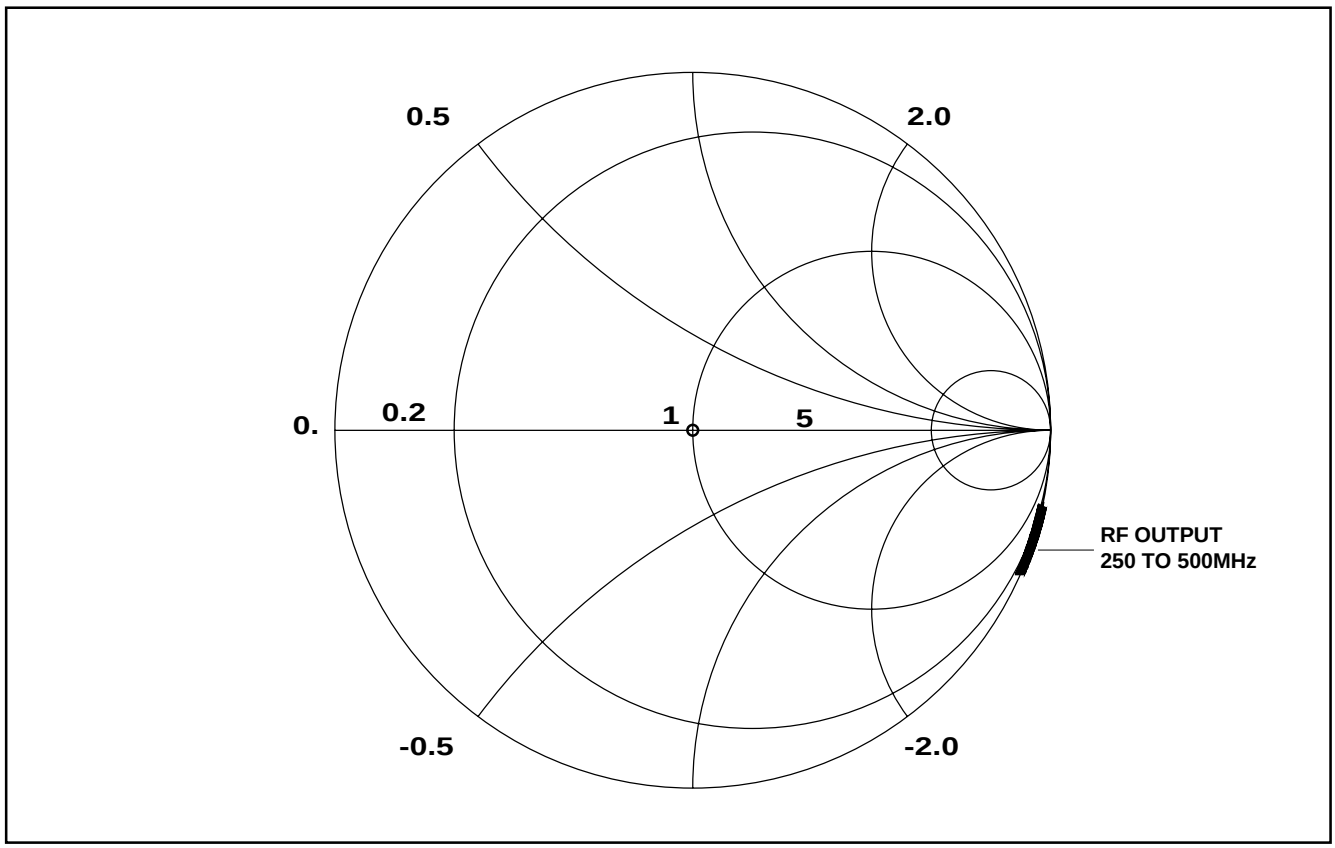
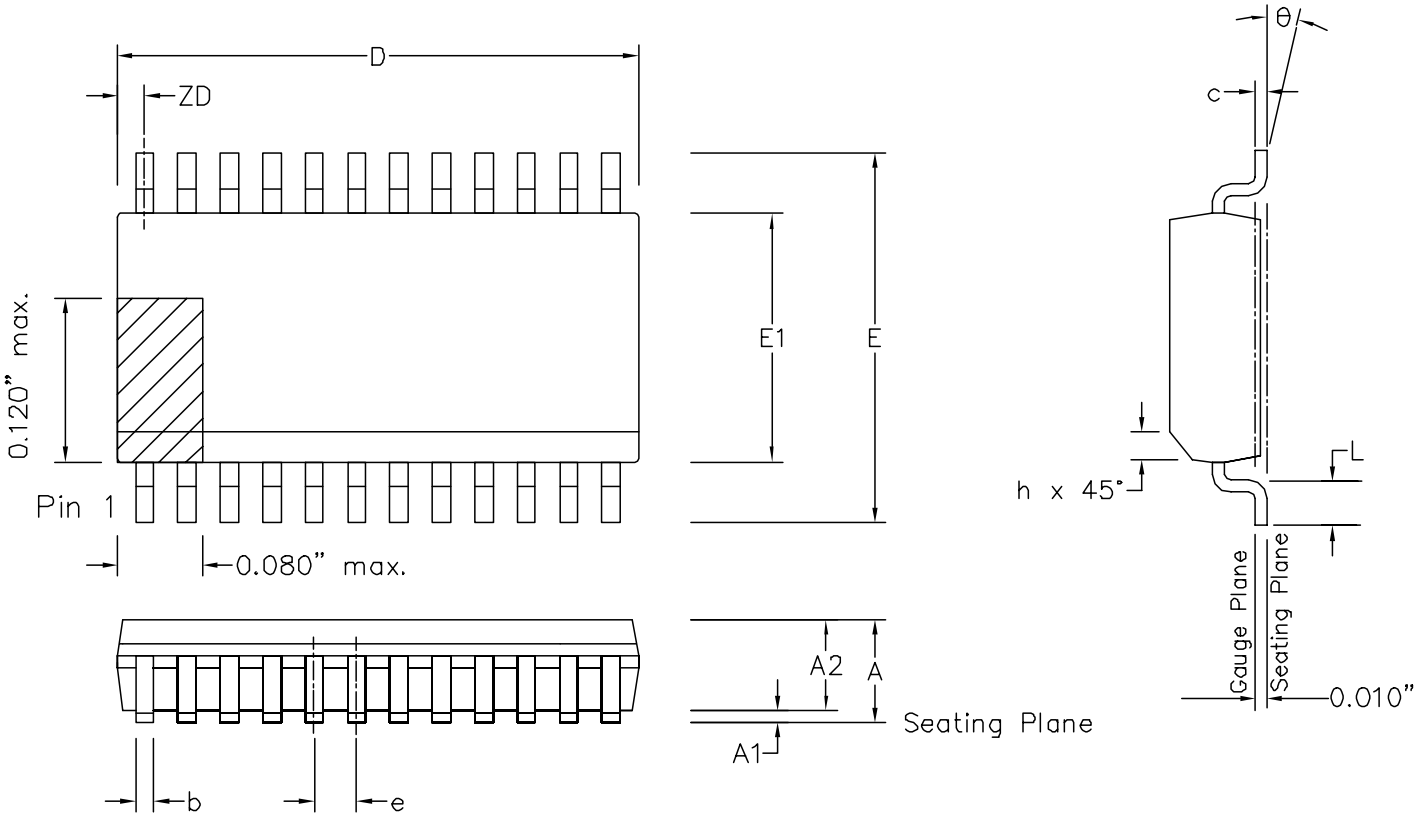


Fig. 10 KESSRX01 LNA output impedance at -40, 27 and +85 degrees

	RF INPUT IMPEDANCE					
	Min		Typ		Max	
Freq MHz	Mag	Phase	Mag	Phase	Mag	Phase
303	0.935	-22.49	0.963	-23.16	0.975	-23.35
315	0.935	-23.43	0.962	-24.09	0.999	-24.26
403	0.935	-30.17	0.959	-30.74	0.999	-30.80
418	0.934	-31.29	0.958	-31.85	0.969	-31.89
434	0.934	-32.47	0.957	-33.02	0.968	-33.04

	RF OUTPUT IMPEDANCE					
	Min		Typ		Max	
Freq MHz	Mag	Phase	Mag	Phase	Mag	Phase
303	0.999	-14.62	0.999	-14.32	0.999	-13.92
315	0.999	-15.2	0.999	-14.88	0.999	-14.47
403	0.999	-19.37	0.999	-18.97	0.999	-19.36
418	0.999	-20.08	0.999	-19.67	0.999	-19.37
434	0.999	-20.83	0.999	-20.40	0.999	-19.84

	MIXER INPUT IMPEDANCE					
	Min		Typ		Max	
Freq MHz	Mag	Phase	Mag	Phase	Mag	Phase
303	0.927	-14.64	0.938	-14.42	0.949	-14.11
315	0.926	-15.16	0.935	-14.95	0.949	-14.63
403	0.925	-19.03	0.937	-18.82	0.948	-18.49
418	0.925	-19.98	0.937	-19.47	0.948	-19.11
434	0.925	-20.39	0.937	-20.17	0.948	-19.84



Symbol	Control Dimensions in inches		Altern Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	—	0.059	—	1.50
D	0.337	0.344	8.56	8.74
ZD	0.033 REF.		0.84 REF.	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27
e	0.025 BSC.		0.64 BSC.	
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50
	Pin features			
N	24			
Conforms to JEDEC MO-137AE Iss. A				

This drawing supersedes
418/ED/51617/003 (Swindon/Roborough)
TD/D 1030 (Oldham)

Notes:

1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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Drawing Number
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