AT91SAM7A3-EK Evaluation Board

User Guide

Table of Contents

Section 1

Overview 1-1

1.1 Scope 1-1
1.2 Deliverables 1-1
1.3 The AT91SAM7A3-EK Evaluation Board 1-1

Section 2

Setting Up the AT91SAM7A3-EK Evaluation Board 2-1

2.1 Electrostatic Warning 2-1
2.2 Requirements 2-1
2.3 Layout 2-2
2.4 Powering Up the Board 2-3
2.5 Backup Power Supply 2-3
2.6 Getting Started 2-3
2.7 AT91SAM7A3-EK Block Diagram 2-4

Section 3

Board Description 3-1

3.1 AT91SAM7A3 Microcontroller 3-1
3.2 AT91SAM7A3 Block Diagram 3-4
3.3 Memory 3-5
3.4 Clock Circuitry 3-5
3.5 Reset Circuitry 3-5
3.6 Shutdown Controller 3-5
3.7 Power Supply Circuitry 3-5
3.8 Remote Communication 3-5
3.9 Analog Interface 3-5
3.10 User Interface 3-5
3.11 Debug Interface 3-6
3.12 Expansion Slot 3-6

Section 4

Configuration Straps 4-1

4.1 Configuration Straps 4-1

Section 5

Schematics 5-1

5.1 Schematics 5-1

Section 6

Revision History 6-1

6.1 Revision History 6-1

Section 1
Overview

1.1 Scope

The AT91SAM7A3-EK evaluation kit enables evaluation capabilities and code development of applications running on an AT91SAM7A3.

This guide focuses on the AT91SAM7A3-EK board as an evaluation platform.

1.2 Deliverables

The AT91SAM7A3-EK package contains the following items:

- an AT91SAM7A3-EK board
- one A/B-type USB cable
- one serial RS232 cable
- one DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 The AT91SAM7A3-EK Evaluation Board

The board is equipped with an AT91SAM7A3 (100-pin LQFP Green package) together with the following:

- USB device port interface
- one DBGU serial communication port
- JTAG/ICE debug interface connector
- two serial CAN communication ports
- one serial LIN communication port
- one buffered analog input and PWM output
- one Power LED and four general-purpose LEDs
- one SD/MMC/DataFlash® card slot
- expansion connector
- one Atmel® serial DataFlash
- one footprint for 3.6V lithium thionyl-chloride backup battery

Section 2

Setting Up the AT91SAM7A3-EK Evaluation Board

2.1 Electrostatic Warning

The AT91SAM7A3-EK evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM7A3-EK evaluation board, the following items are required:

- the AT91SAM7A3-EK evaluation board itself
- an A/B-type USB cable

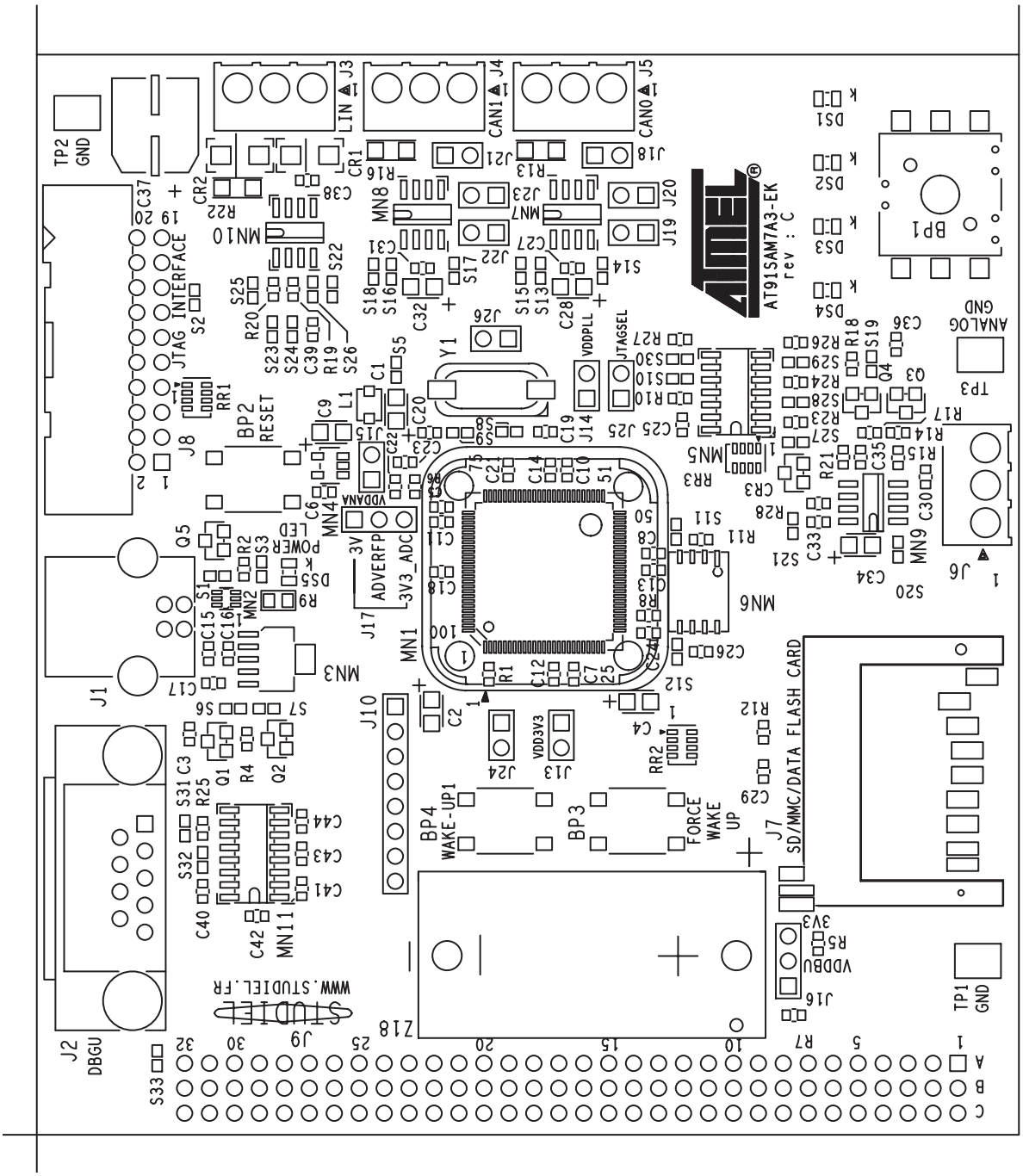
or

- a DC USB power adapter (5V at 0.5 A) with USB A/B cable

Note: The AT91SAM7A3-EK is not delivered with a JTAG/ICE interface which is required to start evaluating the device.

2.3 Layout

Figure 2-1. Top Level Layout



2.4 Powering Up the Board

AT91SAM7A3 is self-powered by the USB port or by a USB power adapter.

2.5 Backup Power Supply

The user may add a battery (SAFT LS14250 3.6V or equivalent) in order to permanently power the backup part of the device. In this case, the configuration of J16, S6 and S7 must be changed.

Refer to Table 4-1.

2.6 Getting Started

The AT91SAM7A3-EK evaluation board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this DVD-ROM, or to the Atmel web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM7A3-EK.

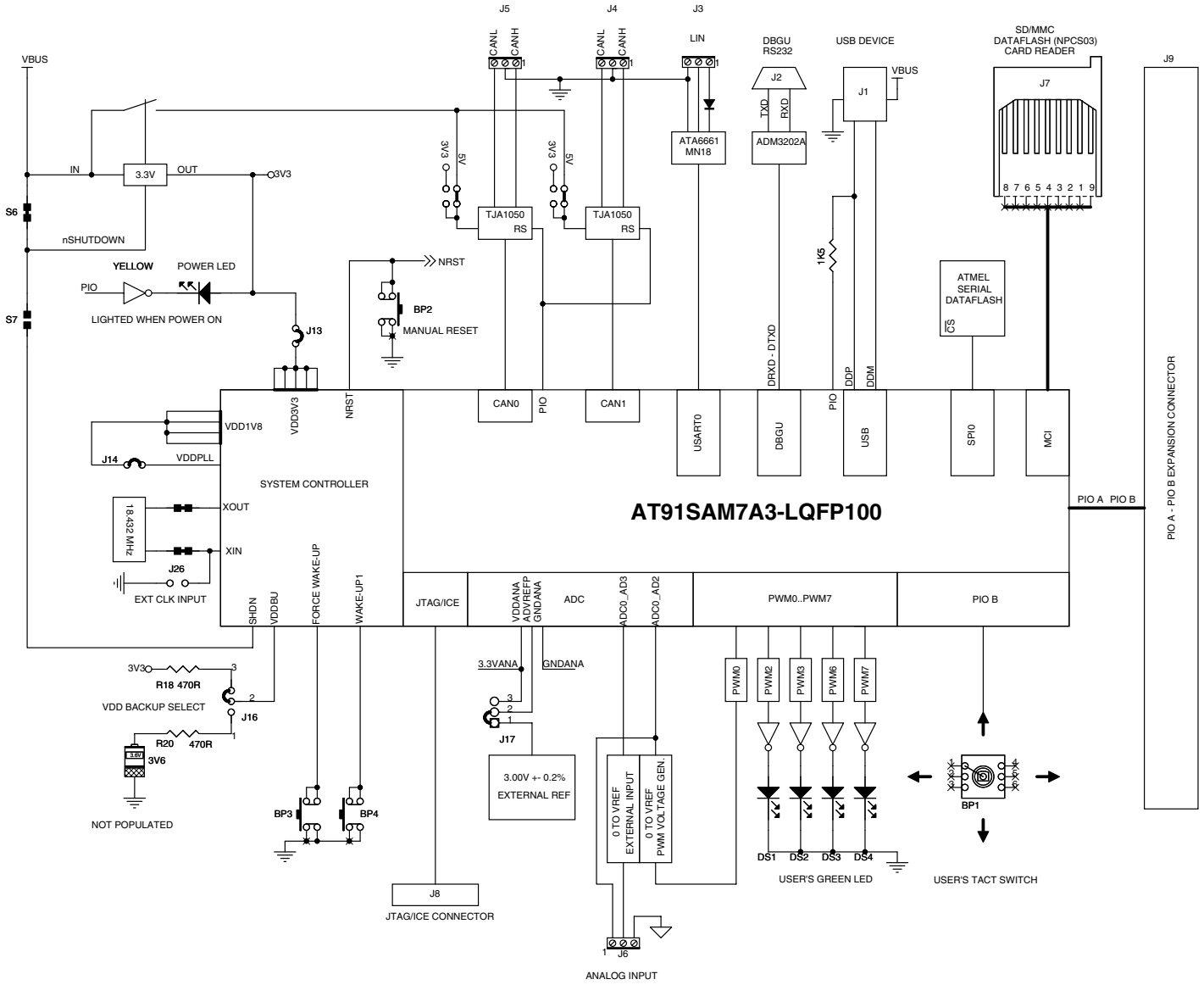
Note that the AT91SAM7A3 microcontroller fitted on the evaluation board has been programmed with the SAM Boot Assistant (SAM-BA™) which provides an easy way to program the embedded Flash memory through the USB or DBGU communication channel.

Programming through DBGU requires that the evaluation kit is powered using a Power Supply USB Adapter

Note: The SAM-BA Boot Assistant resides in the embedded Flash memory and will be deleted when programming the Flash. A JTAG/ICE interface is required to recover SAM-BA Boot Assistant.

2.7 AT91SAM7A3-EK Block Diagram

Figure 2-2. Block Diagram



Section 3

Board Description

3.1 AT91SAM7A3 Microcontroller

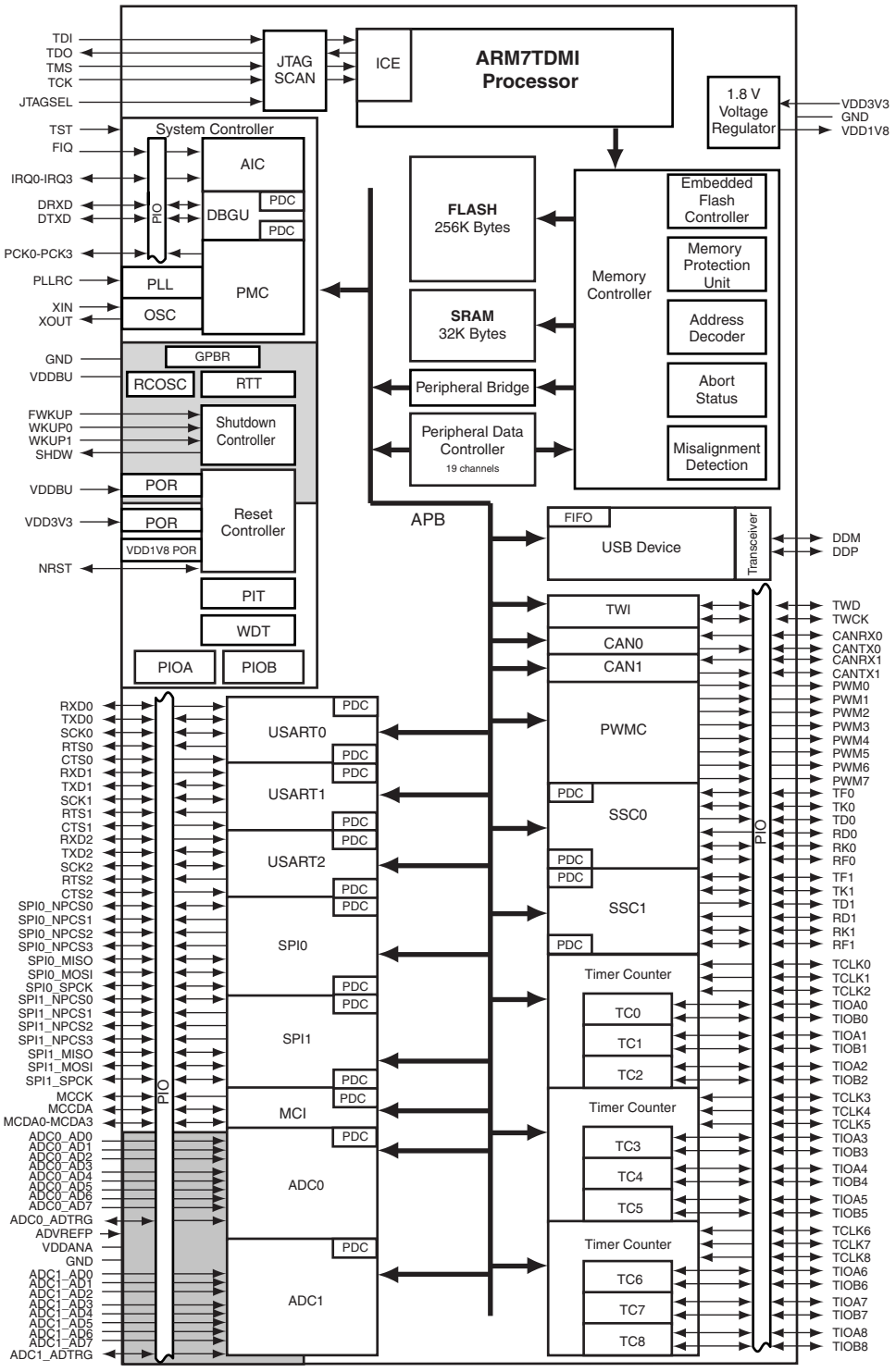
- Incorporates the ARM7TDMI ® ARM® Thumb® Processor
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
- Embedded ICE In-circuit Emulation, Debug Communication Channel Support
- 256 Kbytes of Internal High-speed Flash, Organized in 1024 Pages of 256 Bytes
  - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
  - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
  - Page Programming Time: 6 ms, Including Page Auto-erase, Full Erase Time: 15 ms
  - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities
- 32K Bytes of Internal High-speed SRAM, Single-cycle Access at Maximum Speed
- Memory Controller (MC)
  - Embedded Flash Controller, Abort Status and Misalignment Detection
  - Memory Protection Unit
- Reset Controller (RSTC)
  - Based on Three Power-on Reset Cells
  - Provides External Reset Signal Shaping and Reset Sources Status
- Clock Generator (CKGR)
  - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and One PLL
- Power Management Controller (PMC)
  - Power Optimization Capabilities, including Slow Clock Mode (Down to 500 Hz), Idle Mode, Standby Mode and Backup Mode
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources

  - Four External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel interrupt
- Periodic Interval Timer (PIT)
  - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
  - 12-bit key-protected Programmable Counter
  - Provides Reset or Interrupt Signal to the System
  - Counter May Be Stopped While the Processor is in Debug Mode or in Idle State
- Real-time Timer (RTT)
  - 32-bit Free-running Counter with Alarm
  - Runs Off the Internal RC Oscillator
- Two Parallel Input/Output Controllers (PIO)
  - Sixty-two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin and Wake-up Circuitry
- Two 32-bit Battery Backup Registers for a Total of 8 Bytes
- One 8-channel 20-bit PWM Controller (PMWC)
- One USB 2.0 Full Speed (12 Mbits per Second) Device Port
  - On-chip Transceiver, 2-Kbyte Configurable Integrated FIFOs
- Nineteen Peripheral Data Controller (PDC) Channels
- Two CAN 2.0B Active Controllers, Supporting 11-bit Standard and 29-bit Extended Identifiers
  - 16 Fully Programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- Two 8-channel 10-bit Analog-to-Digital Converter
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- Three 3-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability

- Two Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- One Two-wire Interface (TWI)
  - Master Mode Support Only, All Two-wire Atmel EEPROMs Supported
- Multimedia Card Interface (MCI)
  - Compliant with Multimedia Cards and SD Cards
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC, MMC and SDCard Compliant
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 130 mA for the Core and the External Components, Enables 3.3V Single Supply Mode
  - 3.3V VDD3V3 Regulator, I/O Lines and Flash Power Supply
  - 1.8V VDD1V8 Output of the Voltage Regulator and Core Power Supply
  - 3V to 3.6V VDDANA ADC Power Supply
  - 3V to 3.6V VDDBU Backup Power Supply
- 5V-tolerant I/Os
- Fully Static Operation: 0 Hz to 60 MHz at 1.65V and 85°C Worst Case Conditions
- Available in a 100-lead LQFP Green Package

3.2 AT91SAM7A3 Block Diagram

Figure 3-1. Block Diagram



3.3 Memory

- 256 Kbytes of Internal High-speed Flash
- 32 Kbytes of Internal High-speed SRAM
- Atmel serial DataFlash

3.4 Clock Circuitry

- 18.432 MHz standard crystal for the embedded oscillator
- 32 KHz internal RC oscillator

3.5 Reset Circuitry

- Internal reset controller with a bi-directional reset pin
- External reset pushbutton

3.6 Shutdown Controller

- Programmable shutdown and Wake-Up
- Force Wake-Up and Wake-up pushbutton

3.7 Power Supply Circuitry

- USB powered, the dynamic power consumption on VDD1V8 is less than 50 mA at full speed when running out of the Flash. The total current at power-up is less than 100 mA.
- External power can be applied via USB Power adapter 5V 0.5A with USB A/B cable
- On-chip embedded VDDCORE 1.8V regulator
- On-board 3.3V linear regulator with shutdown control

3.8 Remote Communication

- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket
- USB V2.0 Full-speed compliant, 12 Mbits per second (UDP)
- Two CAN 2.0B communication ports via the 3-position printed circuit terminal block
- One LIN communication port via the 3-position printed circuit terminal block

3.9 Analog Interface

- One selectable 0.2% 3.00V Vref or 3.3V ANA
- One 3-position printed circuit terminal block
- Two analog up to Vref inputs. One external user input and one back-looped with buffered PWM0 output.
- One buffered PWM0 analog output (up to Vref)

3.10 User Interface

- One 5-way joystick (4 directions and push for confirmation)
- Four general-purpose buffered green LEDs (PWM controlled)

- One yellow power LED (can also be software controlled)

3.11 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU serial RS232 COM Port

3.12 Expansion Slot

- One SD/MMC/DataFlash card slot
- All I/Os of the AT91SAM7A3 are routed to peripheral extension connectors (J9). This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

Section 4

Configuration Straps

4.1 Configuration Straps

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J13	Closed	VDD3V3 Jumper (1)
J14	Closed	VDDPLL Jumper (1)
J15	Closed	VDDANA Jumper (1)
J16	2-3	VDDBU Jumper select (1) 1-2 : Optional Lithium Thionyl Chloride 3.6V Backup Battery 2-3 : 3.3V power
J17	1-2	ADVREFP Jumper select(1) 1-2 : 3.00V Voltage reference 2-3 : VDDANA
J18	Closed	Enables 120 ohms CAN bus resistance termination (CAN0)
J19	Closed	Enables 5V power supply for TJA1050 Transceiver. It is closed by wire on solder side. J19 and J20 should not be closed at the same time.
J20	Open	Disables 3.3V power supply for TJA1050 Transceiver. J20 and J19 should not be closed at the same time.
J21	Closed	Enables 120 ohms CAN bus resistance termination (CAN1)
J22	Closed	Enables 5V power supply for TJA1050 Transceiver. It is closed by wire on solder side. J22 and J23 should not be closed at the same time.
J23	Opened	Disables 3.3V power supply for TJA1050 Transceiver. J23 and J22 should not be closed at the same time.
J24	Opened	Do not use: Factory test mode
J25	Opened	Select ICE mode or JTAG mode (Closed)
J26	Opened	External XIN clock input. S8 and S9 must be open.

Table 4-1. Configuration Jumpers and Straps (Continued)

Designation	Default Setting	Feature
S1	Opened	Solder it, enables permanent pull up on USB DP. S3 must be open.
S2	Closed	The System Reset signal (NRST) is connected to the ICE/JTAG socket (J8, pin 15).
S3	Closed	Enables the use of the USB DP PUP (PB1)
S4	Closed	Enables the use of the USB CNX detection (PB0)
S5	Closed	Digital Analog GND planes separation. Do not cut it
S6	Closed	Disables shutdown control and forces Power on. **Do not close at same time as S7.**
	Opened	Enables shutdown control
S7	Opened	Disables shut down control
	Closed	Enables shutdown control **Do not close at same time as S6.**
S8 - S9	Closed	Enables the use of 18.432 MHz crystal. Must be open if external clock used.
S10	Closed	Enables the Power LED control
S11	Closed	Enables the use of the NPCS13
S12	Opened	Disable Serial DataFlash write protect
S13	Closed	Enables the use of the TXD CAN0 transceiver (PA27)
S14	Closed	Enables the use of the RXD CAN0 transceiver (PA26)
S15	Closed	Enables control of the Standby/Normal mode for CAN0 and CAN1 transceivers (PA23)
S16	Closed	Enables the use of the TXD CAN1 transceiver (PA29)
S17	Closed	Enables the use of the RXD CAN1 transceiver (PA28)
S18	Opened	Enables control of the Standby/Normal mode for CAN0 and CAN1 transceivers (PA23). **If S18 is closed, S15 must be open.**
S19	Closed	Enables the use of PWM0 Analog Output (PA18)
S20	Closed	Enables the use of AD02 Analog Input (PB16)
S21	Closed	Enables the use of AD03 Analog Input (PB17)
S22	Closed	Enables the use of the TXD LIN transceiver (PA3)
S23	Closed	Enables the use of the RXD LIN transceiver (PA2)
S24	Closed	Enables the control of the EN LIN transceiver (PA5)
S25	Closed	Enables the control of the INH LIN transceiver (PA6)
S26	Opened	Do not use
S27	Closed	Enables the use of the User LED DS4 (PA25)
S28	Closed	Enables the use of the User LED DS3 (PA24)
S29	Closed	Enables the use of the User LED DS2 (PA21)
S30	Closed	Enables the use of the User LED DS1 (PA20)

Table 4-1. Configuration Jumpers and Straps (Continued)

Designation	Default Setting	Feature
S31	Closed	Enables the use of the DBGU TXD signal (PA31)
S32	Closed	Enables the use of the DBGU RXD signal (PA30)
S33	Opened	Disable VUSB power supply on J9 extension connector.
TP1	N.A	GND Test point
TP2	N.A	GND Test point
TP3	N.A	GND_ADC Test point

Note: 1. These jumpers are provided for measuring power consumption. By default, they are closed. To use this feature, the user has to open the strap and insert an anmeter.

Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Processor
- I/O

USB DEVICE INTERFACE

J1 USB B

S1

MN2 USBUF02W6

Q5 Si2301BDS

R2 100K

S3

USB_DP_PUP

PB1

Q1 Si2301BDS

R4 100K

C3 100NF

MN3 TPS73633

S6

Q2 Si2302BDS

S7

C15 1µF C16 1µF C17 10NF

TP1

ADHESIVE FEET

Z8 11.1 Z9 11.1 Z10 11.1 Z11 11.1

JTAG INTERFACE

MANUAL RESET

BP2

RR1 100K

J8

S2

J24 DNP

J25 DNP

R1 10K

NRST

J15

L1 4.7µH

C1 10 uF 10V

S5

GND_ADC

TP3 ANALOG GND

J17

MN4

3.00V +- 0.2%

C6 22NF

C9 10 uF 10V

LM4120AIM5-3.0

VREF

C5 100NF

C11 22NF

AT91SAM7A3

MN1

DDP DDM NRST TST JTAGSEL TDO TCK TMS TDI

VDDANA ADVREFP

C4 10 uF
C7 100NF
C8 100NF
C10 100NF

3V3 CURRENT MEASURE

J13

C2 10 uF
C12 100NF
C13 100NF
C14 100NF
C18 100NF

VDD1V8 VDD3V3 GND

S8 S9 J26

C19 10pF C20 10pF Y1 18.432MHz

XOUT XIN

J14 C21 100NF

VDDPLL

R5 470R R7 470R J16

C22 1NF C23 R6 1.5K 10NF

PLLRC VDDBU

C24 100NF

DNP Z18 3.6V Primary lithium-thionyl chloride

RR2 100K R8 3.3M

FORCEWUP WUP0 WUP1 SHDN

FWKUP WKUP0 WKUP1 SHDN

J10

FORCE WAKE-UP

WAKE-UP1

BP3 BP4

ADC1_AD7/SCK2/TIOB8/PB29
ADC1_AD6/CTS2/TIOA8/PB28
ADC1_AD5/RTS2/TIOB7/PB27
ADC1_AD4/SCK1/TIOA7/PB26
ADC1_AD3/CTS1/TIOB6/PB25
ADC1_AD2/RTS1/TIOA6/PB24
ADC1_AD1/TIOB5/PB23
ADC1_AD0/TIOA5/PB22
ADC0_AD7/NPCS13/TIOB4/PB21
ADC0_AD6/NPCS12/TIOA4/PB20
ADC0_AD5/NPCS11/TIOB3/PB19
ADC0_AD4/PWM4/TIOA3/PB18
ADC0_AD3/PWM3/TIOB2/PB17
ADC0_AD2/PWM2/TIOA2/PB16
ADC0_AD1/PWM1/TIOB1/PB15
ADC0_AD0/PWM0/TIOA1/PB14
RD1/TIOB0/PB13
TD1/TIOA0/PB12
RF1/TCLK2/PB11
RK1/TCLK1/PB10
TK1/TCLK0/PB9
TF1/FIQ/PB8
CANTX1/RF0/PB7
PCK3/RK0/PB6
PCK2/RD0/PB5
PCK1/TD0/PB4
PCK0/TK0/PB3
PWM7/TF0/PB2
PWM6/IRQ3/PB1
PWM5/IRQ2/PB0

PA0/TWD/ADC0_ADTRG
PA1/TWCK/ADC1_ADTRG
PA2/RXD0
PA3/TXD0
PA4/SCK0/SPI1_NPCS0
PA5/RTS0/SPI1_NPCS1
PA6/CTS0/SPI1_NPCS2
PA7/RXD1/SPI1_NPCS3
PA8/TXD1/SPI1_MISO
PA9/RXD2/SPI1_MOSI
PA10/TXD2/SPI1_SPCK
PA11/SPI0_NPCS0
PA12/SPI0_NPCS1/MCDA1
PA13/SPI0_NPCS2/MCDA2
PA14/SPI0_NPCS3/MCDA3
PA15/SPI0_MISO/MCDA0
PA16/SPI0_MOSI/MCCDA
PA17/SPI0_SPCK/MCCK
PA18/PWM0/PCK0
PA19/PWM1/PCK1
PA20/PWM2/PCK2
PA21/PWM3/PCK3
PA22/PWM4/IRQ0
PA23/PWM5/IRQ1
PA24/PWM6/TCLK4
PA25/PWM7/TCLK5
PA26/CANRX0
PA27/CANTX0
PA28/CANRX1/TCLK3
PA29/CANTX1/TCLK6
PA30/DRXD/TCLK7
PA31/DTXD/TCLK8

PB[0..29]

PA[0..31]

J9A

TWD	PA0	A1	
TWCK	PA1	A2	
RXD0	PA2	A3	
TXD0	PA3	A4	
SCK0	PA4	A5	
RTS0	PA5	A6	
CTS0	PA6	A7	
	PA7	A8	
	PA8	A9	
	PA9	A10	
	PA10	A11	
SPI0_NPCS0	PA11	A12	
SPI0_NPCS1	PA12	A13	
	PA13	A14	
	PA14	A15	
SPI0_MISO	PA15	A16	
SPI0_MOSI	PA16	A17	
SPI0_SPCK	PA17	A18	
	PA18	A19	
PCK1	PA19	A20	
	PA20	A21	
	PA21	A22	
IRQ0	PA22	A23	
	PA23	A24	
	PA24	A25	
PWM7	PA25	A26	
	PA26	A27	
	PA27	A28	
	PA28	A29	
	PA29	A30	
	PA30	A31	
	PA31	A32	

J9B

	PB0	B1
	PB1	B2
TF0	PB2	B3
TK0	PB3	B4
TD0	PB4	B5
RD0	PB5	B6
RK0	PB6	B7
RF0	PB7	B8
	PB8	B9
	PB9	B10
	PB10	B11
	PB11	B12
	PB12	B13
	PB13	B14
	PB14	B15
	PB15	B16
	PB16	B17
	PB17	B18
PWM4	PB18	B19
	PB19	B20
TIOA4	PB20	B21
TIOB4	PB21	B22
	PB22	B23
	PB23	B24
	PB24	B25
	PB25	B26
	PB26	B27
	PB27	B28
ADC1_AD6	PB28	B29
ADC1_AD7	PB29	B30
		B31
		B32

J9C

S33

		C1
		C2
RXD0		C3
TXD0		C4
SCK0		C5
RTS0		C6
CTS0		C7
SPI0_MISO		C8
SPI0_MOSI		C9
SPI0_SPCK		C10
SPI0_NPCS0		C11
SPI0_NPCS1		C12
TWD		C13
TWCK		C14
TF0		C15
TK0		C16
TD0		C17
RD0		C18
RK0		C19
RF0		C20
TIOA4		C21
TIOB4		C22
PCK1		C23
IRQ0		C24
PWM4		C25
PWM7		C26
		C27
		C28
ADC1_AD6		C29
ADC1_AD7		C30
		C31
		C32

USART SPI TWI SCC TIMER PCK IRQ PWM RESERVED ADC

TP2

C25 100NF MN5G

MN5F 74ALVC04

R9 120R

POWER LED DS5 YELLOW

MN5E 74ALVC04

R10 100K S10

PB15

PA8 SPI1_MISO
PA9 SPI1_MOSI
PA10 SPI1_SPCK
PA7 SPI1_NPCS3

S11

MN6

SO SI SCK CS RESET WP VCC GND

C26 100NF

R11 100K

NRST

S12

WRITE PROTECT NORMALLY OPEN

Friday, June 09, 2006

REV	MODIF.	DES.	DATE	VER.	DATE
C		JPG	13/09/05		
B		JPG	10/03/05		
A	INIT EDIT	JPG	08/12/04		

AT91SAM7A3-EK

PROCESSOR BOARD

SCALE 1/1

REV. C

SHEET 1/2

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CAN0

J5 · R13 120 · J18 · MN7 TJA1050T (TXD, RXD, RS, VREF, VCC, GND, CANH, CANL) · J19 DNP 5V · J20 DNP 3V3 · C28 10 uF 10V · C27 100NF

CAN1

J4 · R16 120 · J21 · MN8 TJA1050T (TXD, RXD, RS, VREF, VCC, GND, CANH, CANL) · J22 DNP 5V · J23 DNP 3V3 · C32 10 uF 10V · C31 100NF

DO NOT CONNECT J19 AND J20 AT THE SAME TIME

DO NOT CONNECT J22 AND J23 AT THE SAME TIME

LIN0

J3 · CR1 GF1B · CR2 GF1B · R22 1K · C37 47uF 50V · C38 220pF · MN10 ATA6661 (VS, TXD, RXD, EN, INH, WAKE, LIN, GND) · 10K R19 · 3.3K R20 · S26 · C39 100NF

USART0

TXD0 S22 PA3 · RXD0 S23 PA2 · RTS0 S24 PA5 · CTS0 S25 PA6

SERIAL DEBUG PORT

J2 MALE RIGHT ANGLED · MN11 ADM3202ARN (VCC, GND, V+, V-, C1+, C1-, C2+, C2-, T, R) · C40 100NF · C41 100NF · C42 100NF · C43 100NF · C44 100NF · R25 100K

DBGU_TXD S31 PA31 · DBGU_RXD S32 PA30

PA[0..31]

SD CARD / MMC CARD DATAFLASH CARD INTERFACE

J7 FPS009 · R12 10K · C29 100NF · C36 1µF

PA12 MCDA1 · PA15 SPI0_MISO MCDA0 · PA17 SPI0_SPCK MCCK · PA16 SPI0_MOSI MCCDA · PA14 SPI0_NPCS3 MCDA3 · PA13 MCDA2

VREF · Q3 Si2301BDS · R14 10K · R15 82K · R17 10K · C30 100NF · MN9A TLC2272A · R18 100K · Q4 Si2302BDS · PWM 0 · S19 PA18

S20 PB16 · CR3 BAT54 · MN9B TLC2272A · C33 100NF · C34 10 uF 10V · S21 PB17 · R28 1K · R21 1K · C35 100NF · J6

PB[0..29]

USER INTERFACE

MN5A 74ALVC04 · S27 PA25 · R23 120R · DS4 GREEN

MN5B 74ALVC04 · S28 PA24 · R24 120R · DS3 GREEN

MN5C 74ALVC04 · S29 PA21 · R26 120R · DS2 GREEN

MN5D 74ALVC04 · S30 PA20 · R27 120R · DS1 GREEN

100K RR3

PB13 PB8 PB12 PB14 PB9 · BP1

UP = PB8
DOWN = PB9
LEFT = PB12
RIGHT = PB13
PUSH = PB14

Friday, June 09, 2006

REV	MODIF.	DES.	DATE	VER.	DATE
C		JPG	13/09/05		
B		JPG	10/03/05		
A	INIT EDIT	JPG	08/12/04		

ATMEL ROUSSET

AT91SAM7A3-EK

I/O

SCALE 1/1 · REV. C · SHEET 2/2

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Section 6

Revision History

6.1 Revision History

Table 6-1.

Document	Comments	Change Request Ref.
6165A	First issue.	
6165B	Added information on SAM-BA in Section 2.6.	05-415
6165C	Removed references to 32 Mbit serial DataFlash (AT45DB321C-CNC) in Section 1.3 and in Section 3.3. Inserted new Figure 2-2 and new schematics in Section 5.	2846

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