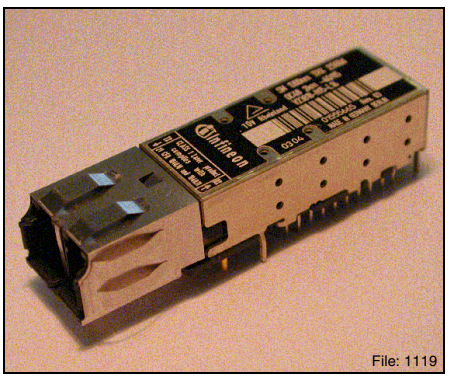
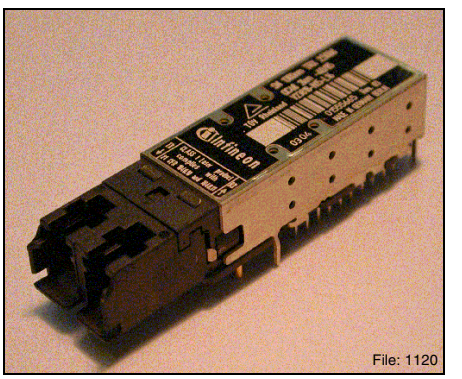
Small Form Factor
Single Mode 1300 nm
Multirate up to 2.5 Gbit/s Transceiver
2x5/2x10 Pinning with LC™ Connector

V23818-N15-Lxx/Lxxx

Features

- Small Form Factor transceiver
- RJ-45 style LC™ connector system
- Half the size of SC Duplex 1x9 transceiver
- Optimized for SDH STM-16 / SONET OC-48
- Single power supply (3.3 V)
- Extremely low power consumption
- Loss of optical signal indicator
- Laser disable input
- LVPECL differential inputs and outputs
- Suitable for multirate applications up to 2.5 Gbit/s
- Distance up to 2 km on single mode fiber (SMF)
- Class 1 FDA and IEC laser safety compliant
- Multisource footprint
- Small footprint for high channel density
- UL 94 V-0 certified
- Compliant with FCC (Class B) and EN 55022
- Tx and Rx power monitor


File: 1119


File: 1120

For ordering information see next page.
LC™ is a trademark of Lucent.

Ordering Information

Part Number	Pinning	Signal Detect	Operating Temperature	Data Outputs if SD is Low	Collar	In-put	Out-put
V23818-N15-L17	2x10	LVPECL	–5...70°C	Switched to Low	yes	DC	DC
V23818-N15-L16			–40...85°C				
V23818-N15-L353		LVTTL	–5...70°C			AC	AC
V23818-N15-L356			–40...85°C				
V23818-N15-L354		LVTTL	–5...70°C				
V23818-N15-L355					no		
V23818-N15-L37	2x5	LVPECL	–5...70°C	Switched to Low	yes	DC	DC
V23818-N15-L36			–40...85°C				
V23818-N15-L47		LVTTL	–5...70°C			AC	AC
V23818-N15-L46			–40...85°C				
V23818-N15-L457	2x10	LVTTL	–5...70°C	Active	yes	AC	AC
V23818-N15-L356-C	2x10	LVTTL	–40...85°C	Switched to Low	yes[1)]	AC	AC

[1)] Incorporates non-standard collar type (see **Figure 20** on **Page 26**).

Pin Configuration

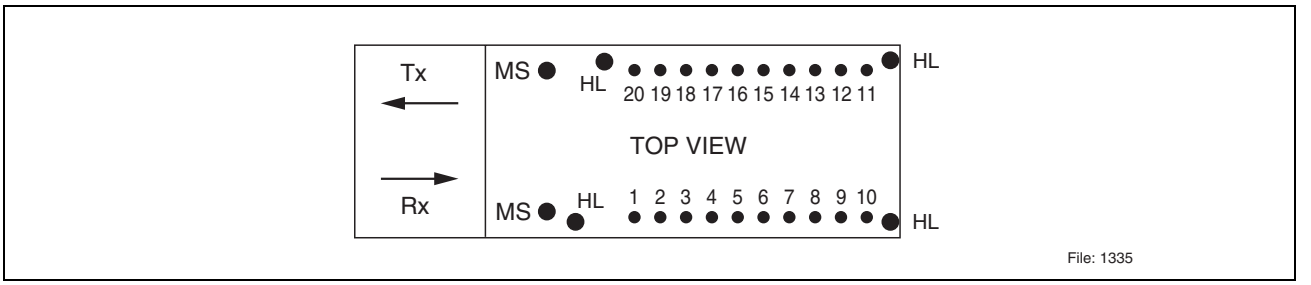


Figure 1 2x10 Pin Connect Diagram

2x10 Pin Description

Pin No.	Symbol	Level/Logic	Description
1	PDBias	DC current	PIN photo detector bias current
2	V_{EEr}	Ground	Receiver signal ground
3	V_{EEr}	Ground	Receiver signal ground
4	NC		Not connected
5	NC		Not connected
6	V_{EEr}	Ground	Receiver signal ground
7	V_{CCr}	Power supply	Receiver power supply
8	SD	LVTTL or LVPECL output[1)]	Receiver optical input level monitor
9	RD–	LVPECL output	Receiver data out bar
10	RD+	LVPECL output	Receiver data out
11	V_{CCt}	Power supply	Transmitter power supply
12	V_{EEt}	Ground	Transmitter signal ground
13	TDis	LVTTL input	Transmitter disable
14	TD+	LVPECL input	Transmitter data in
15	TD–	LVPECL input	Transmitter data in bar
16	V_{EEt}	Ground	Transmitter signal ground
17	BMon–	DC voltage	Laser diode bias current monitor
18	BMon+	DC voltage	Laser diode bias current monitor
19	PMon–	DC voltage	Laser diode optical power monitor
20	PMon+	DC voltage	Laser diode optical power monitor
MS			Mounting studs
HL			Housing leads

[1)] LVPECL output active high for V23818-N15-L17/L16/L417/L373.
LVTTL output active high for V23818-N15-L353/L356/L457/L355/L354.

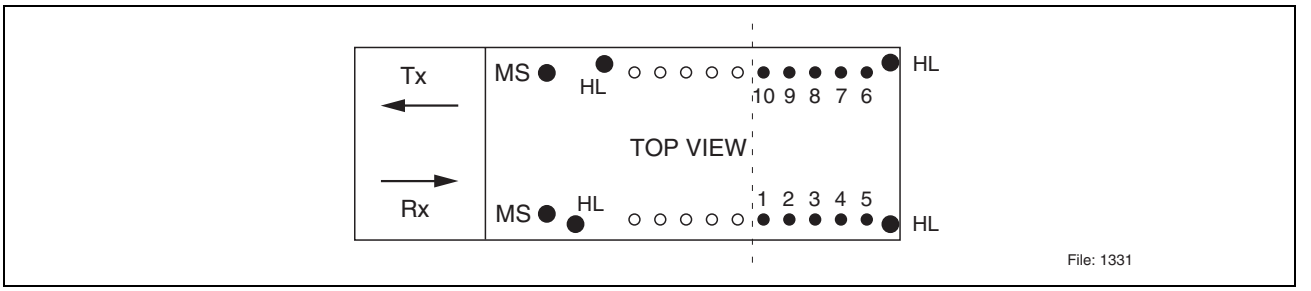


Figure 2 2x5 Pin Connect Diagram

2x5 Pin Description

Pin No.	Symbol	Level/Logic	Description
1	V_{EEr}	Ground	Receiver signal ground
2	V_{CCr}	Power supply	Receiver power supply
3	SD	LVTTL or LVPECL output[1)]	Receiver optical input level monitor
4	RD–	LVPECL output	Receiver data out bar
5	RD+	LVPECL output	Receiver data out
6	V_{CCt}	Power supply	Transmitter power supply
7	V_{EEt}	Ground	Transmitter signal ground
8	TDis	LVTTL input	Transmitter disable
9	TD+	LVPECL input	Transmitter data in
10	TD–	LVPECL input	Transmitter data in bar
MS			Mounting studs
HL[2)]			Housing leads

1) LVPECL output active high for V23818-N15-L37/L36.
LVTTL output active high for V23818-N15-L47/L46.

2) Housing leads removed for V23818-N15-L46WH. Due to possible EMI performance issues, use of this transceiver should be restricted to applications where the chassis is completely sealed and the transceiver encapsulated within.

V_{EEr} / V_{EEt}

For 2x10 transceivers, connect pins 2, 3, 6, 12 and 16 to signal ground. For 2x5 transceivers, connect pins 1 and 7 to signal ground.

V_{CCr} / V_{CCt}

For 2x10 transceivers a 3.3 V DC power supply must be applied at pins 7 and 11. For 2x5 transceivers a 3.3 V DC power supply must be applied at pins 2 and 6. A recommended power supply filter network is given in the termination scheme. Locate power supply filtering directly at the transceiver power supply pins. Proper power supply filtering is essential for good EMI performance.

TD+ / TD–

Transmitter data LVPECL level inputs. For V23818-N15-L353/L356/L457/L354/L355/L47/L46/L373 terminated and AC coupled internally. For V23818-N15-L17/L16/L417/L37/L36 use termination and coupling as shown in the termination scheme.

RD– / RD+

Receiver data LVPECL level outputs. For V23818-N15-L353/L356/L457/L354/L355/L47/L46/L373 biased and AC coupled internally. For V23818-N15-L17/L16/L417/L37/L36 use termination and coupling as shown in the termination scheme.

TDis

A logical LVTTL high input will disable the laser. To enable the laser, an LVTTL low input must be applied. Leave pin unconnected if feature not required.

SD

LVTTL output for V23818-N15-L353/L356/L457/L354/L355/L47/L46.
LVPECL output for V23818-N15-L17/L16/L417/L37/L36/L373.
A logical high output indicates normal optical input levels to the receiver. Low optical input levels at the receiver result in a low output. Signal Detect can be used to determine a definite optical link failure; break in fiber, unplugging of a connector, faulty laser source. However it is not a detection of a bad link due to data-related errors.

MS

Mounting studs are provided for transceiver mechanical attachment to the circuit board. They also provide an optional connection of the transceiver to the equipment chassis ground. The holes in the circuit board must be tied to chassis ground.

HL

Housing leads are provided for additional signal grounding. The holes in the circuit board must be included and tied to signal ground.

2x10 Transceiver Additional Functionality

PDBias

Connect pin 1 to V_{CC} through a bias resistor, of a value not exceeding 2 kΩ, as shown in **Figure 3** to monitor PIN photo detector bias current. Leave pin floating if not used. Typical behaviour is shown in **Figure 4** and **Figure 5** using a 2 kΩ load.

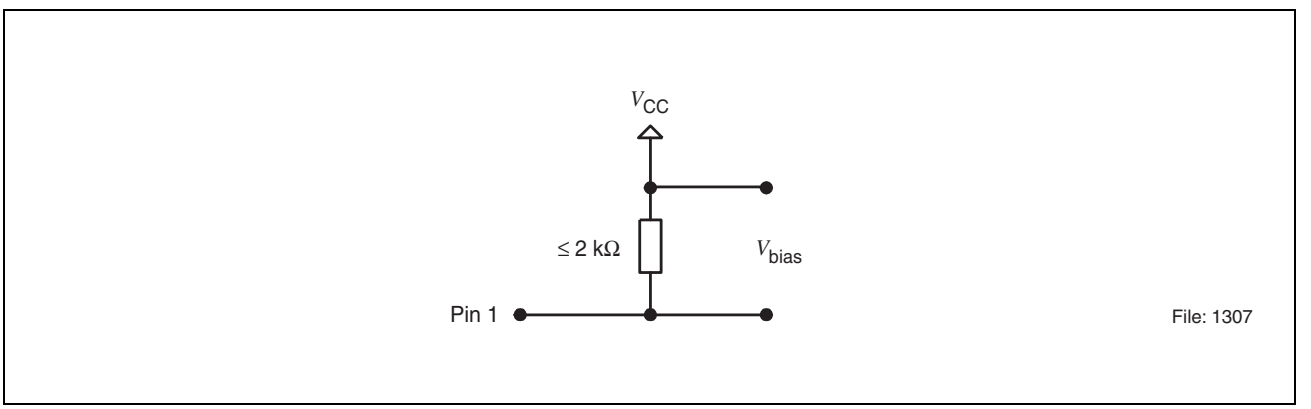
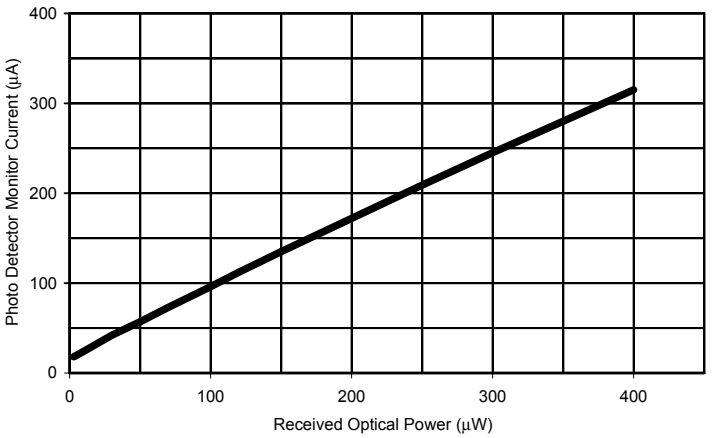


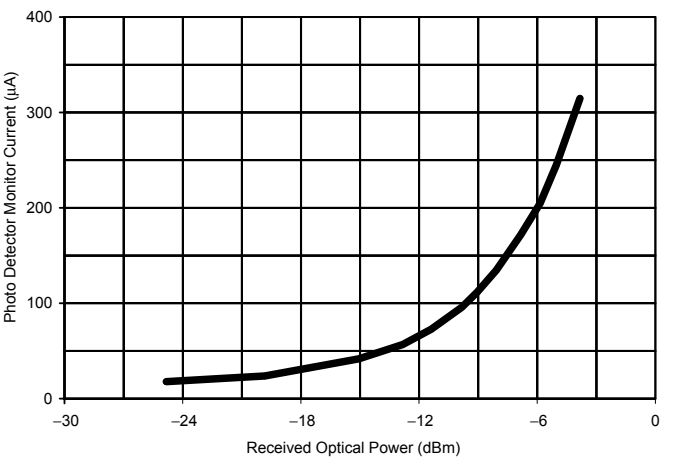
Figure 3 Photo Detector Bias Interface

Typical Responsitivity of PIN Photo Detector Bias Current Monitor



File: 1308

Figure 4 Linear Response



File: 1309

Figure 5 Logarithmic Response

BMon– / BMon+

The DC voltage measured across pins 17 and 18 is proportional to the laser bias current. Use the equation:

$I_{bias} = V_{bias}/10\ \Omega$

Use this output to monitor laser performance and EOL conditions. A schematic and typical behaviour are shown in **Figure 6** and **Figure 7**. I_{bias} @ ambient 25°C < 60 mA. Leave pins floating if function is not required.

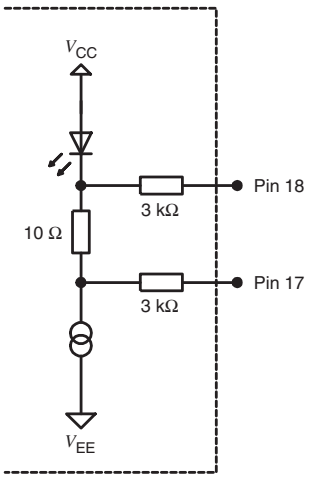


Figure 6 Bias Monitor – Transceiver Internal

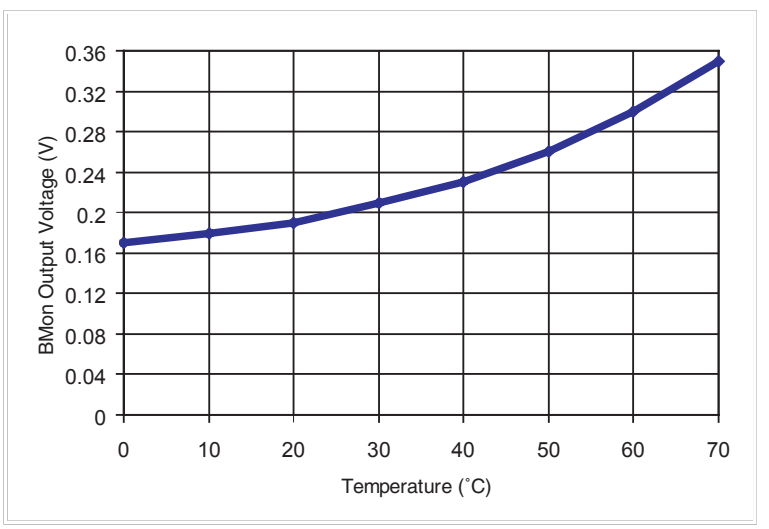


Figure 7 Typical Variations of Bias Monitor Voltage over Temperature

PMon– / PMon+

The DC voltage that can be measured across pins 19 and 20 is proportional to the laser monitor diode current through a 200 Ω resistor in its path. This output remains constant and can be used to monitor correct operation of laser control circuitry, a deviation indicates faulty behaviour. A schematic and typical behaviour are shown in **Figure 8** and **Figure 9**. The SFF MSA defines that V_{mon} must be in the range of 0.01 V and 0.2 V. The Infineon OC-48 transceiver has a nominal range of 0.04 to 0.08 V. Leave pins unconnected if feature is not required.

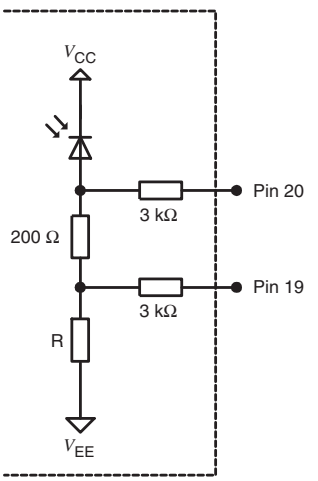


Figure 8 Power Monitor – Transceiver Internal

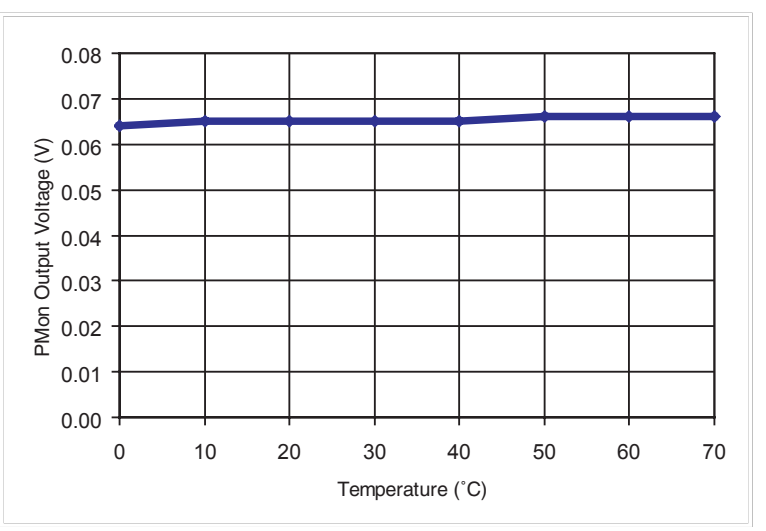


Figure 9 Typical Behaviour of Power Monitor Voltage over Temperature

Description

The Infineon 2.5 Gigabit single mode transceiver – part of the Infineon Small Form Factor transceiver family – is based on the Physical Medium Depend (PMD) sublayer and baseband medium, type 2000 Base-LX, compliant with ITU-T G.957 STM-16, S-16.1 and SONET OC-48 SR-1.

This transceiver is also suitable for multirate applications. The performance at lower datarates may vary from application to application and is link dependent. Refer to Infineon Application Note 97 for more information.

The appropriate fiber optic cable is 9 µm single mode fiber with LC connector.

The Infineon OC-48 single mode transceiver is a single unit comprised of a transmitter, a receiver, and an LC receptacle. This design frees the customer from many alignment and PC board layout concerns.

This transceiver supports the LC connectorization concept, which competes with UTP/ CAT 5 solutions. It is compatible with RJ-45 style backpanels for fiber-to-the-desktop applications while providing the advantages of fiber optic technology. The transmission distance is up to 2 km.

The module is designed for low cost LAN, WAN, and up to 2.5 Gbit/s applications. It can be used as the network end device interface in mainframes, workstations, servers, and storage devices, and in a broad range of network devices such as bridges, routers, hubs, and local and wide area switches.

This transceiver operates at up to 2.5 Gbit/s from a single power supply (+3.3 V). The full differential data inputs and outputs are LVPECL compatible.

Functional Description of SFF Transceiver

This transceiver is designed to transmit serial data via single mode fiber.

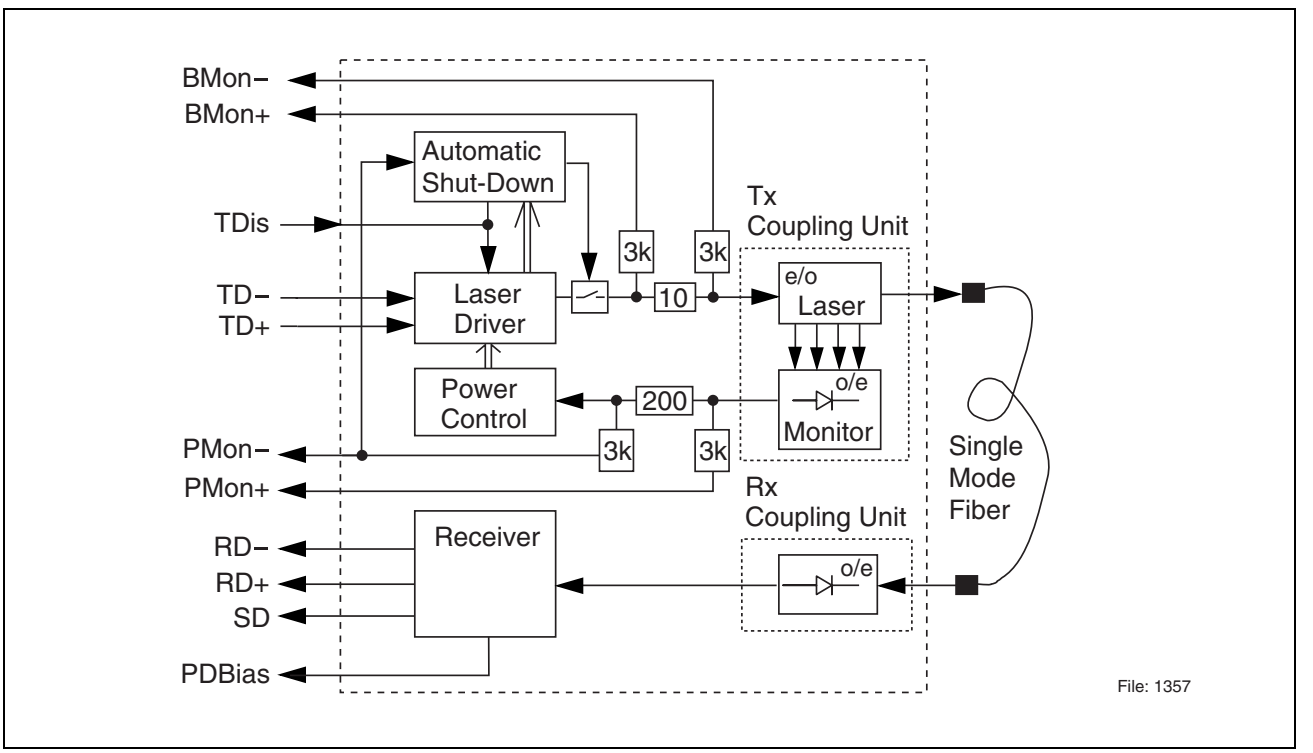


Figure 10 Functional Diagram 2x10 Pin Rows

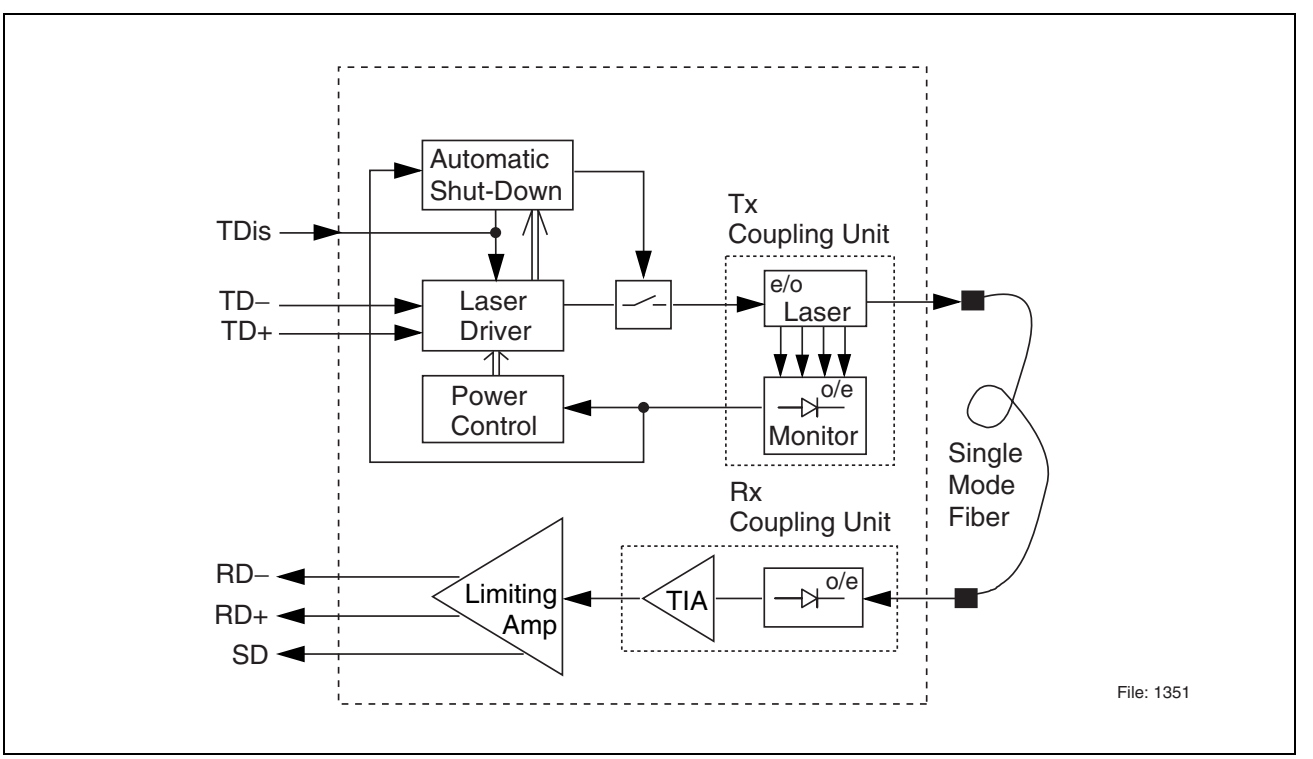


Figure 11 Functional Diagram 2x5 Pin Rows

The receiver component converts the optical serial data into an electrical data (RD+ and RD–). The Signal Detect output (SD) shows whether an optical signal is present.

The transmitter part converts electrical LVPECL compatible serial data (TD+ and TD–) into optical serial data.

The module has an integrated shutdown function that switches the laser off in the event of an internal failure.

Reset is only possible if the power is turned off, and then on again. (V_{CCt} switched below V_{TH}).

The transmitter contains a laser driver circuit that drives the modulation and bias current of the laser diode. The currents are controlled by a power control circuit to guarantee constant output power of the laser over temperature and aging. The power control uses the output of the monitor PIN diode (mechanically built into the laser coupling unit) as a controlling signal, to prevent the laser power from exceeding the operating limits.

Regulatory Compliance

Feature	Standard	Comments
ESD: Electrostatic Discharge to the Electrical Pins	EIA/JESD22-A114-B (MIL-STD 883D Method 3015.7)	Class 1C
Immunity: Against Electrostatic Discharge (ESD) to the Duplex LC Receptacle	EN 61000-4-2 IEC 61000-4-2	Discharges ranging from ±2 kV to ±15 kV on the receptacle cause no damage to transceiver (under recommended conditions).
Immunity: Against Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 61000-4-3	With a field strength of 3 V/m, noise frequency ranges from 10 MHz to 2 GHz. No effect on transceiver performance between the specification limits.
Emission: Electromagnetic Interference (EMI)	FCC 47 CFR Part 15, Class B EN 55022 Class B CISPR 22	Noise frequency range: 30 MHz to 18 GHz

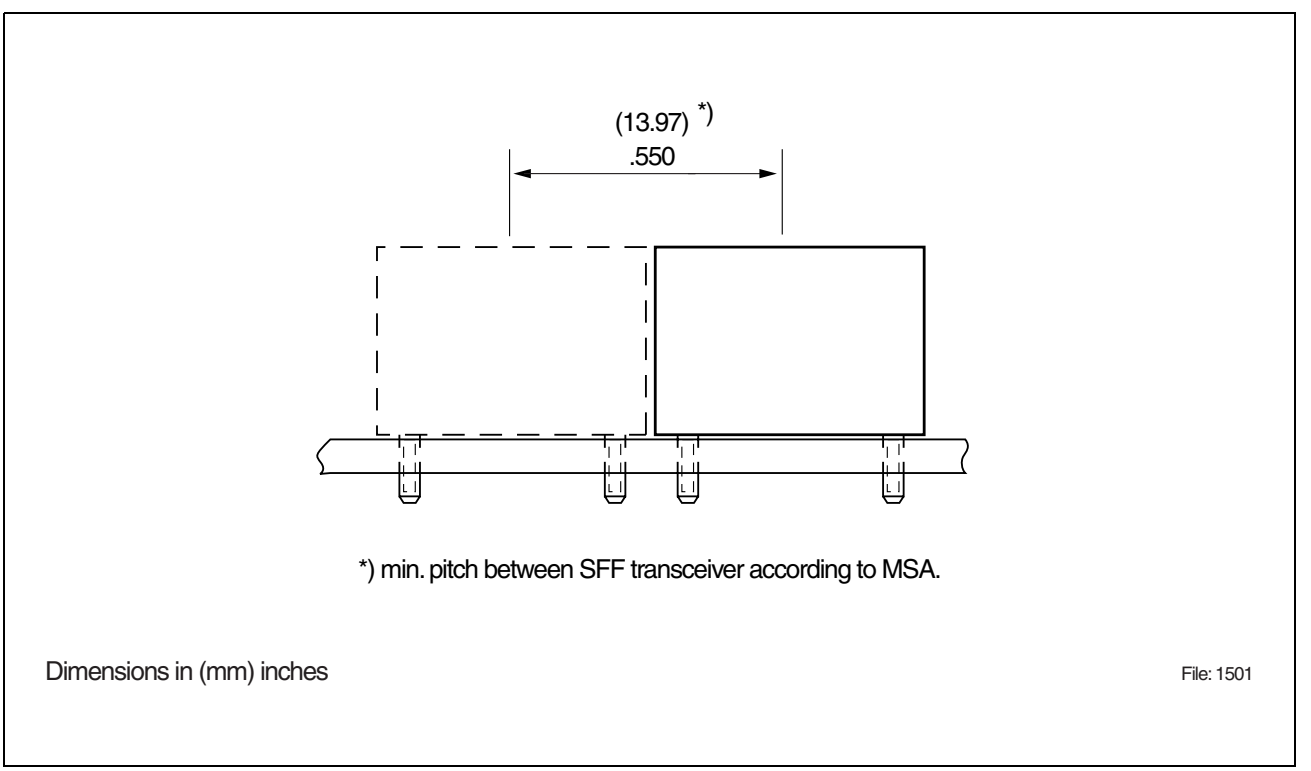


Figure 12 Transceiver Pitch

Technical Data

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Package Power Dissipation			0.9	W
Supply Voltage	V_{CC}–V_{EE}		4	V
Data Input Levels		V_{CC}+0.5	V_{EE}–0.5	V
Differential Data Input Voltage Swing	V_{ID}pk-pk		5	V
PIN PDBias Voltage			4	V
Storage Ambient Temperature		–40	85	°C
Hand Lead Soldering Temp/Time			260/10	°C/s
Wave Soldering Temp/Time			260/10	°C/s
Aqueous Wash Pressure			< 110	psi

Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Ambient Temperature[1), 3)]	T_{AMB}	–40		85	°C
Ambient Temperature[2), 3)]		–5		70	
Power Supply Voltage	$V_{CC}–V_{EE}$	3.14	3.3	3.46	V
Transmitter					
Supply Current Tx	I_{CCt}			110	mA
Data Input High Voltage	$V_{IH}–V_{CC}$	–1165		–880	mV
Differential Data Input Voltage Swing[4)]	V_{ID}pk-pk	500		3200	mV
Data Input Low Voltage	$V_{IL}–V_{CC}$	–1810		–1475	mV
Data Input Rise/Fall Time (20% - 80%)	t_i			120	ps
Receiver					
Supply Current Rx	I_{CCr}			120	mA
Input Center Wavelength	λ_{Rx}	1260		1580	nm

1) Only for V23818-N15-Lx6/Lxx6.

2) Not for V23818-N15-Lx6/Lxx6.

3) Ambient operating temperature requires a 2 ms^{-1} airflow over the device.

4) V23818-N15-L353/L356/L457/L354/L355/L47/L46/L373 are internally AC coupled. External coupling capacitors required only for V23818-N15-L17/L16/L417/L37/L36.

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

Transmitter Electro-Optical Characteristics

Transmitter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Output Power (Average) [1]	P_O	–10		–3	dBm
Output Power (Average) [2]		–8		–3	
Center Wavelength	λ_C	1266		1360	nm
Spectral Width (RMS)	σ			4	nm
Side Mode Suppression Ratio	SMSR	30			dB
Extinction Ratio (Dynamic)	ER	8.2			dB
Optical Eye Mask	ED	Compliant with ITU-T G.957			
Reset Threshold for V_{CCt} [3]	V_{TH}	2.2		2.99	V
Power on Delay [3]	t_{DEL}		30		ms
Jitter Generation [4]	J_{GE}p-p		0.04		UI
Jitter Generation [4]	J_{GE}RMS		0.004		UI
Rise Time [5]	t_R			70	ps
Fall Time [5]	t_F			225	ps
T_{Dis} Assert Voltage TTL	V_{TDH}	2			V
T_{Dis} Deassert Voltage TTL	V_{TDL}			0.8	V
T_{Dis} Assert Time [6]	t_{ASS}		0.4	1	ms
T_{Dis} Deassert Time [7]	t_{DAS}		0.06	10	µs

[1] Not for V23818-N15-L354/L355.
[2] Only for V23818-N15-L354/L355.
[3] Laser power is shut down if power supply is below V_{TH} and switched on if power supply is above V_{TH} after t_{DEL}.
[4] Jitter Generation under worst case conditions reaches a maximum value of 0.06 UI pk-pk/0.006 UI RMS.
[5] Measured using 20% - 80% levels without bandwidth filtering.
[6] T_{Dis} assertion to laser shutdown.
[7] T_{Dis} reassertion to laser startup.

Jitter

The transceiver is specified to meet the SONET Jitter performance as outlined in ITU-T G.958 and Telcordia GR-253.

Jitter Generation is defined as the amount of jitter that is generated by the transceiver. The Jitter Generation specifications are referenced to the optical OC-48 signals. If no or minimum jitter is applied to the electrical inputs of the transmitter, then Jitter Generation can simply be defined as the amount of jitter on the Tx optical output. The SONET specifications for Jitter Generation are 0.01 UI RMS, maximum and 0.1 UI pk-pk, maximum. Both are measured with a 12 kHz - 20 MHz filter in line. A UI is a Unit Interval, which is equivalent to one bit slot. At OC-48, the bit slot is 400 ps, so the Jitter Generation specification translates to 4 ps RMS, max. and 40 ps pk-pk, max.

Receiver Electro-Optical Characteristics

Receiver	Symbol	Limit Values			Unit
		min.	typ.	max.	
Sensitivity (Average Power)[1]	P_{IN}			–19	dBm
Saturation (Average Power)	P_{SAT}	–3			dBm
Signal Detect Assert Level[2]	P_{SDA}			–19	dBm
Signal Detect Deassert Level[3]	P_{SDD}	–30			dBm
Signal Detect Hysteresis	$P_{SDA} - P_{SDD}$		3		dB
Signal Detect Assert Time[2]	t_{ASS}			0.1	ms
Signal Detect Deassert Time[3]	t_{DAS}			0.35	ms
Data Output High Voltage[4]	$V_{OH}–V_{CC}$	–1110		–650	mV
Differential Data Output Voltage Swing	V_{OD}pk-pk	500		1000	mV
Data Output Low Voltage[4]	$V_{OL}–V_{CC}$	–1800		–1300	mV
Signal Detect Output High Voltage PECL[5], [6]	$V_{SDH}–V_{EE}$	V_{CC} –1200		V_{CC} –820	mV
Signal Detect Output Low Voltage PECL[5], [6]	$V_{SDL}–V_{EE}$	V_{CC} –1900		V_{CC} –1580	mV
Signal Detect Output High Voltage TTL[5], [7]	V_{SDH}	2.4			V
Signal Detect Output Low Voltage TTL[5], [7]	V_{SDL}			0.5	V
Photo Detector Bias Responsivity[8]	$PDBias_{RES}$	0.5		1	A/W
Photo Detector Bias Offset	$PDBias_{OFF}$	5		15	µA
Reflectance	P_{REF}		–33	–27	dB

[1] Minimum average optical power at which the BER is less than $1x10^{-10}$. Measured with a $2^{23}–1$ NRZ PRBS as recommended by ANSI T1E1.2, SONET OC-48, and ITU-T G.957 S-16.1.

[2] An increase in optical power above the specified level will cause the Signal Detect to switch from a low state to a high state (high active output).

[3] A decrease in optical power below the specified level will cause the Signal Detect to switch from a high state to a low state.

[4] Load is 100 Ω differential.

[5] Internal load is 510 Ω to GND, no external load necessary. Signal Detect is a high active output. High level means signal is present, low level means loss of signal.

[6] For V23818-N15-L17/L16/L417/L37/L36/L373.

[7] For V23818-N15-L353/L356/L457/L354/L355/L47/L46.

[8] Monitor current needs to be sunk to V_{CC}.

Eye Safety

This laser based single mode transceiver is a Class 1 product.
It complies with IEC 60825-1 and FDA 21 CFR 1040.10 and 1040.11.

The transceiver has been certified with FDA under accession number 9520890.

To meet laser safety requirements the transceiver shall be operated within the Absolute Maximum Ratings.

Attention: All adjustments have been made at the factory prior to shipment of the devices. No maintenance or alteration to the device is required. Tampering with or modifying the performance of the device will result in voided product warranty.

Note: Failure to adhere to the above restrictions could result in a modification that is considered an act of "manufacturing", and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration (ref. 21 CFR 1040.10 (i)).

Laser Data

Wavelength	1300 nm
Total Output Power (as defined by IEC: 7 mm aperture at 14 mm distance)	< 2 mW
Total Output Power (as defined by FDA: 7 mm aperture at 20 cm distance)	< 180 µW
Beam Divergence	6°

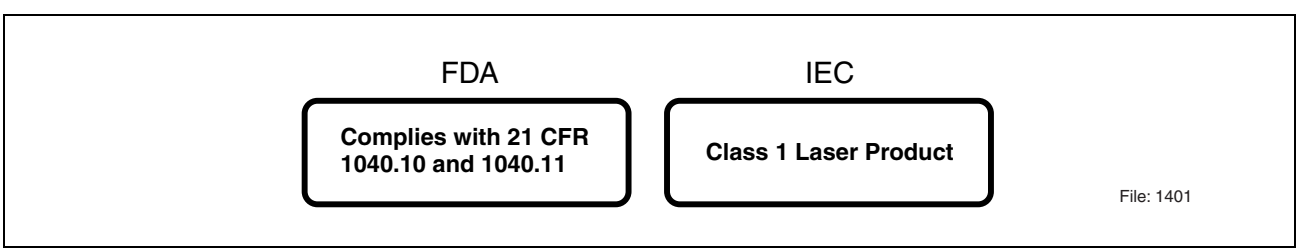


Figure 13 Required Labels

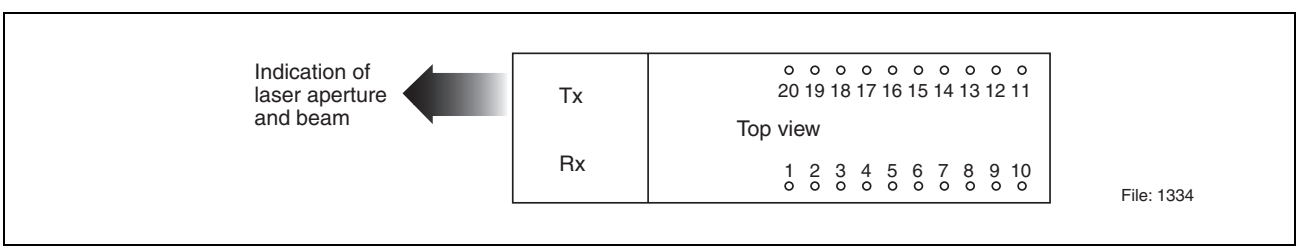


Figure 14 Laser Emission

EMI-Recommendations

To avoid electromagnetic radiation exceeding the required limits please take note of the following recommendations.

When Gigabit switching components are found on a PCB (multiplexers, clock recoveries etc.) any opening of the chassis may produce radiation also at chassis slots other than that of the device itself. Thus every mechanical opening or aperture should be as small as possible.

On the board itself every data connection should be an impedance matched line (e.g. strip line, coplanar strip line). Data, Datanot should be routed symmetrically, vias should be avoided. A terminating resistor of 100 Ω should be placed at the end of each matched line. An alternative termination can be provided with a 50 Ω resistor at each (D, Dn). In DC coupled systems a thevenin equivalent 50 Ω resistance can be achieved as follows: for 3.3 V: 125 Ω to V_{CC} and 82 Ω to V_{EE}, for 5 V: 82 Ω to V_{CC} and 125 Ω to V_{EE} at Data and Datanot. Please consider whether there is an internal termination inside an IC or a transceiver.

In certain cases signal GND is the most harmful source of radiation. Connecting chassis GND and signal GND at the plate/bezel/chassis rear e.g. by means of a fiber optic transceiver may result in a large amount of radiation. Even a capacitive coupling between signal GND and chassis may be harmful if it is too close to an opening or an aperture.

If a separation of signal GND and chassis GND is not planned, it is strongly recommended to provide a proper contact between signal GND and chassis GND at every location where possible. This concept is designed to avoid hotspots. Hotspots are places of highest radiation which could be generated if only a few connections between signal and chassis GND exist. Compensation currents would concentrate at these connections, causing radiation.

By use of Gigabit switching components in a design, the return path of the RF current must also be considered. Thus a split GND plane of Tx and Rx portion may result in severe EMI problems.

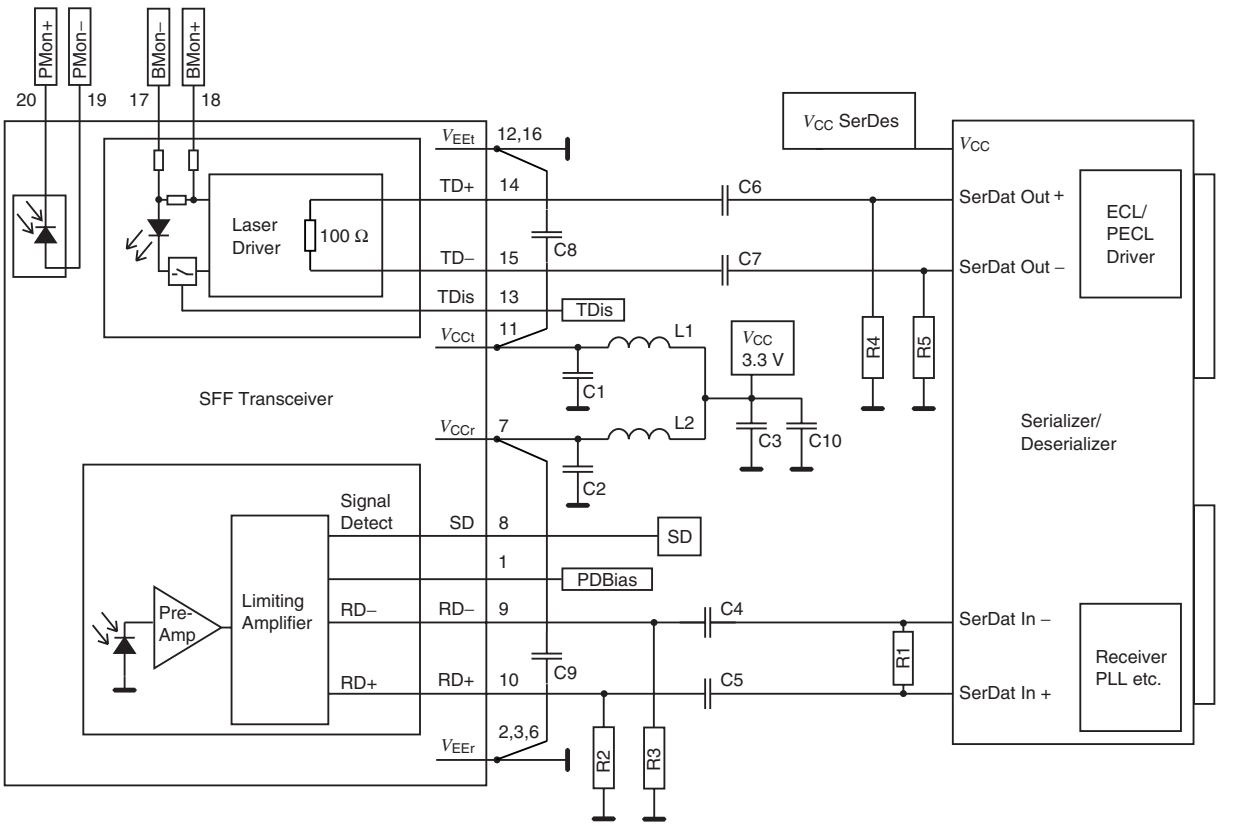
A recommendation is to connect the housing leads to signal GND. However, in certain applications it may improve EMI performance by connecting them to chassis GND.

The cutout should be sized so that all contact springs make good contact with the face plate.

Please consider that the PCB may behave like a waveguide. With an ε_r of 4, the wavelength of the harmonics inside the PCB will be half of that in free space. In this scenario even the smallest PCBs may have unexpected resonances.

Recommended Termination Schemes

2x10 DC/DC Transceiver

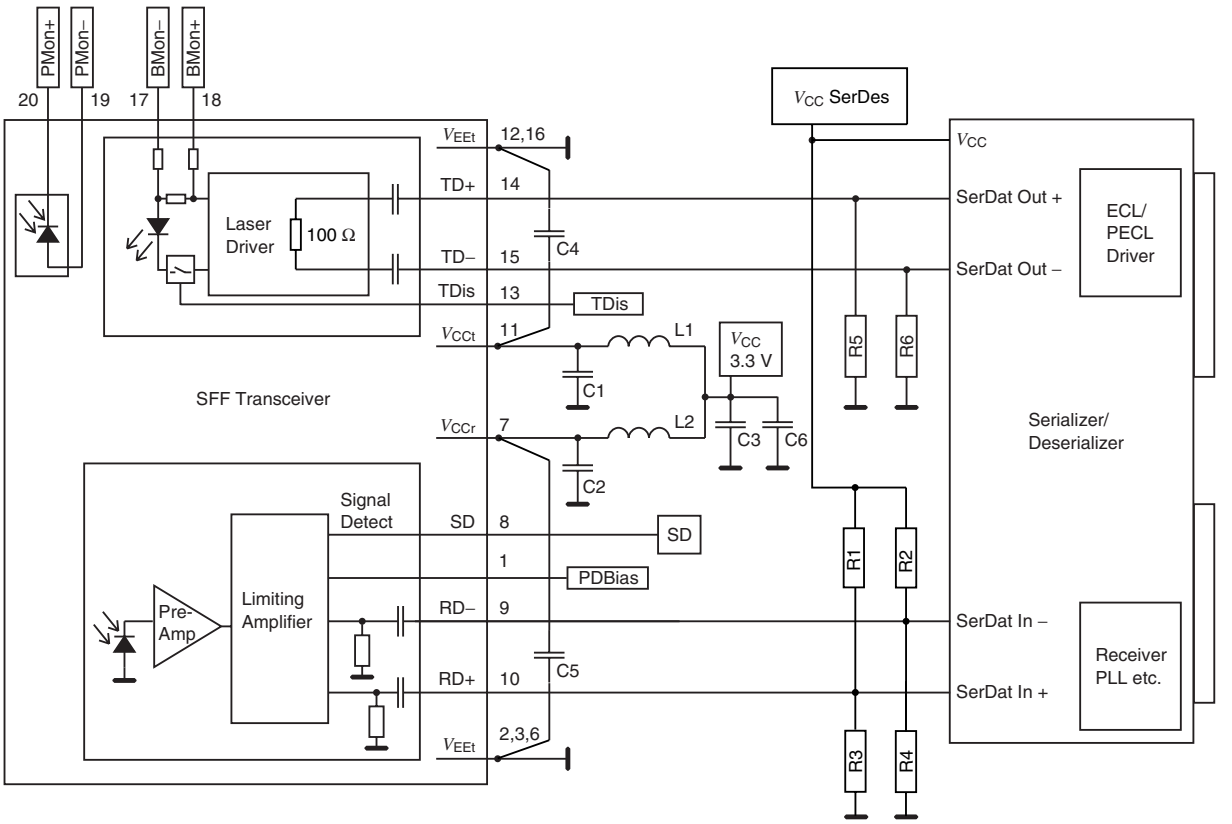


C1/2/3 = 4.7 ... 10 µF
C4/5/6/7 = 100 nF
C8/9/10 = Design criterion is the resonance frequency only. The self resonant frequency of the capacitor must be in the vicinity of the nominal data rate. Short traces are mandatory.
L1/2*) = 1 ... 4.7 µH
R1 = 100 Ω (depending on SerDes chip used, ensure proper 50 Ω termination to V_{EE} or 100 Ω differential is provided. Check for termination inside of SerDes chip).
R2/3 = 150 Ω
R4/5 = Biasing (depends on SerDes chip).
Place R1/4/5 close to SerDes chip.
Place R2/3 close to Infineon transceiver.
*) The inductors may be replaced by appropriate Ferrite beads.

File: 1390

Figure 15

2x10 AC/AC Transceiver



C1/2/3 = 4.7 ... 10 µF

C4/5/6 = Design criterion is the resonance frequency only. The self resonant frequency of the capacitor must be in the vicinity of the nominal data rate. Short traces are mandatory.

L1/2*) = 1 ... 4.7 µH

R1/2/3/4 = Depends on SerDes chip used, ensure proper 50 Ω termination to V_{EE} or 100 Ω differential is provided. Check for termination inside of SerDes chip.

R5/6 = Biasing (depends on SerDes chip).

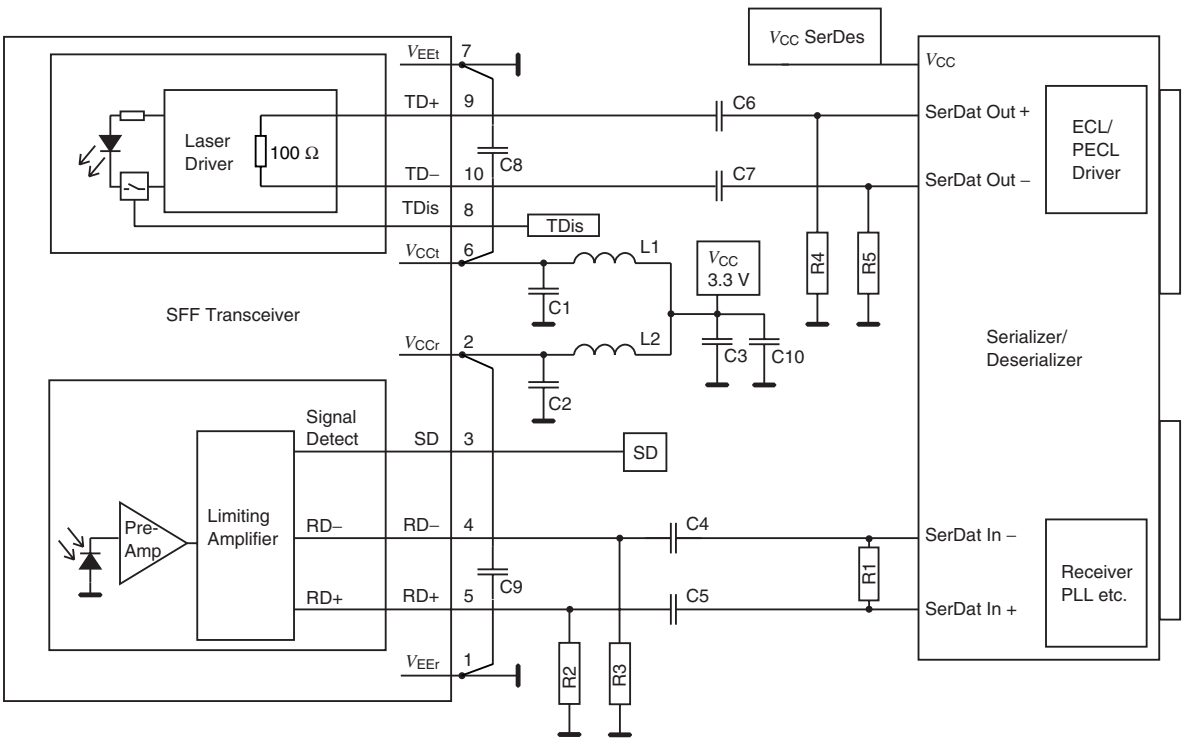
Place R1/2/3/4/5/6 close to SerDes chip.

*) The inductors may be replaced by appropriate Ferrite beads.

File: 1391

Figure 16

2x5 DC/DC Transceiver

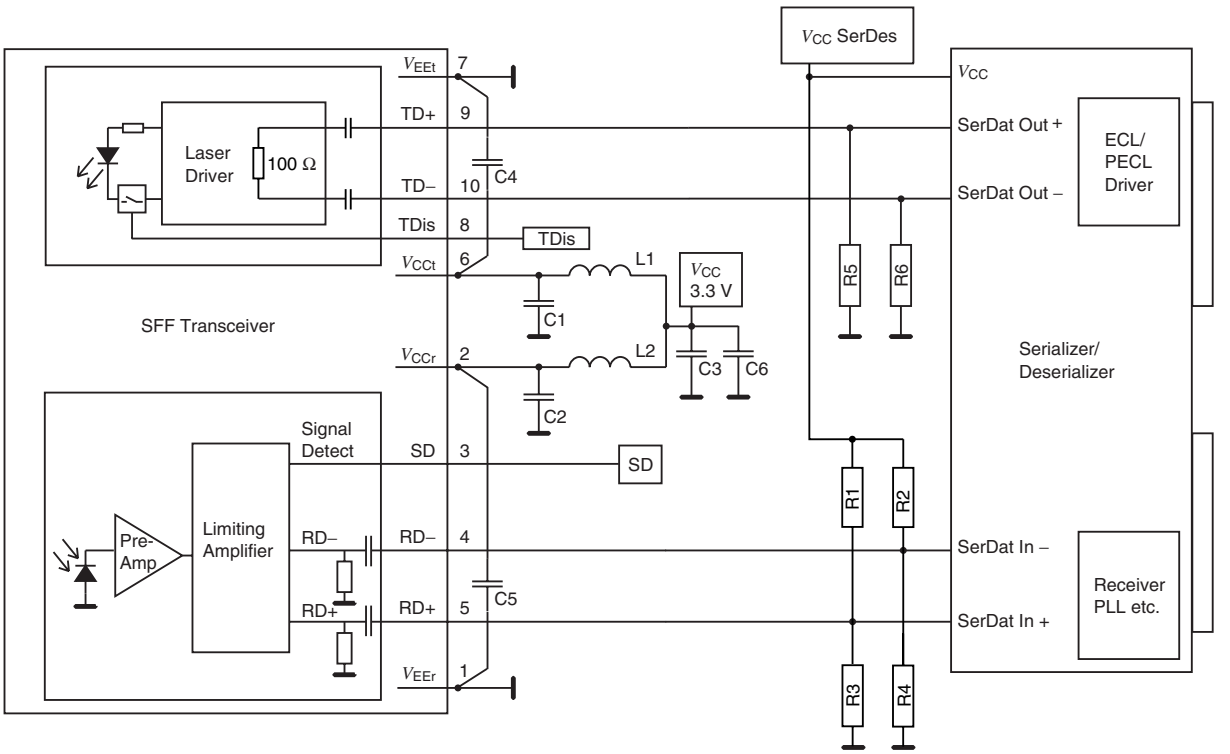


C1/2/3 = 4.7 ... 10 µF
C4/5/6/7 = 100 nF
C8/9/10 = Design criterion is the resonance frequency only. The self resonant frequency of the capacitor must be in the vicinity of the nominal data rate. Short traces are mandatory.
L1/2*) = 1 ... 4.7 µH
R1 = 100 Ω (depending on SerDes chip used, ensure proper 50 Ω termination to V_{EE} or 100 Ω differential is provided. Check for termination inside of SerDes chip).
R2/3 = 150 Ω
R4/5 = Biasing for outputs depending on Serializer.
Place R1/4/5 close to SerDes chip.
Place R2/3 close to Infineon transceiver.
*) The inductors may be replaced by appropriate Ferrite beads.

File: 1392

Figure 17

2x5 AC/AC Transceiver



C1/2/3 = 4.7 ... 10 µF
C4/5/6 = Design criterion is the resonance frequency only. The self resonant frequency of the capacitor must be in the vicinity of the nominal data rate. Short traces are mandatory.
L1/2*) = 1 ... 4.7 µH
R1/2/3/4 = Depends on SerDes chip used, ensure proper 50 Ω termination to V_{EE} or 100 Ω differential is provided. Check for termination inside of SerDes chip.
R5/6 = Biasing (depends on SerDes chip).
Place R1/2/3/4/5/6 close to SerDes chip.

*) The inductors may be replaced by appropriate Ferrite beads.

File: 1393

Figure 18

Package Outlines

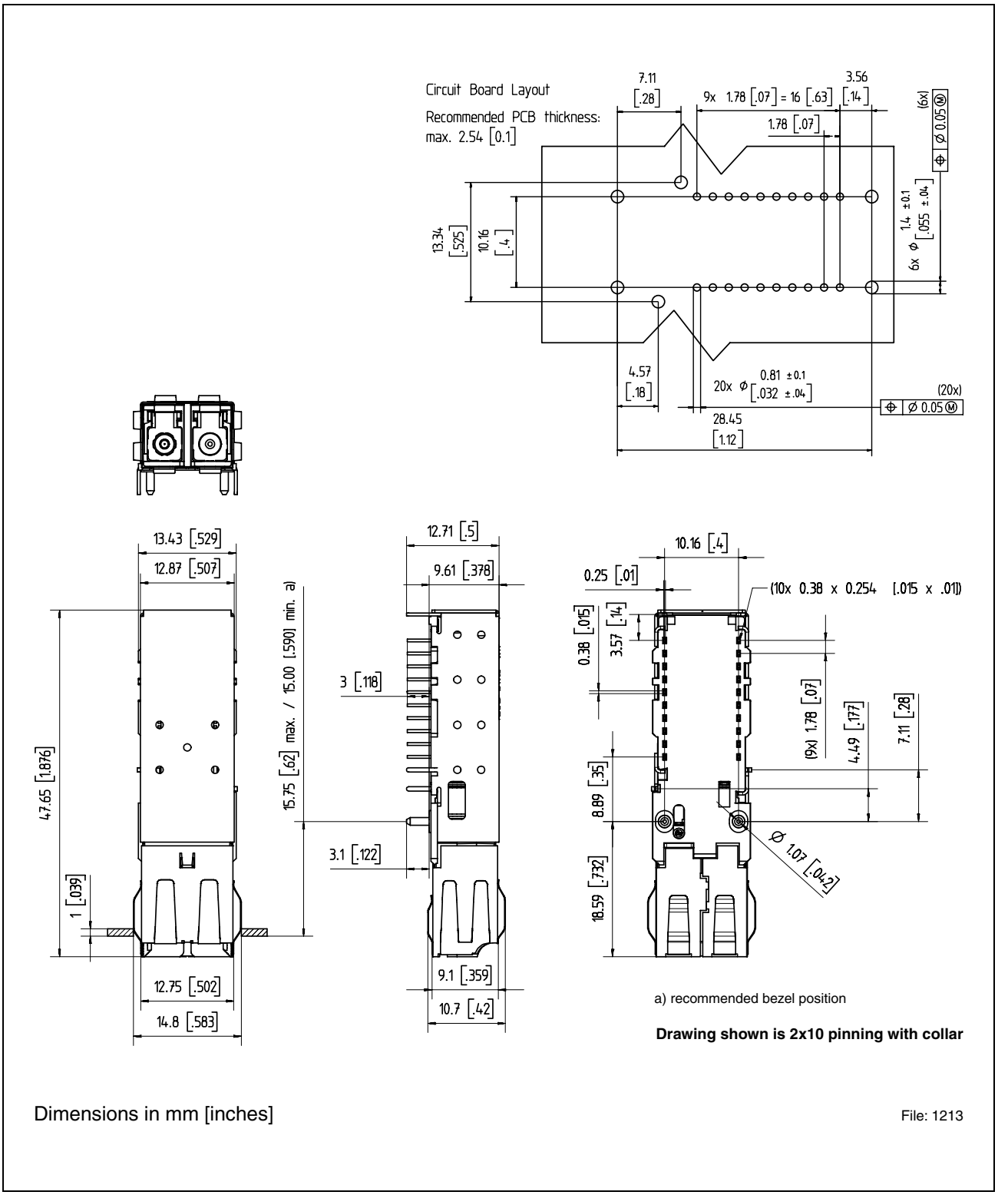
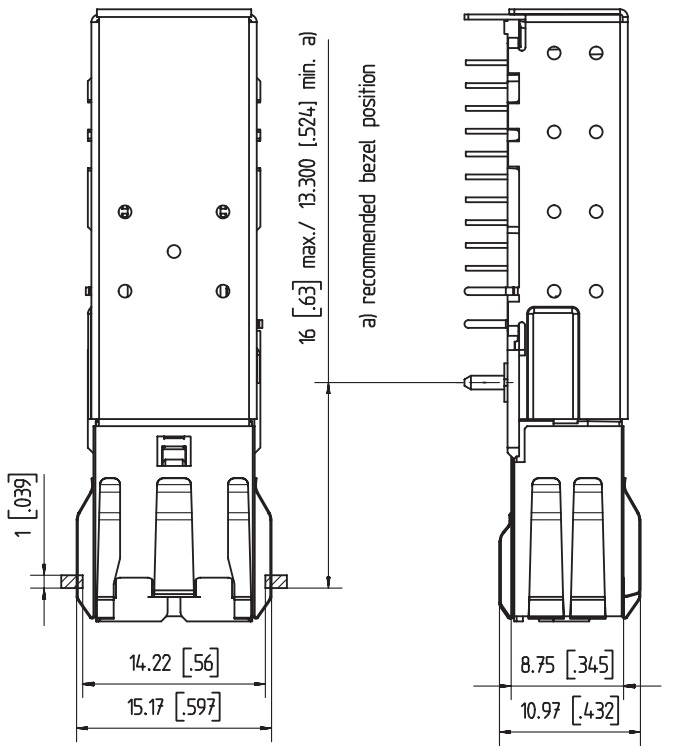


Figure 19

Advanced Collar



Dimensions in mm [inches]

File: 1505

Figure 20 Non-standard Collar

V23818-N15-Lxx/Lxxx

Revision History:	**2003-08-18**	DS1
Previous Version:	2003-03-10	

Page	**Subjects (major changes since last revision)**
	“Preliminary Data Sheet” deleted V23818-N15-L373, V23818-N15-L417, V23818-N15-L46WH deleted

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