calogic
CORPORATION

High Speed Buffer

CLM6121 / CLM6321

FEATURES

- **Slew Rate 1200V/μs**
- **Wide Bandwidth. 100MHz**
- **Output current 230mA**
- **High Input Impedance 2MΩ**
- **No Oscillations with Capacitive Loads**
- **5V to ±15V Operation Guaranteed**
- **Current and Thermal Limiting**
- **Fully Specified to Drive 50Ω Lines**

APPLICATIONS

- **Line Driving**
- **Radar**
- **Sonar**

GENERAL DESCRIPTION

The CLM6121 family are high speed unity gain buffers that slew at 1200V/μs, having a small signal bandwidth of 100MHz, and capable of providing a continuous output current of ±200mA. They are monolithic ICs which are pin to pin compatible with the LH0002H/CH with the additional feature of current limiting.

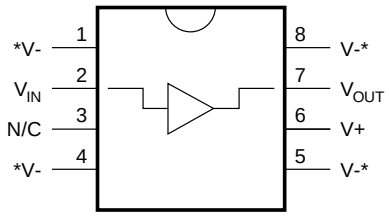
The internal output short circuit current limiting feature has been designed in the device such that when the junction temperature reaches 170°C, the current is limited to 100mA.

ORDERING INFORMATION

Part	Package	Temperature Range
CLM6121 H	Hermetic TO5 8 Lead	-55°C to 125°C
CLM6321 H	Hermetic TO5 8 Lead	-40°C to 85°C
CLM6121 N	Plastic P Dip 8 Lead	-40°C to 85°C
CLM6321 N	Plastic P Dip 8 Lead	-40°C to 85°C
CLM6121 M	SOIC 8 Lead	-25°C to 70°C
CLM6321 M	SOIC 8 Lead	-25°C to 70°C

CONNECTION DIAGRAMS

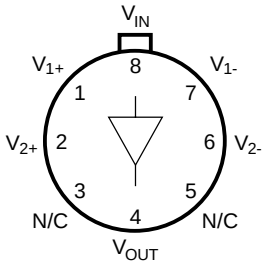
Plastic DIP



***Heat-sinking pins. Pin 1 and Pin 8 must be connected to the negative supply.**

Package NO8A

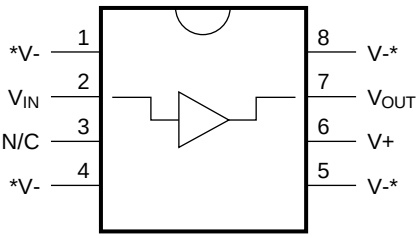
Metal Can



Top View

Package HO8A

Plastic SO



***Heat-sinking pins. Pin 1 and Pin 8 must be connected to the negative supply.**

Package MO8A

ABSOLUTE MAXIMUM RATINGS (Note 1)

If Military/Aerospace specified devices are required, please contact the Calogic Sales Office for availability and specifications.

Supply Voltage . . . . . ±18
Input Voltage . . . . . ±Vsupply
Short Circuit to GND (Note 2) . . . . . Continuous
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature
(Soldering 10 seconds) . . . . . 260°C

ESD Tolerance (Note 4) . . . . . ±2000V
Thermal Resistance (θ_{JA}) (Note 7)
H Package . . . . . 125°C/W
N Package . . . . . 50°C/W
M Package . . . . . 60°C/W
Thermal Resistance (θ_{JC})
H Package . . . . . 15°C/W

DC ELECTRICAL CHARACTERISTICS
The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100k\Omega$ and $R_S = 50\Omega$ unless otherwise noted.
Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

SYMBOL	CHARACTERISTICS	TYP	CLM6121 Limit (Note 6)	CLM6321 Limit (Note 6)	UNITS	CONDITIONS
A_{V1}	Voltage Gain 1	0.990	0.980 **0.970**	0.970 **0.950**	V/V Min	R_L = 1kΩ, V_{IN} = ±10V
A_{V2}	Voltage Gain 2	0.900	0.860 **0.800**	0.850 **0.820**		R_L = 50Ω, V_{IN} = ±10V
A_{V3}	Voltage Gain 3	0.840	0.780 **0.750**	0.750 **0.700**		R_L = 50Ω, V^+ = 5V $V_{IN} = 2V_{PP}$
V_{OS}	Offset Voltage	15	30 **50**	50 **100**	mV Max	R_L = 1kΩ
I_B	Input Bias Current	1	4 **7**	5 **7**	µA Max	R_L = 1kΩ, R_S = 10kΩ,
R_{IN}	Input Resistance	5			MΩ	R_L = 50Ω
C_{IN}	Input Capacitance	3.5			pF	
R_O	Output Resistance	3	5 **10**	5 **6**	Ω Max	I_{OUT} = ±10mA
I_{S1}	Supply Current 1	15	18 **20**	20 **22**	mA Max	$R_L = \infty$
I_{S2}	Supply Current 2	14	16 **18**	18 **20**		$R_L = \infty$, V^+ = 5V
V_{O1}	Output Swing 1	13.5	13.3 **13**	13.2 **13**	±V Min	R_L = 1k
V_{O2}	Output Swing 2	12.7	11.5 **10**	11 **10**		R_L = 100Ω
V_{O3}	Output Swing 3	12	11 **9**	10 **9**		R_L = 50Ω
V_{O4}	Output Swing 4	1.8	1.6 **1.3**	1.6 **1.5**	V_{PP} Min	R_L = 50Ω, V^+ = 5V (Note 6)
PSSR	Power Supply Rejection Ratio	70	60 **55**	60 **50**	dB Min	$V^{\pm}$ = ±5V to ±15V

AC ELECTRICAL CHARACTERISTICS

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25^oC$.

SYMBOL	CHARACTERISTICS	TYP	CLM6121	CLM6321	UNITS	CONDITIONS
			Limit (Note 6)	Limit (Note 6)		
SR_1	Slew Rate 1	1200	550	550	V/µs	V_{IN} = ±11V, R_L = 1kΩ
SR_2	Slew Rate 2	800	550	550	V/µs	V_{IN} = ±5V, R_L = 50Ω (Note 3)
SR_3	Slew Rate 3	650	550	550	V/µs	V_{IN} = 2 V_{PP}, R_L = 50Ω V^+ = 5V
BW	-3 dB Bandwidth	50	30	30	MHz	V_{IN} = ±100 mV_{PP}, R_L = 50Ω $C_L \leq$ 10pF
t_r, t_f	Rise Time Fall Time	7.0			ns	R_L = 50Ω, $C_L \leq$ 10pF V_O = 100mV_{PP}
t_{pd}	Propagation Delay Time	4.0			ns	R_L = 50Ω, $C_L \leq$ 10pF V_O = 100mV_{PP}
O_S	Overshoot	10			%	R_L = 50Ω, $C_L \leq$ 10pF V_O = 100mV_{PP}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: The CLM6121 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 3: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. For accurate measurements, the input slew rate should be at least 1700V/µs.

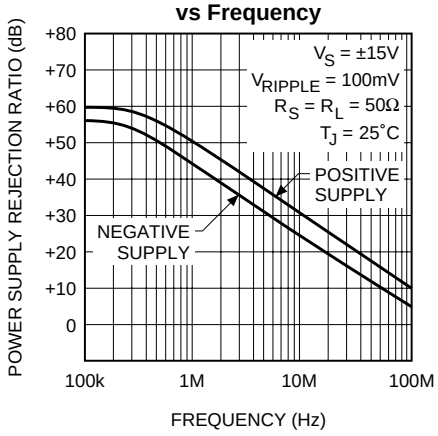
Note 4: The test circuit consists of the human body model of 120pF in series with 1500Ω.

Note 5: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

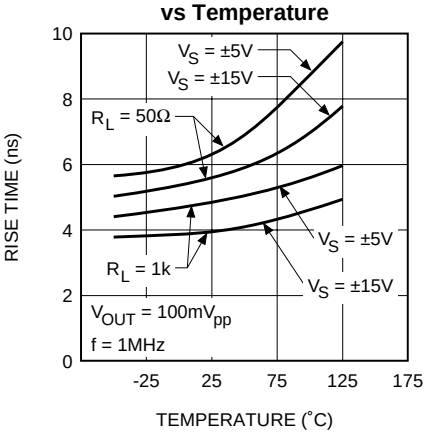
Note 6: Limits are guaranteed by testing, correlation or periodic characterization.

Note 7: For M & N package, θ_{JA} is measured by soldering the unit directly on a printed circuit board and V^- pins are connected to 2 square inches of 2 oz copper.

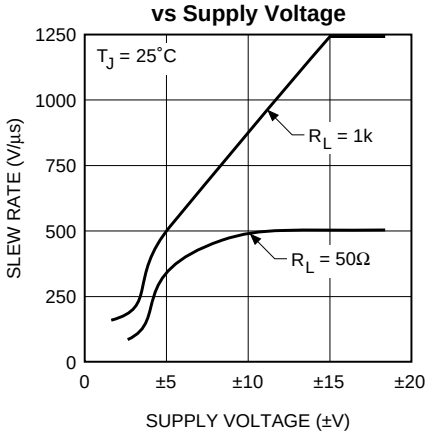
PSSR vs Frequency



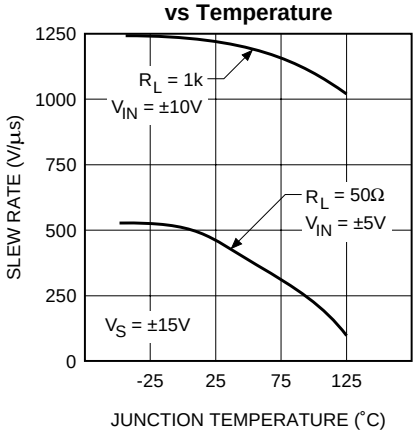
Rise Time vs Temperature



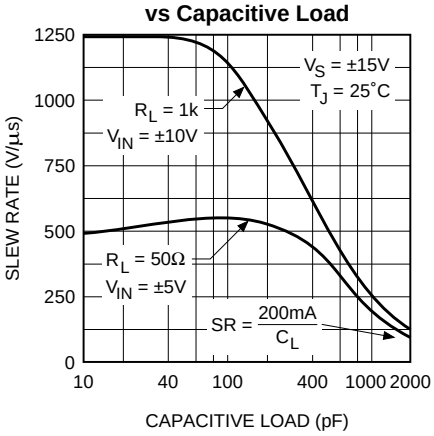
Slew Rate vs Supply Voltage



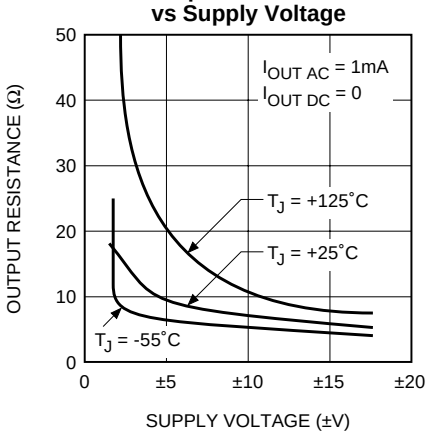
Slew Rate vs Temperature



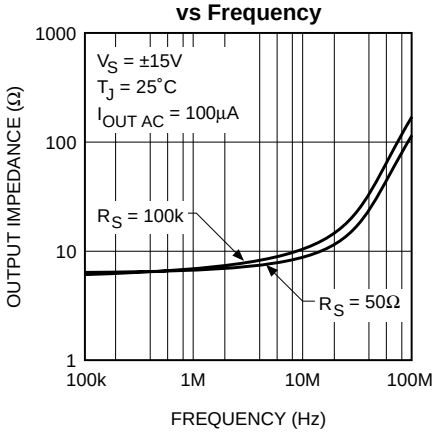
Slew Rate vs Capacitive Load



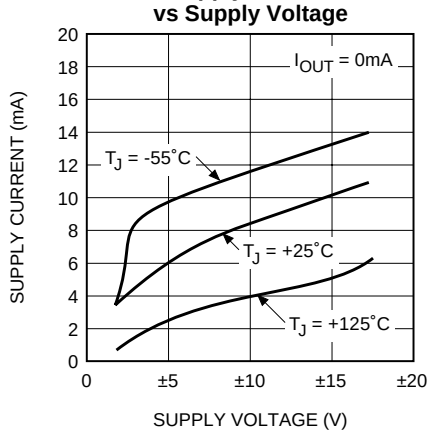
Output Resistance vs Supply Voltage



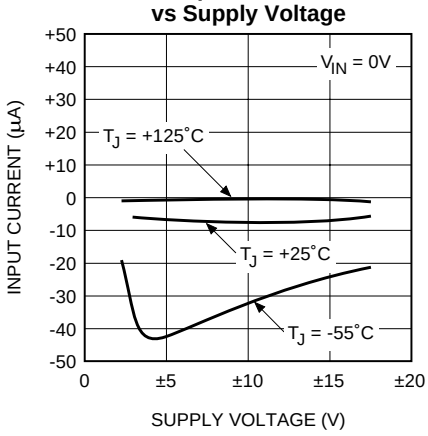
Output Impedance vs Frequency



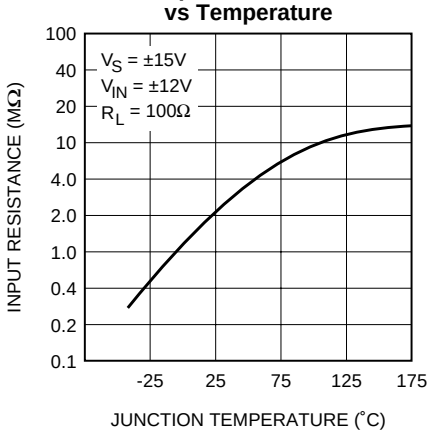
Supply Current vs Supply Voltage



Input Current vs Supply Voltage

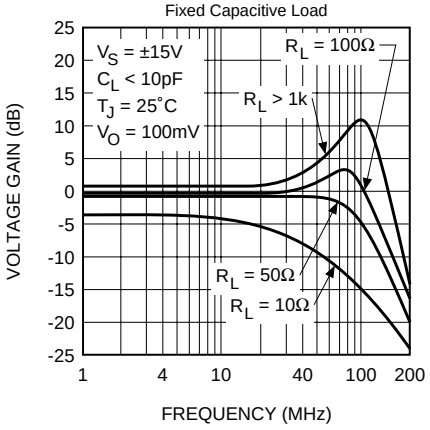


Input Resistance vs Temperature



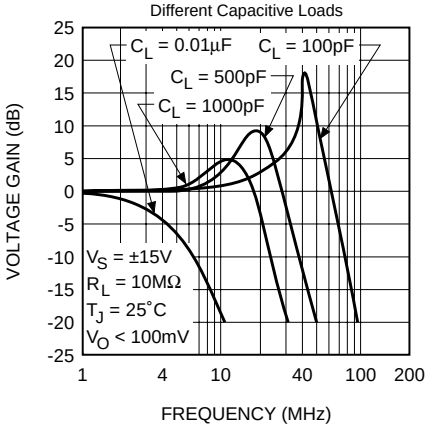
Voltage Gain vs Frequency

Different Resistive Loads - Fixed Capacitive Load



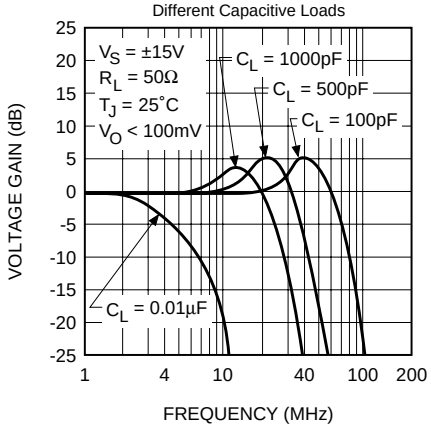
Voltage Gain vs Frequency

No Resistive Load - Different Capacitive Loads



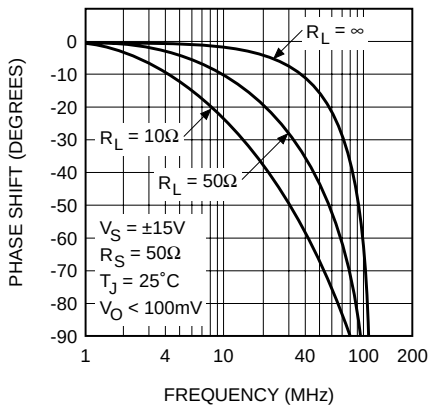
Voltage Gain vs Frequency

50Ω Resistive Load - Different Capacitive Loads



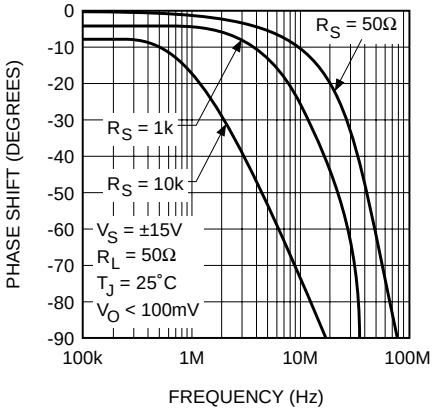
Phase Shift vs Frequency

Different Resistive Loads

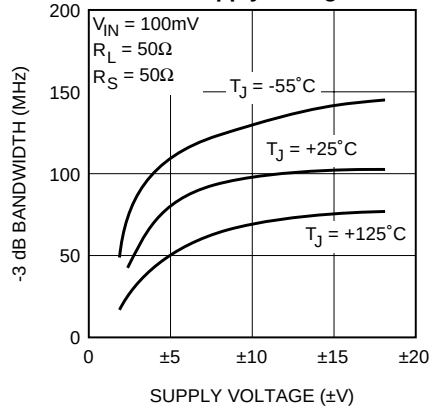


Phase Shift vs Frequency

Different Source Resisters



Small Signal Bandwidth vs Supply Voltage



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