ZL49010/1, ZL49020/1, ZL49030/1

Wide Dynamic Range DTMF Receiver

Data Sheet

September 2003

Features

- Wide dynamic range (50dB) DTMF Receiver
- Call progress (CP) detection via cadence indication
- 4-bit synchronous serial data output
- Software controlled guard time for ZL490x0
- Internal guard time circuitry for ZL490x1
- Powerdown option (ZL4901x & ZL4903x)
- 3.579MHz crystal or ceramic resonator (ZL4903x and ZL4902x)
- External clock input (ZL4901x)
- Guarantees non-detection of spurious tones

Applications

- Integrated telephone answering machine
- End-to-end signalling
- Fax Machines

Ordering Information

ZL49010DAA	8 Pin PDIP	Tubes
ZL49011DAA	8 Pin PDIP	Tubes
ZL49020DAA	8 Pin PDIP	Tubes
ZL49021DAA	8 Pin PDIP	Tubes
ZL49030DCA	18 Pin SOIC	Tubes
ZL49030DCB	18 Pin SOIC	Tape & Reel
ZL49030DDA	20 Pin SSOP	Tubes
ZL49030DDB	20 Pin SSOP	Tape & Reel
ZL49031DCA	18 Pin SOIC	Tubes
ZL49031DCB	18 Pin SOIC	Tape & Reel
ZL49031DDA	20 Pin SSOP	Tubes
ZL49031DDB	20 Pin SSOP	Tape & Reel

-40°C to +85°C

Description

The ZL490xx is a family of high performance DTMF receivers which decode all 16 tone pairs into a 4-bit binary code. These devices incorporate an AGC for wide dynamic range and are suitable for end-to-end signalling. The ZL490x0 provides an early steering (ESt) logic output to indicate the detection of a DTMF signal and requires external software guard time to validate the DTMF digit. The ZL490x1, with preset internal guard times, uses a delay steering (DStD) logic output to indicate the detection of a valid DTMF digit. The 4-bit DTMF binary digit can be clocked out synchronously at the serial data (SD) output. The SD pin is multiplexed with call progress detector output. In the presence of supervisory tones, the call progress

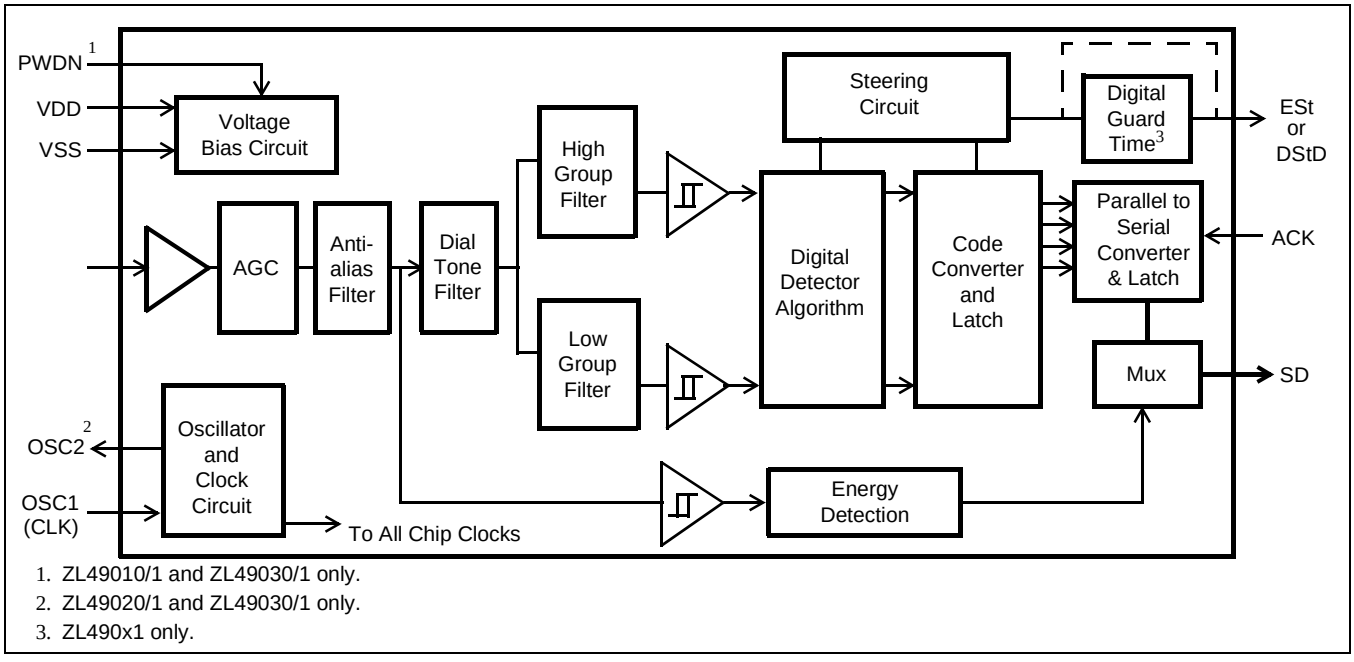


Figure 1 - Functional Block Diagram

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detector circuit indicates the cadence (i.e., envelope) of the tone burst. The cadence information can then be processed by an external microcontroller to identify specific call progress signals. The ZL4902x and ZL4903x can be used with a crystal or a ceramic resonator without additional components. A power-down option is provided for the ZL4901x and ZL4903x.

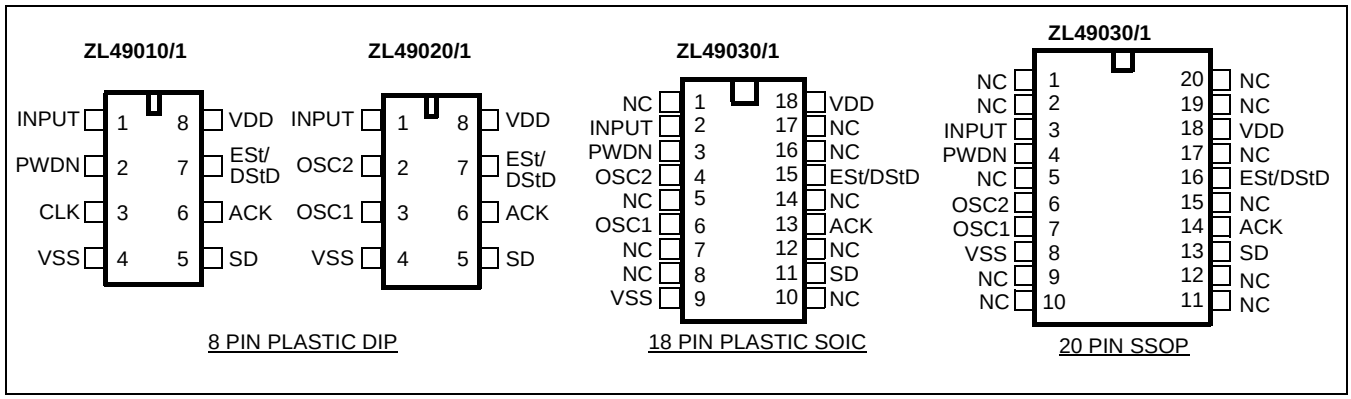


Figure 2 - Pin Connections

Pin Description

Pin #			Name	Description
4903x	**4902x**	**4901x**		
2	1	1	INPUT	**DTMF/CP Input.** Input signal must be AC coupled via capacitor.
4	2	-	OSC2	**Oscillator Output.**
6	3	3	OSC1 (CLK)	**Oscillator/Clock Input.** This pin can either be driven by: 1) an external digital clock with defined input logic levels. OSC2 should be left open. 2) connecting a crystal or ceramic resonator between OSC1 and OSC2 pins.
9	4	4	V_{SS}	**Ground.** (0V)
11	5	5	SD	**Serial Data/Call Progress Output.** This pin serves the dual function of being the serial data output when clock pulses are applied after validation of DTMF signal, and also indicates the cadence of call progress input. As DTMF signal lies in the same frequency band as call progress signal, this pin may toggle for DTMF input. The SD pin is at logic low in powerdown state.
13	6	6	ACK	**Acknowledge Pulse Input.** After ESt or DStD is high, applying a sequence of four pulses on this pin will then shift out four bits on the SD pin, representing the decoded DTMF digit. The rising edge of the first clock is used to latch the 4-bit data prior to shifting. This pin is pulled down internally. The idle state of the ACK signal should be low.
15	7	7	ESt (ZL490x0) DStD (ZL490x1)	**Early Steering Output.** A logic high on ESt indicates that a DTMF signal is present. ESt is at logic low in powerdown state. **Delayed Steering Output.** A logic high on DStD indicates that a valid DTMF digit has been detected. DStD is at logic low in powerdown state.

Pin Description (continued)

Pin #			Name	Description
4903x	4902x	4901x		
18	8	8	V_{DD}	**Positive Power Supply (5V Typ.)** Performance of the device can be optimized by minimizing noise on the supply rails. Decoupling capacitors across V_{DD} and V_{SS} are therefore recommended.
1,5,7,8, 10, 12, 14,16, 17	-	-	NC	**No Connection.** Pin is unconnected internally.
3	-	2	PWDN	**Power Down Input.** A logic high on this pin will power down the device to reduce power consumption. This pin is pulled down internally and can be left open if not used. ACK pin should be at logic '0' to power down device.

Device Type	8 Pin	18 Pin	20 Pin	PWDN	2 Pin OSC	Ext CLK	ESt	DStD
ZL49010	x			x		x	x	
ZL49011	x			x		x		x
ZL49020	x				x	x	x	
ZL49021	x				x	x		x
ZL49030		x	x	x	x	x	x	
ZL49031		x	x	x	x	x		x

Table 1 - Summary of ZL490x0/1 Product Family

Functional Description

The ZL490xxs are high performance and low power consumption DTMF receivers. These devices provide wide dynamic range DTMF detection and a serial decoded data output. These devices also incorporate an energy detection circuit. An input voiceband signal is applied to the devices via a series decoupling capacitor. Following the unity gain buffering, the signal enters the AGC circuit followed by an anti-aliasing filter. The bandlimited output is routed to a dial tone filter stage and to the input of the energy detection circuit. A bandsplit filter is then used to separate the input DTMF signal into high and low group tones. The high group and low group tones are then verified and decoded by the internal frequency counting and DTMF detection circuitry. Following the detection stage, the valid DTMF digit is translated to a 4-bit binary code (via an internal look-up ROM). Data bits can then be shifted out serially by applying external clock pulses.

Automatic Gain Control (AGC) Circuit

As the device operates on a single power supply, the input signal is biased internally at approximately VDD/2. With large input signal amplitude (between 0 and approximately -30dBm for each tone of the composite signal), the AGC is activated to prevent the input signal from being clipped. At low input level, the AGC remains inactive and the input signal is passed directly to the hardware DTMF detection algorithm and to the energy detection circuit.

Filter and Decoder Section

The signal entering the DTMF detection circuitry is filtered by a notch filter at 350 and 440 Hz for dial tone rejection. The composite dual-tone signal is further split into its individual high and low frequency components by two 6^{th} order switched capacitor bandpass filters. The high group and low group tones are then smoothed by separate

output filters and squared by high gain limiting comparators. The resulting squarewave signals are applied to a digital detection circuit where an averaging algorithm is employed to determine the valid DTMF signal. For ZL490x0, upon recognition of a valid frequency from each tone group, the early steering (ESt) output will go high, indicating that a DTMF tone has been detected. Any subsequent loss of DTMF signal condition will cause the ESt pin to go low. For ZL490x1, an internal delayed steering counter validates the early steering signal after a predetermined guard time which requires no external components. The delayed steering (DStD) will go high only when the validation period has elapsed. Once the DStD output is high, the subsequent loss of early steering signal due to DTMF signal dropout will activate the internal counter for a validation of tone absent guard time. The DStD output will go low only after this validation period.

Energy Detection

The output signal from the AGC circuit is also applied to the energy detection circuit. The detection circuit consists of a threshold comparator and an active integrator. When the signal level is above the threshold of the internal comparator (-35dBm), the energy detector produces an energy present indication on the SD output. The integrator ensure the SD output will remain at high even though the input signal is changing. When the input signal is removed, the SD output will go low following the integrator decay time. Short decay time enables the signal envelope (or cadence) to be generated at the SD output. An external microcontroller can monitor this output for specific call progress signals. Since presence of speech and DTMF signals (above the threshold limit) can cause the SD output to toggle, both ESt (DStD) and SD outputs should be monitored to ensure correct signal identification. As the energy detector is multiplexed with the digital serial data output at the SD pin, the detector output is selected at all times except during the time between the rising edge of the first pulse and the falling edge of the fourth pulse applied at the ACK pin.

Serial Data (SD) Output

When a valid DTMF signal burst is present, ESt or DStD will go high. The application of four clock pulses on the ACK pin will provide a 4-bit serial binary code representing the decoded DTMF digit on the SD pin output. The rising edge of the first pulse applied on the ACK pin latches and shifts the least significant bit of the decoded digit on the SD pin. The next three pulses on ACK pin will shift the remaining latched bits in a serial format (see Figure 5). If less than four pulses are applied to the ACK pin, new data cannot be latched even though ESt/DStD can be valid. Clock pulses should be applied to clock out any remaining data bits to resume normal operation. Any transitions in excess of four pulses will be ignored until the next rising edge of the ESt/DStD. ACK should idle at logic low. The 4-bit binary representing all 16 standard DTMF digits are shown in Table .

Powerdown Mode (ZL4901x/4903x)

The ZL4901x/4903x devices offer a powerdown function to preserve power consumption when the device is not in use. A logic high can be applied at the PWDN pin to place the device in powerdown mode. The ACK pin should be kept at logic low to avoid undefined ESt/DStD and SD outputs (see Table 3).

F_{LOW}	F_{HIGH}	DIGIT	b_3	b_2	b_1	b_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1

Table 2 - Serial Decode Bit Table

F_{LOW}	F_{HIGH}	DIGIT	b_3	b_2	b_1	b_0
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0
0= LOGIC LOW, 1= LOGIC HIGH Note: b0=LSB of decoded DTMF digit and shifted out first.						

Table 2 - Serial Decode Bit Table (continued)

ACK (input)	PWDN (input)	ESt/DStD (output)	SD (output)	ZL4901x/4903x status
low	low	Refer to Fig. 4 for timing waveforms	Refer to Fig. 4 for timing waveforms	normal operation
low	high^{+}	low	low	powerdown mode
high	low	low	undefined	undefined
high	high	undefined	undefined	undefined
Note: $^{+}$ =enters powerdown mode on the rising edge.				

Table 3 - Powerdown Mode

Frequency 1 (Hz)	Frequency 2 (Hz)	On/Off	Description
350	440	continuous	North American Dial Tones
425	---	continuous	European Dial Tones
400	---	continuous	Far East Dial Tones
480	620	0.5s/0.5s	North American Line Busy
440	---	0.5s/0.5s	Japanese Line Busy
480	620	0.25s/0.25s	North American Reorder Tones
440	480	2.0s/4.0s	North American Audible Ringing
480	620	0.25s/0.25s	North American Reorder Tones

Table 4 - Call Progress Tones

Oscillator

The ZL4902x/4903x can be used in both external clock or two pin oscillator mode. In two pin oscillator mode, the oscillator circuit is completed by connecting either a 3.579MHz crystal or ceramic resonator across OSC1 and OSC2 pins. It is also possible to configure a number of these devices (4 maximum) employing only a single oscillator crystal. The OSC2 output of the first device in the chain is connected to the OSC1 input of the next device. Subsequent devices are connected similarily. The oscillator circuit can also be driven by an 3.579MHz external clock applied on pin OSC 1. The OSC2 pin should be left open.

For ZL4901x devices, the CLK input is driven directly by an 3.579MHz external digital clock.

Applications

The circuit shown in Figure 3 illustrates the use of a ZL4902x in a typical receiver application. It requires only a coupling capacitor (C1) and a crystal or ceramic resonator (X1) to complete the circuit.

The ZL490x0 is designed for user who wishes to tailor the guard time for specific applications. When a DTMF signal is present, the ESt pin will go high. An external microcontroller monitors ESt in real time for a period of time set by the user. A guard time algorithm must be implemented such that DTMF signals not meeting the timing requirements are rejected. The ZL490x1 uses an internal counter to provide a preset DTMF validation period. It requires no external components. The DStD output high indicates that a valid DTMF digit has been detected.

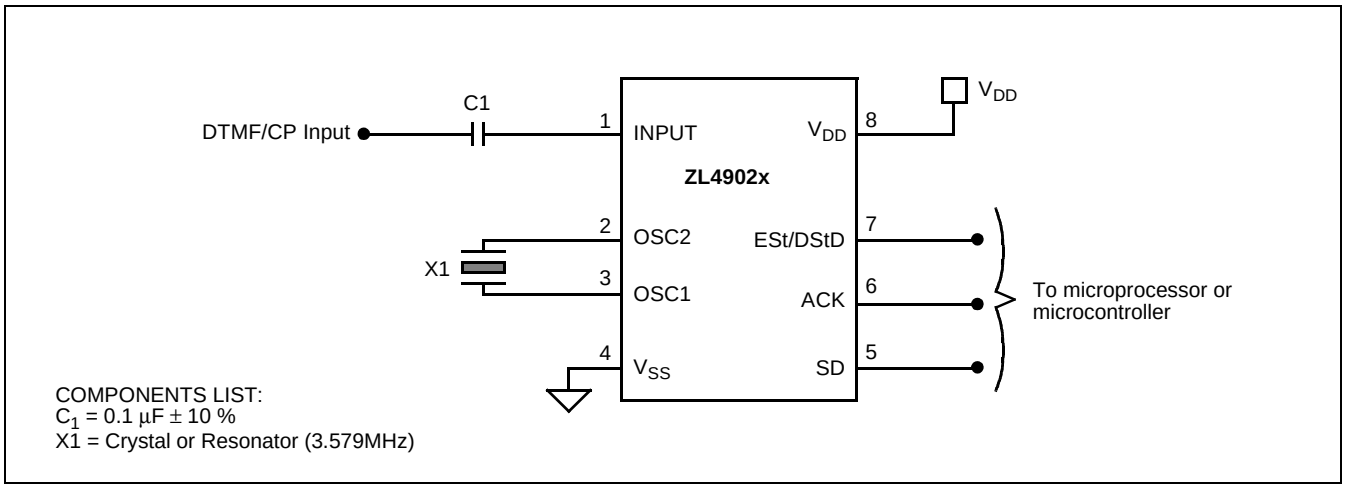


Figure 3 - Application Circuit for ZL4902x

Absolute Maximum Ratings† - Voltages are with respect to V_{SS}=0V unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V_{DD}-V_{SS}		6	V
2	Voltage on any pin (other than supply)	$V_{I/O}$	-0.3	6.3	V
3	Current at any pin (other than supply)	$I_{I/O}$		10	mA
4	Storage temperature	T_S	-65	150	°C
5	Package power dissipation	P_D		500	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS}=0V unless otherwise stated

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive Power Supply	V_{DD}	4.75	5.0	5.25	V	
2	Oscillator Clock Frequency	f_{OSC}		3.579		MHz	
3	Oscillator Frequency Tolerance	Δf_{OSC}			±0.1	%	
4	Operating Temperature	T_d	-40	25	85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to V_{DD}=5V±5%,V_{SS}=0V, and temperature -40 to 85°C, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating supply current	I_{DD}		3	8	mA	
2	Standby supply current	I_{DDQ}		30	100	µA	PWDN=5V, ACK=0V ESt/DStD = SD = 0V
3a	Input logic 1	V_{IH}	4.0			V	
3b	Input logic 1 (for OSC1 input only)	V_{IH}	3.5			V	ZL4902x/ZL4903x
4a	Input logic 0	V_{IL}			1.0	V	
4b	Input logic 0 (for OSC1 input only)	V_{IL}			1.5	V	ZL4902x/ZL4903x
5	Input impedance (pin 1)	R_{IN}	50			kΩ	
6	Pull-down Current (PWDN, ACK pins)	I_{PD}		25		µA	with internal pull-down resistor of approx. 200kΩ. PWDN/ACK = 5V
7	Output high (source) current	I_{OH}	0.4	4.0		mA	V_{OUT}=V_{DD}-0.4V
8	Output low (sink) current	I_{OL}	1.0	9.0		mA	V_{OUT}=V_{SS}+0.4V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

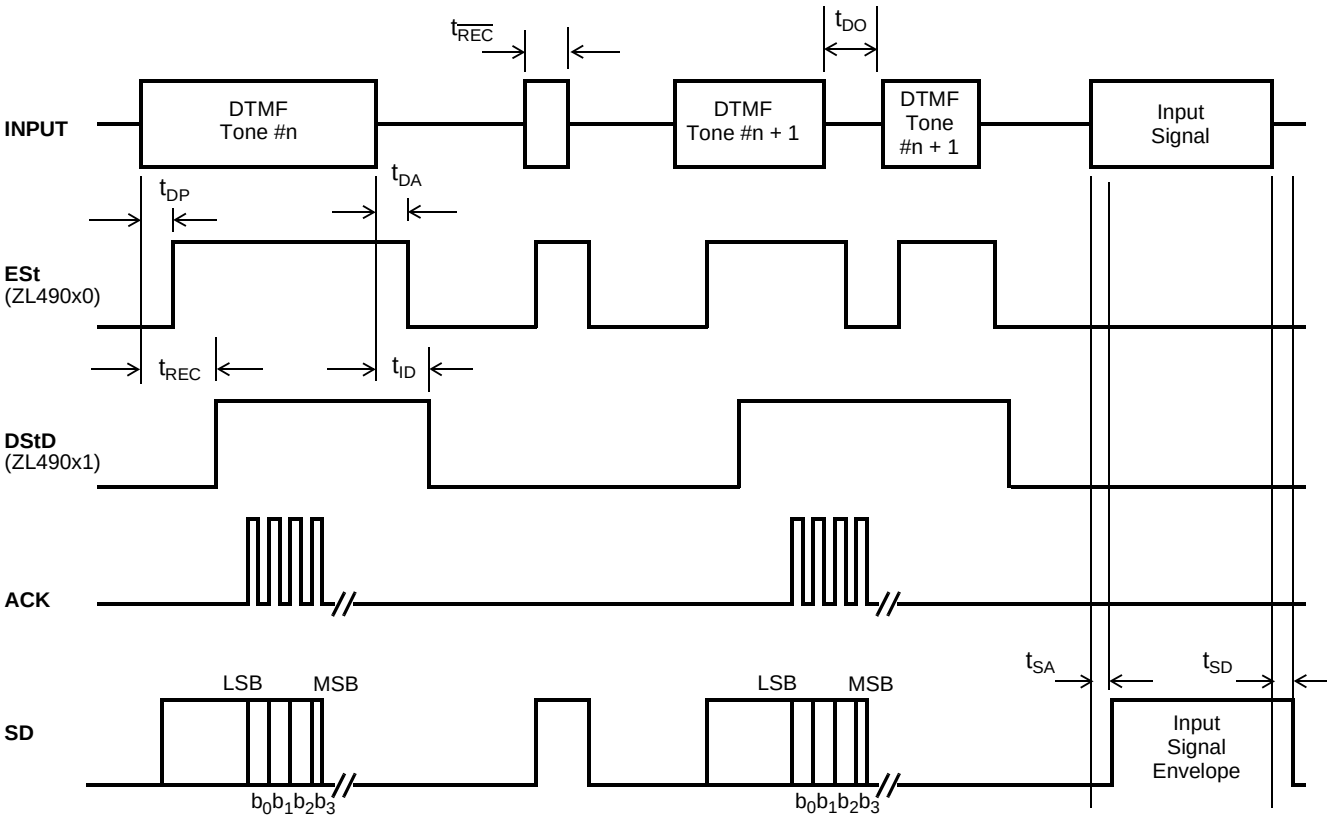
AC Electrical Characteristics - voltages are with respect to V_{DD}=5V±5%, V_{SS}=0V and temperature -40 to +85°C unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions*
1	Valid input signal level (each tone of composite signal)		-50 2.45		0 775	dBm mV_{RMS}	1,2,3,5,6,12
2	Positive twist accept				8	dB	1,2,3,4,11,12,15
3	Negative twist accept				8	dB	1,2,3,4,11,12,15
4	Frequency deviation accept		±1.5%± 2Hz				1,2,3,5,12
5	Frequency deviation reject		±3.5%				1,2,3,5,12,15
6	Third tone tolerance			-16		dB	1,2,3,4,5,12
7	Noise tolerance			-12		dB	7,9,12
8	Dial tone tolerance			+15		dB	8,10,12
9	Supervisory tones detect level (Total power)		-35			dBm	16
10	Supervisory tones reject level				-50	dBm	16
11	Energy detector attack time	t_{SA}		1.0	6.5	ms	16
12	Energy detector decay time	t_{SD}	3		25	ms	16
13a 13b	Powerdown time Powerup time				10 30 50	ms ms ms	IDDQ ≤ 100µA ZL49010/ZL49030 ZL49011/ZL49031 Note 14
14	Tone present detect time (ESt logic output)	t_{DP}	3	13	20	ms	ZL490x0
15	Tone absent detect time (ESt logic output)	t_{DA}		3	15	ms	ZL490x0
16	Tone duration accept (DStD logic output)	t_{REC}			40	ms	ZL490x1
17	Tone duration reject (DStD logic output)	$t_{\overline{REC}}$	20			ms	ZL490x1
18	Interdigit pause accept (DStD logic output)	t_{ID}			40	ms	ZL490x1
19	Interdigit pause reject (DStD logic output)	t_{DO}	20			ms	ZL490x1
20	Data shift rate 40-60% duty cycle	f_{ACK}		1.0	3.0	MHz	13,15
21	Propagation delay (ACK to Data Bit)	t_{PAD}		100	140	ns	1MHz $f_{ACK,}$ 13,15
22	Data hold time (ACK to SD)	t_{DH}	30	50		ns	13,15

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing

*** Test Conditions**

1. dBm refers to a reference power of 1 mW delivered into a 600 ohms load.
2. Data sequence consists of all DTMF digits.
3. Tone on = 40 ms, tone off = 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5%± 2 Hz.
7. Bandwidth limited (0-3 kHz) Gaussian noise.
8. Precise dial tone frequencies are 350 Hz and 440 Hz (± 2%).
9. Referenced to lowest level frequency component in DTMF signal.
10. Referenced to the minimum valid accept level.
11. Both tones must be within valid input signal range.
12. Internal guard time for ZL490x1 = 20ms.
13. Timing parameters are measured with 70pF load at SD output.
14. Time duration between PWDN pin changes from '1' to '0' and ESt/DStD becomes active.
15. Guaranteed by design and characterization. Not subject to production testing.
16. Value measured with an applied tone of 450 Hz.



t_{DO} - maximum allowable dropout during valid DTMF signals. ZL490xx).
t_{ID} - minimum time between valid DTMF signals (ZL49011).
$t_{\overline{REC}}$ - maximum DTMF signal duration not detected as valid (ZL490xx).
t_{REC} - minimum DTMF signal duration required for valid recognition (ZL490x1).
t_{DA} - time to detect the absence of valid DTMF signals (ZL490x0).
t_{DP} - time to detect the presence of valid DTMF signals (ZL490x0).
t_{SA} - supervisory tone integrator attack time (ZL490xx).
t_{SD} - supervisory tone integrator decay time (ZL490xx).

Figure 4 - Timing Diagram

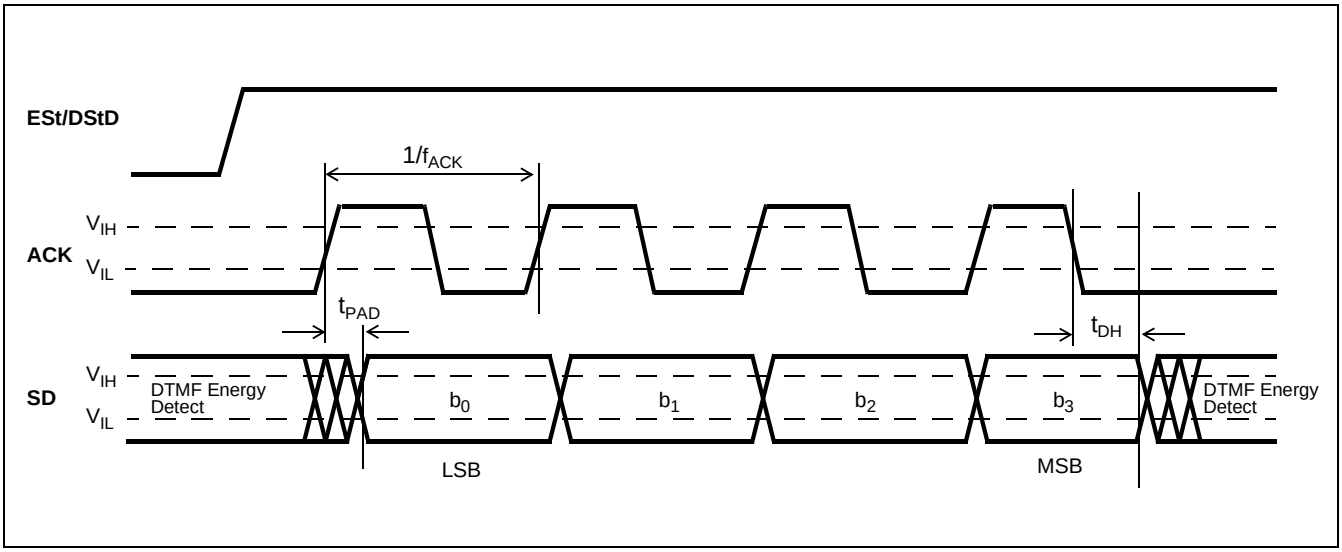
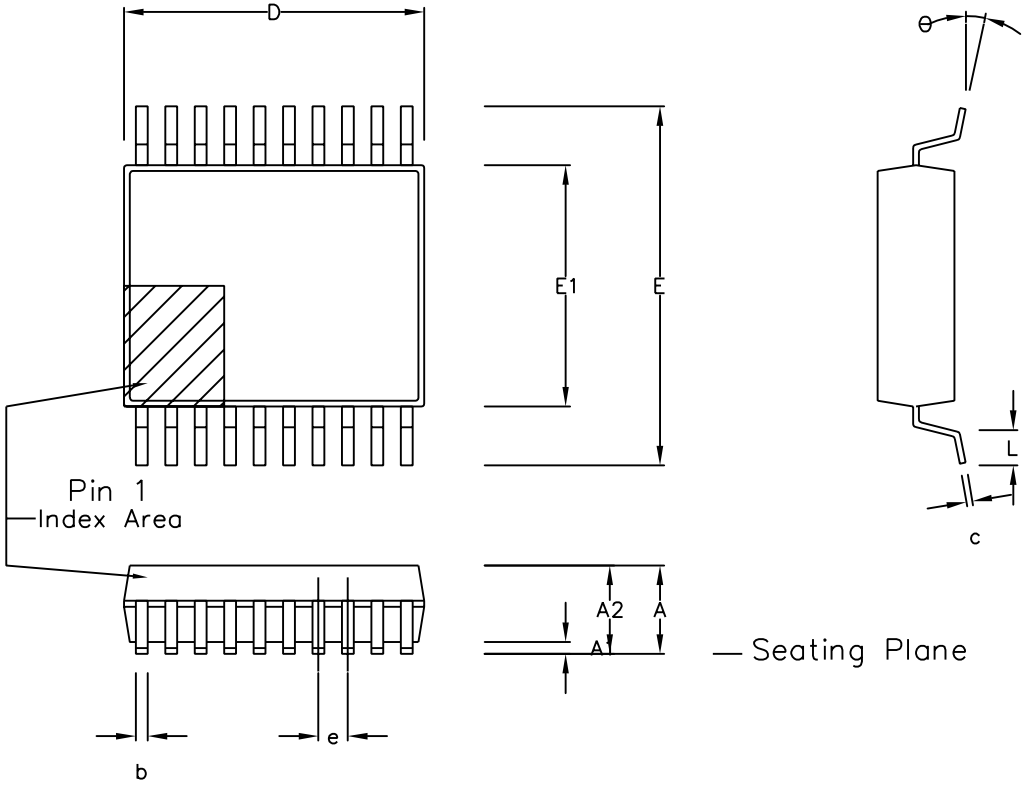


Figure 5 - ACK to SD Timing



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	6.90		7.50		0.272		0.295
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	20						
Conforms to JEDEC MO-150 AE Iss. B							

This drawing supersedes:-
418/ED/51481/002 (Swindon/Plymouth)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

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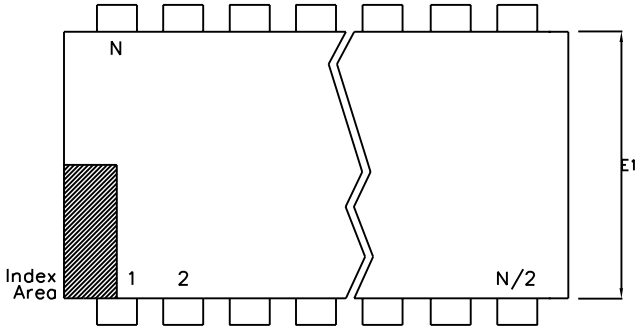
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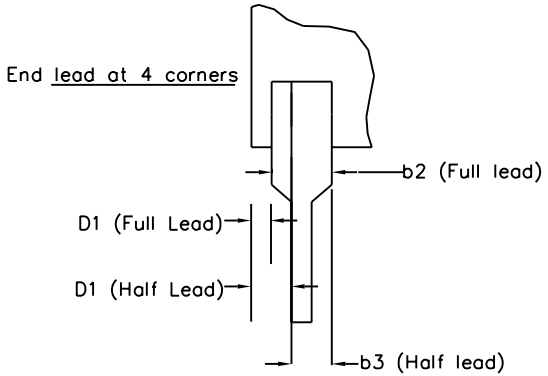
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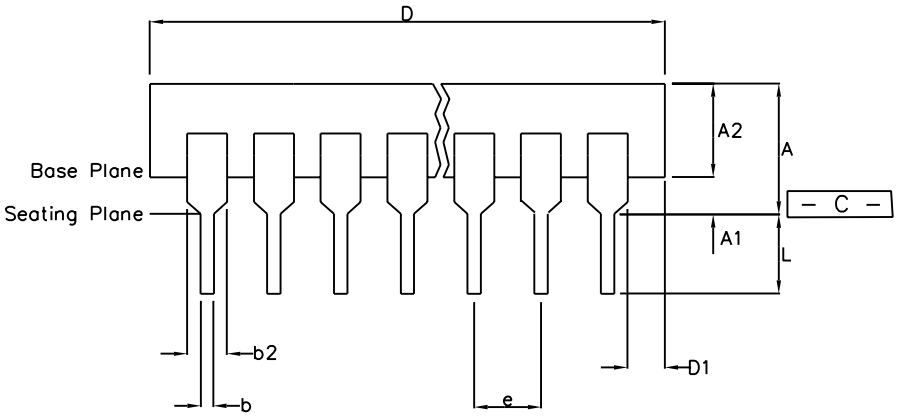
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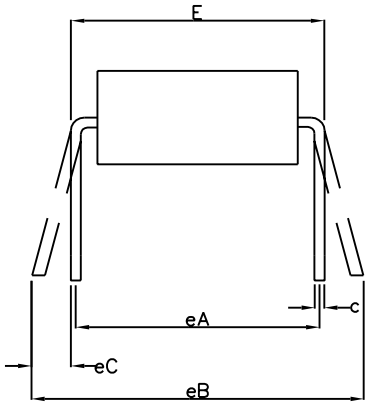
Package Outline for 20 lead SSOP (5.3mm Body Width)

GPD00294









	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	0.76	1.14	0.030	0.045
c	0.20	0.36	0.008	0.014
D	9.02	10.16	0.355	0.400
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	8		8	
Conforms to Jedec MS-001BA Issue D				

Notes:
1. Dimensions D, D1 & E1 do not include mould flash or protrusions.
2. Dimensions E & eA are measured with leads constrained to be perpendicular to datum – C –
3. Dimensions eB & eC are measured with the leads unconstrained
4. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
5. N is the maximum of terminal positions.

This drawing supersedes: –
UK drawing # 418/ED/39502/001

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ISSUE	1	2		
ACN	202540	213105		
DATE	23May97	15Jul02		
APPRD.				

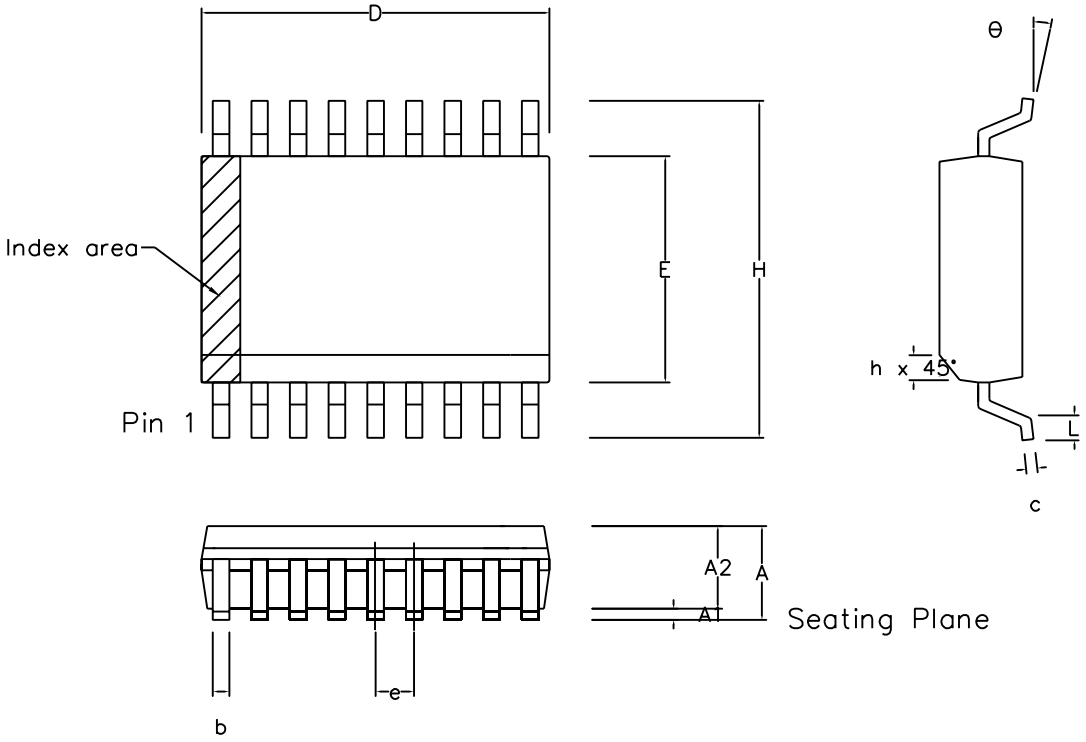
ZARLINK SEMICONDUCTOR

Previous package codes
DP / E

Package Code DA

Package Outline for 8 lead PDIP

GPD00345



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	11.35		11.75		0.447		0.463
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	18						
Conforms to JEDEC MS-013AB Iss. C							

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in millimeters
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 18 lead SOIC (0.300" Body Width)

GPD00014



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