

# DATA SHEET

**BF904WR**

N-channel dual-gate MOS-FET

Product specification  
Supersedes data of 1995 Apr 25

2010 Sep 15



N-channel dual-gate MOS-FET

BF904WR

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

DESCRIPTION

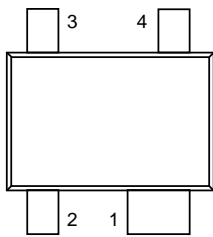
Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION

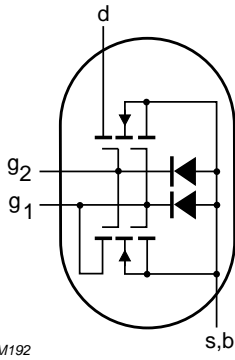
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g <sub>2</sub>	gate 2
4	g <sub>1</sub>	gate 1



Top view



MAM192

Marking code: MC\*

\* = - : made in Hong Kong  
\* = p : made in Hong Kong  
\* = t : made in Malaysia

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage		–	–	7	V
I <sub>D</sub>	drain current		–	–	30	mA
P <sub>tot</sub>	total power dissipation		–	–	280	mW
T <sub>j</sub>	operating junction temperature		–	–	150	°C
y <sub>fs</sub>	forward transfer admittance		22	25	30	mS
C <sub>ig1-s</sub>	input capacitance at gate 1		–	2.2	2.6	pF
C <sub>rs</sub>	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	7	V
$I_D$	drain current		–	30	mA
$I_{G1}$	gate 1 current		–	$\pm 10$	mA
$I_{G2}$	gate 2 current		–	$\pm 10$	mA
$P_{tot}$	total power dissipation	up to $T_{amb} = 50\text{ }^{\circ}\text{C}$ ; see Fig.2; note 1	–	280	mW
$T_{stg}$	storage temperature		–65	+150	$^{\circ}\text{C}$
$T_j$	operating junction temperature		–	+150	$^{\circ}\text{C}$

## Note

1. Device mounted on a printed-circuit board.

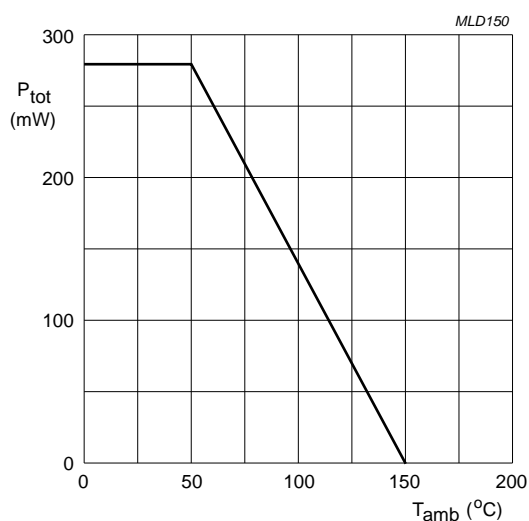


Fig.2 Power derating curve.

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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point	$T_s = 91\ ^\circ\text{C}$ ; note 2	210	K/W

## Notes

1. Device mounted on a printed-circuit board.
2.  $T_s$  is the temperature at the soldering point of the source lead.

## STATIC CHARACTERISTICS

 $T_j = 25\ ^\circ\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{G1-S} = 10\ \text{mA}$	6	15	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{G2-S} = 10\ \text{mA}$	6	15	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{S-G1} = 10\ \text{mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{S-G2} = 10\ \text{mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\ \text{V}$ ; $V_{DS} = 5\ \text{V}$ ; $I_D = 20\ \mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5\ \text{V}$ ; $I_D = 20\ \mu\text{A}$	0.3	1.2	V
$I_{DSX}$	drain-source current	$V_{G2-S} = 4\ \text{V}$ ; $V_{DS} = 5\ \text{V}$ ; $R_{G1} = 120\ \text{k}\Omega$ ; note 1	8	13	mA
$I_{G1-SS}$	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$ ; $V_{G1-S} = 5\ \text{V}$	—	50	nA
$I_{G2-SS}$	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$ ; $V_{G2-S} = 5\ \text{V}$	—	50	nA

## Note

1.  $R_G$  connects gate 1 to  $V_{GG} = 5\ \text{V}$ .

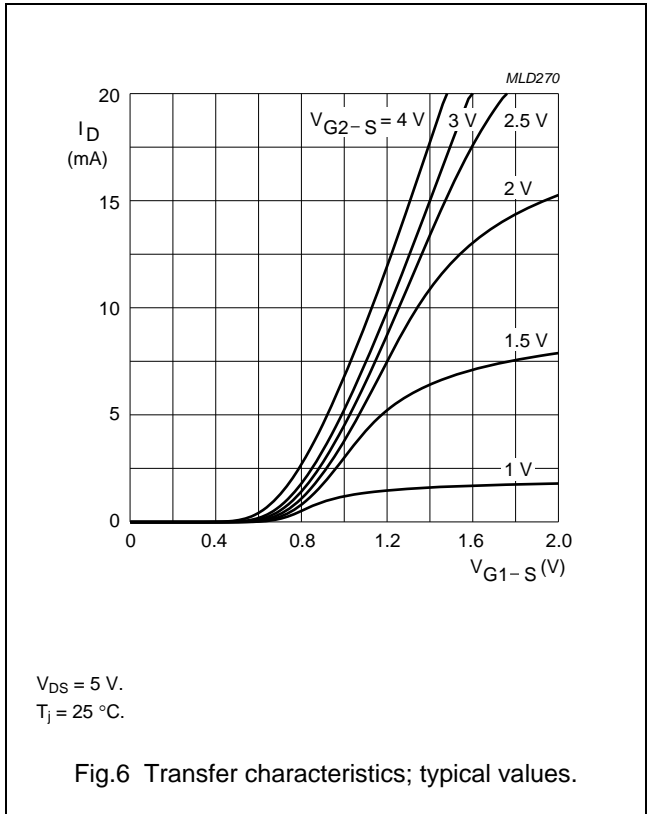
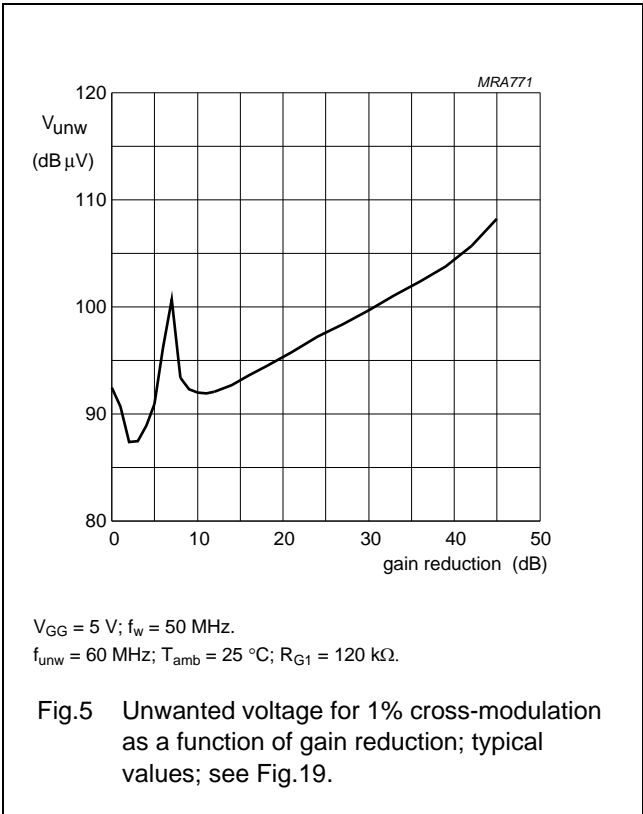
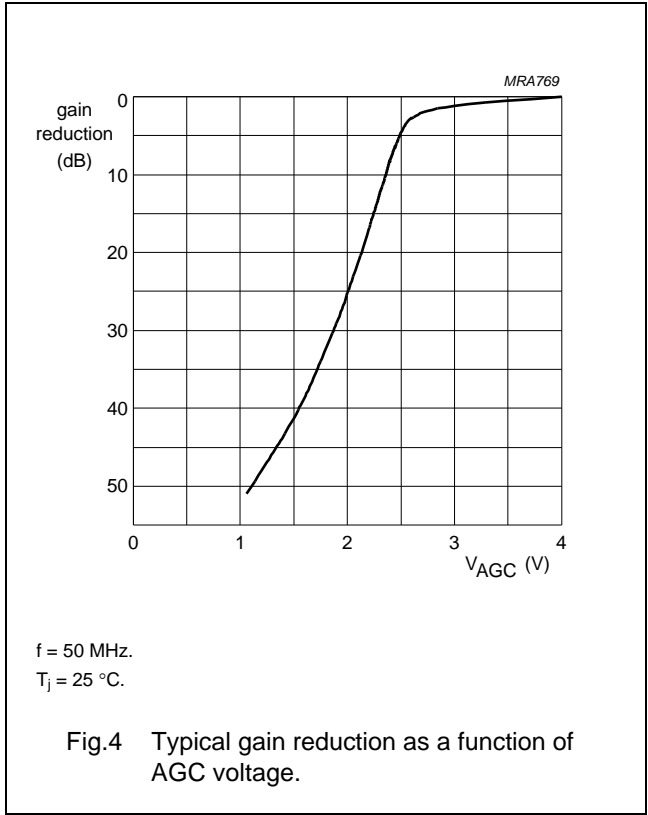
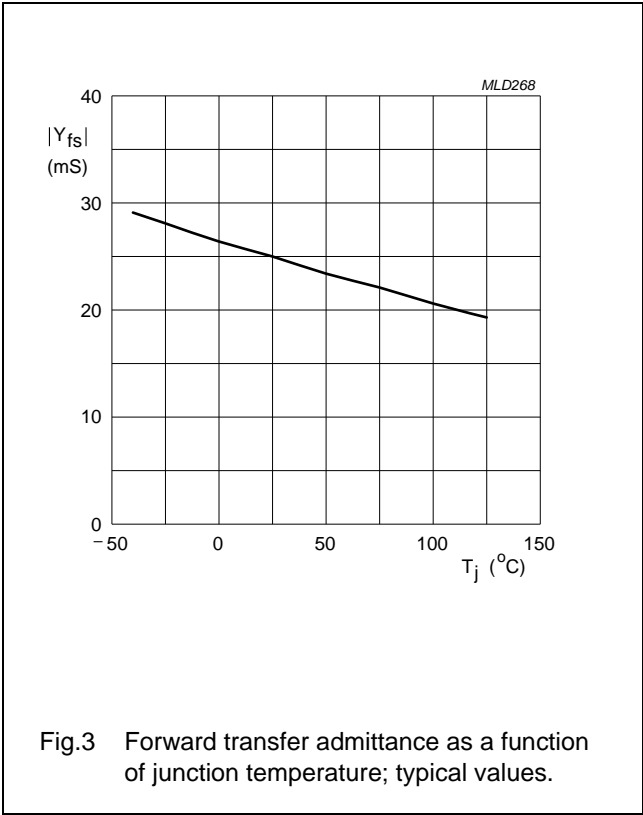
## DYNAMIC CHARACTERISTICS

Common source;  $T_{amb} = 25\ ^\circ\text{C}$ ;  $V_{DS} = 5\ \text{V}$ ;  $V_{G2-S} = 4\ \text{V}$ ;  $I_D = 10\ \text{mA}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\ ^\circ\text{C}$	22	25	30	mS
$C_{ig1-s}$	input capacitance at gate 1	$f = 1\ \text{MHz}$	—	2.2	2.6	pF
$C_{ig2-s}$	input capacitance at gate 2	$f = 1\ \text{MHz}$	1	1.5	2	pF
$C_{os}$	drain-source capacitance	$f = 1\ \text{MHz}$	1	1.3	1.6	pF
$C_{rs}$	reverse transfer capacitance	$f = 1\ \text{MHz}$	—	25	35	fF
F	noise figure	$f = 200\ \text{MHz}$ ; $G_S = 2\ \text{mS}$ ; $B_S = B_{Sopt}$	—	1	1.5	dB
		$f = 800\ \text{MHz}$ ; $G_S = G_{Sopt}$ ; $B_S = B_{Sopt}$	—	2	2.8	dB

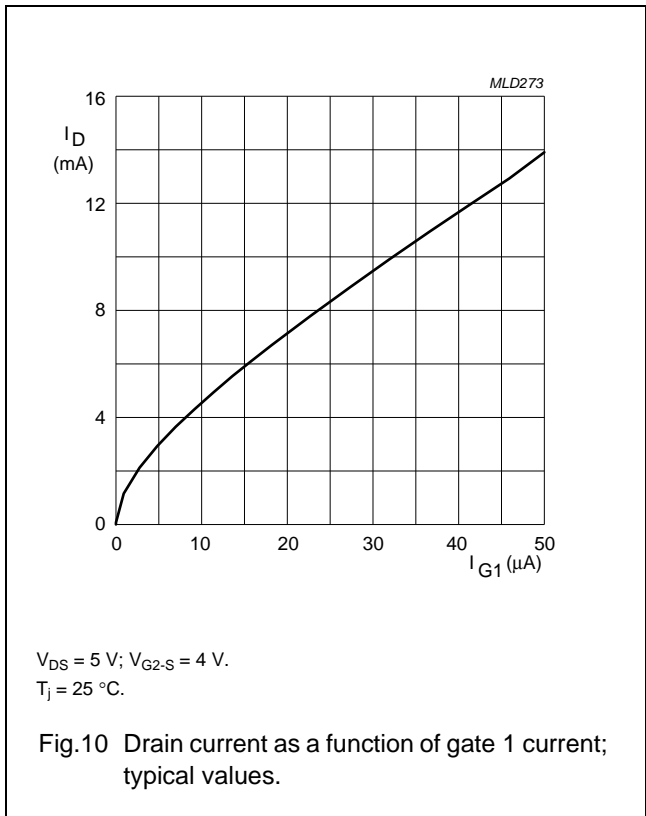
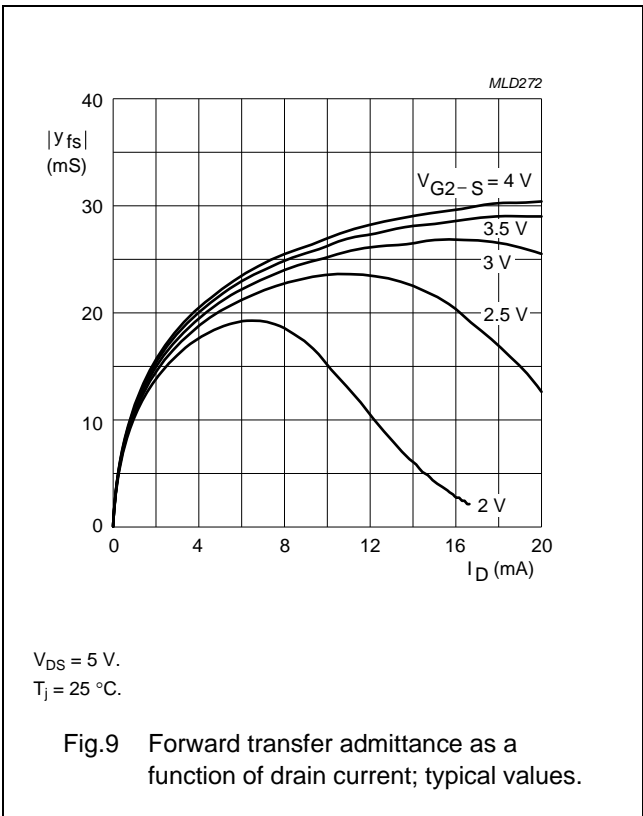
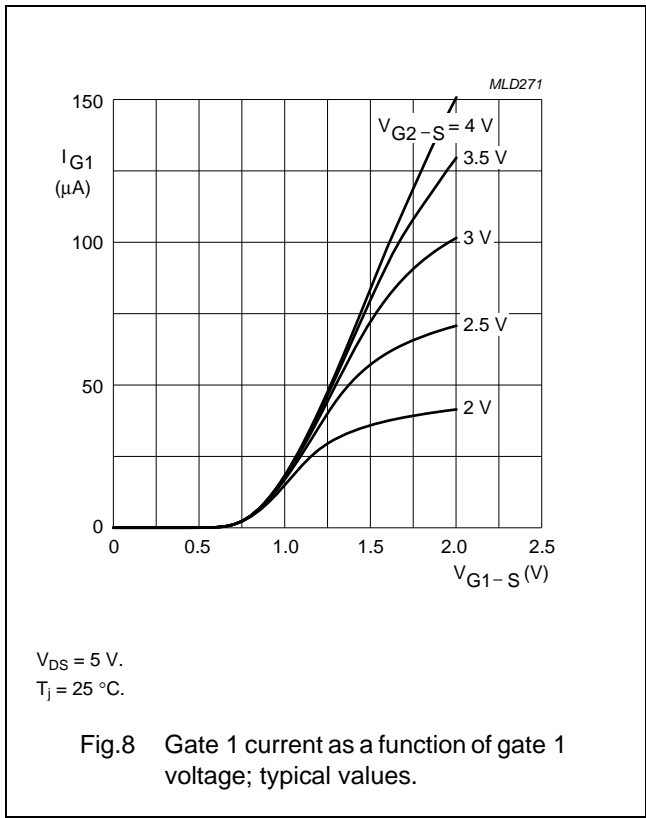
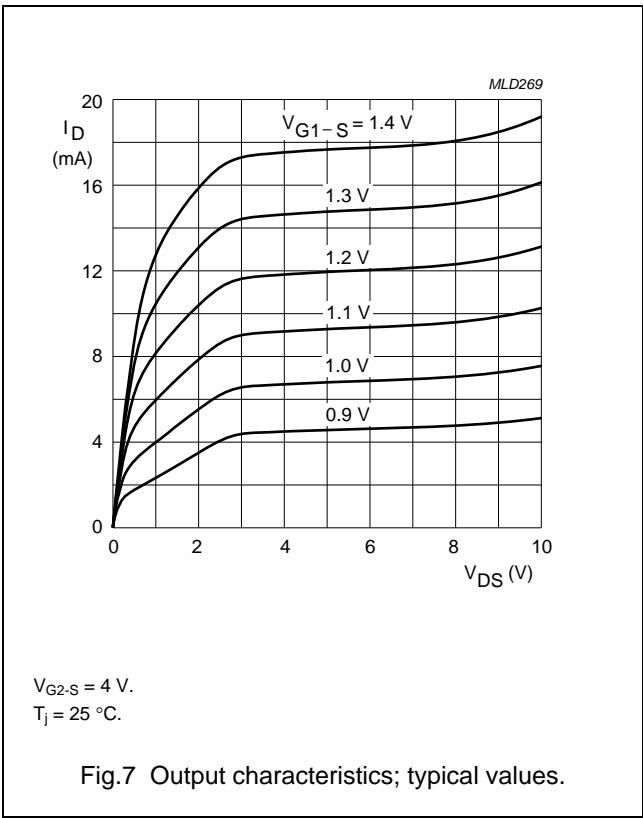
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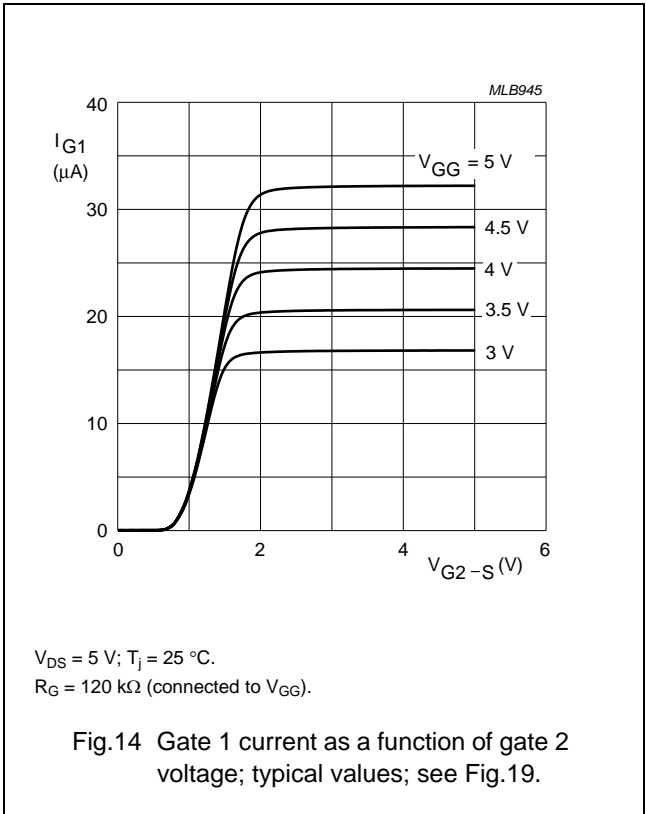
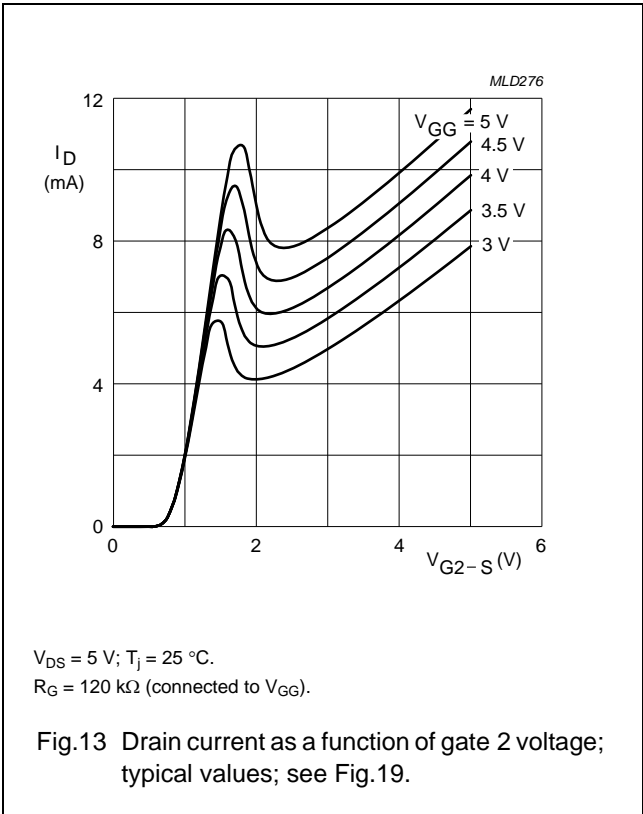
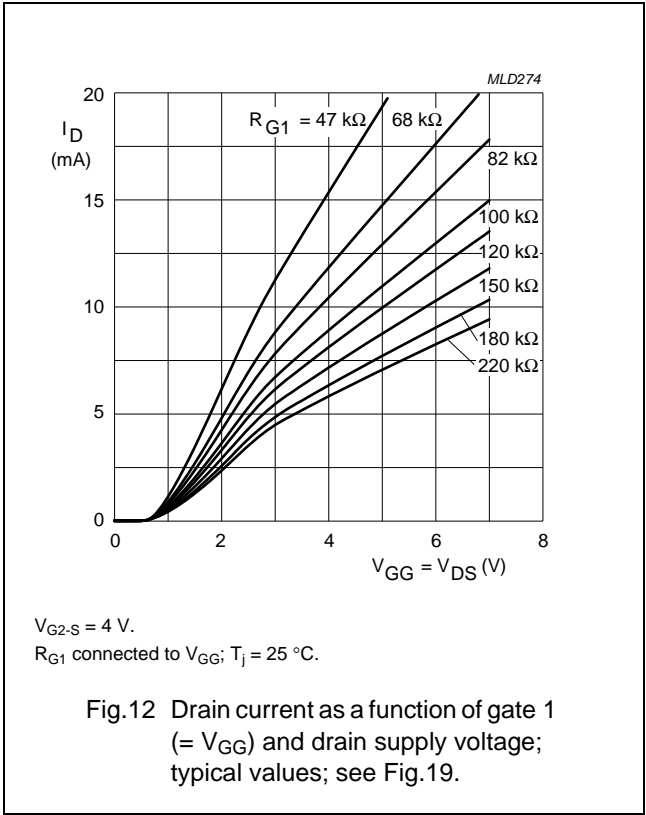
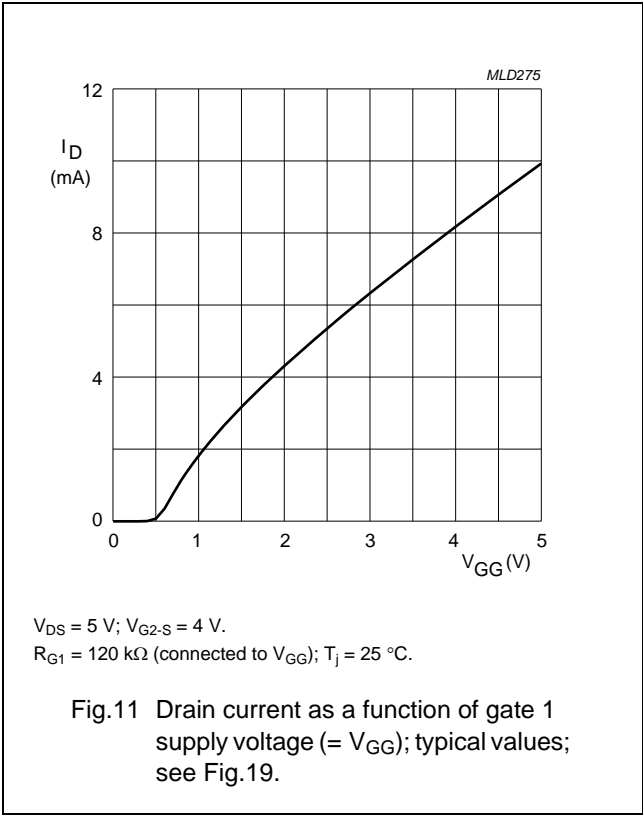
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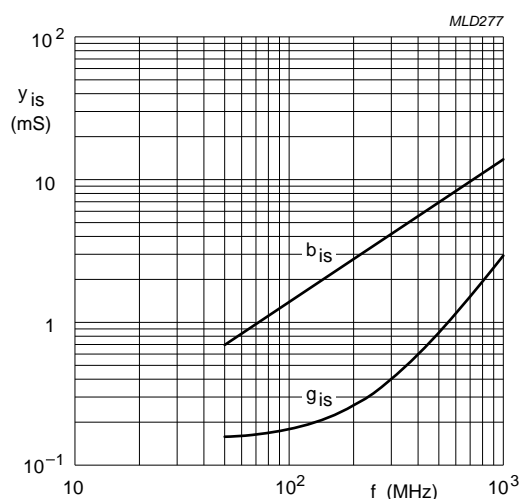
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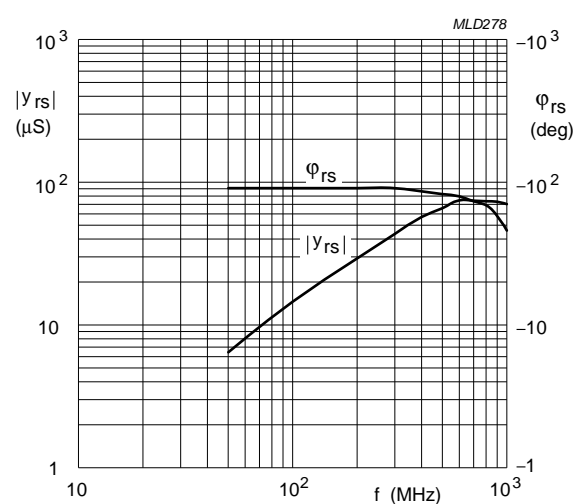
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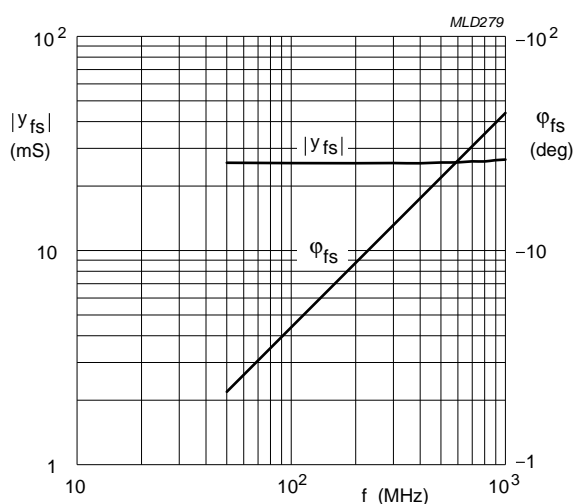
$V_{DS} = 5$  V;  $V_{G2} = 4$  V.  
 $I_D = 10$  mA;  $T_{amb} = 25$  °C.

Fig.15 Input admittance as a function of frequency; typical values.



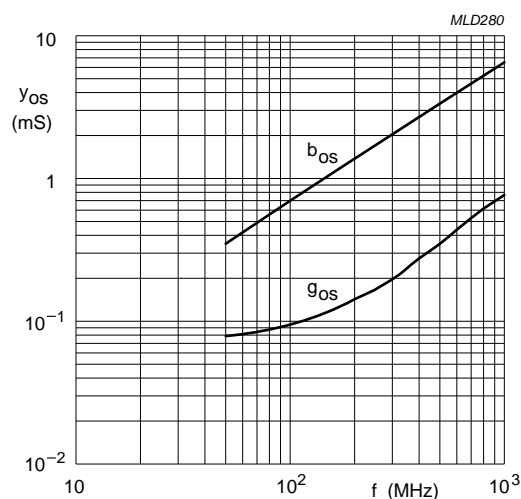
$V_{DS} = 5$  V;  $V_{G2} = 4$  V.  
 $I_D = 10$  mA;  $T_{amb} = 25$  °C.

Fig.16 Reverse transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 5$  V;  $V_{G2} = 4$  V.  
 $I_D = 10$  mA;  $T_{amb} = 25$  °C.

Fig.17 Forward transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 5$  V;  $V_{G2} = 4$  V.  
 $I_D = 10$  mA;  $T_{amb} = 25$  °C.

Fig.18 Output admittance as a function of frequency; typical values.



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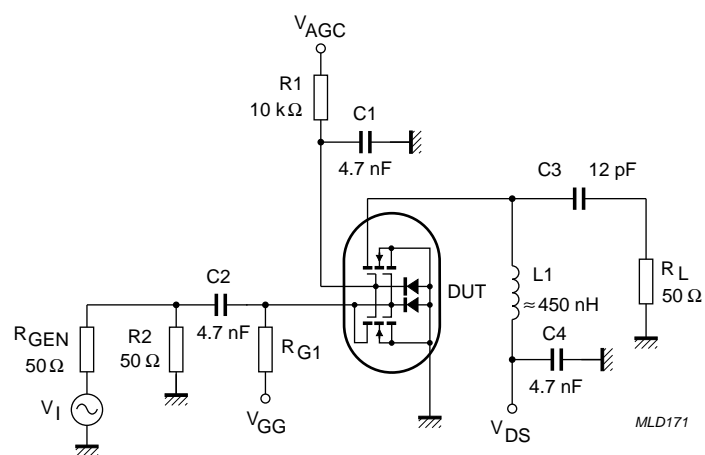


Fig.19 Cross-modulation test set-up.

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**Table 1** Scattering parameters:  $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 10\text{ mA}$ 

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.989	-3.4	2.420	175.7	0.000	79.9	0.993	-1.6
100	0.985	-8.3	2.414	169.1	0.001	78.3	0.992	-3.9
200	0.976	-16.4	2.368	158.8	0.003	80.3	0.987	-7.8
300	0.958	-24.1	2.301	148.5	0.004	73.7	0.980	-11.4
400	0.942	-32.0	2.251	138.8	0.005	70.7	0.974	-15.2
500	0.918	-39.3	2.170	129.5	0.005	67.2	0.966	-18.7
600	0.899	-46.0	2.080	120.7	0.005	67.8	0.958	-22.2
700	0.876	-52.6	2.001	112.1	0.005	68.6	0.951	-25.5
800	0.852	-58.8	1.924	103.2	0.005	72.9	0.944	-28.9
900	0.823	-64.9	1.829	94.7	0.005	78.7	0.937	-32.1
1000	0.800	-70.9	1.747	86.5	0.005	88.3	0.933	-35.2
1200	0.750	-82.4	1.621	70.7	0.005	120.5	0.928	-41.7
1400	0.719	-92.7	1.535	54.6	0.008	139.8	0.930	-48.4
1600	0.682	-102.5	1.424	39.4	0.010	137.8	0.924	-54.9
1800	0.642	-109.8	1.349	22.5	0.013	156.8	0.928	-62.9
2000	0.602	-116.5	1.283	1.1	0.018	175.1	0.928	-73.1
2200	0.547	-124.9	1.130	-15.1	0.014	172.6	0.887	-81.0
2400	0.596	-128.7	1.018	-49.1	0.040	-163.9	0.837	-95.8
2600	0.682	-132.6	0.979	-79.4	0.077	-164.0	0.778	-109.6
2800	0.771	-142.5	0.804	-116.2	0.120	178.8	0.629	-119.5
3000	0.793	-157.5	0.541	-153.5	0.149	158.3	0.479	-119.9

**Table 2** Noise data:  $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 10\text{ mA}$ 

f (MHz)	F <sub>min</sub> (dB)	$\Gamma_{opt}$		r <sub>n</sub>
		(ratio)	(deg)	
800	2.00	.686	49.6	50.40

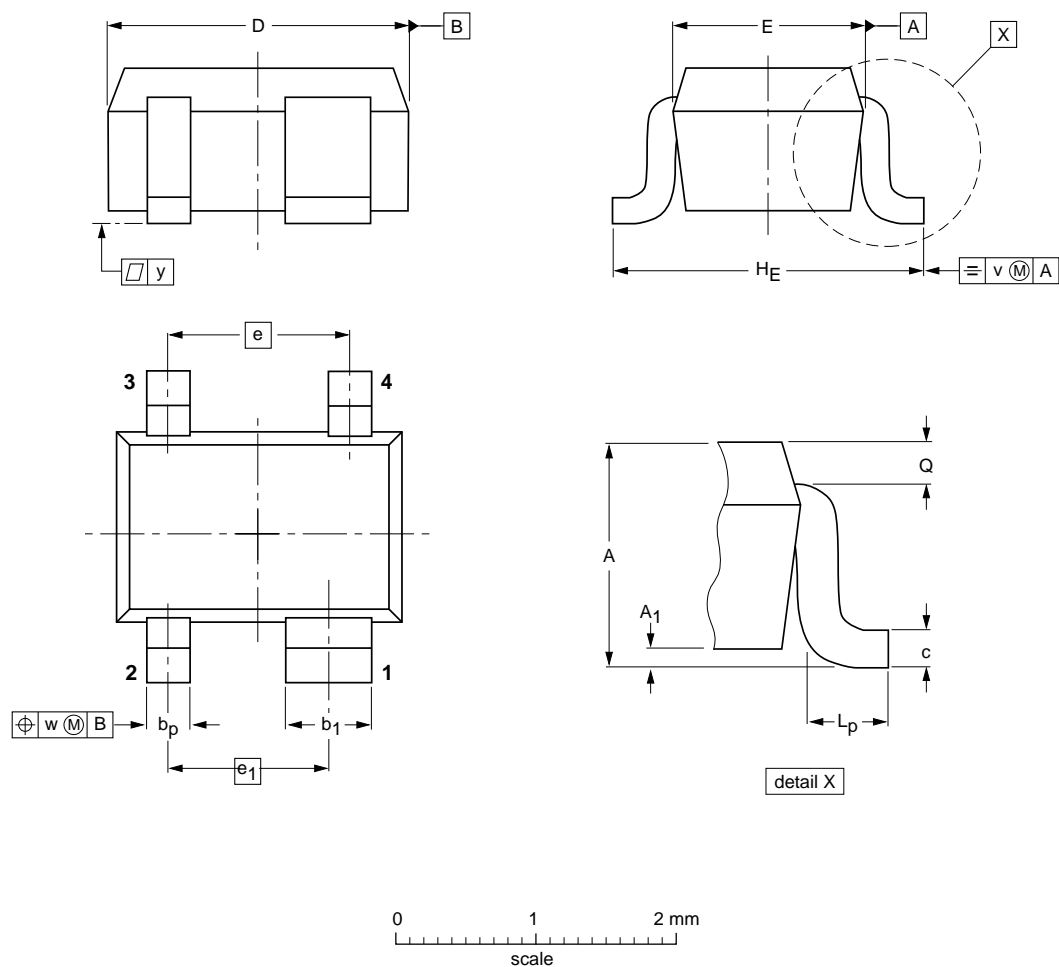
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PACKAGE OUTLINE

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>P</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>P</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21 06-03-16

## N-channel dual-gate MOS-FET

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## DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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***provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise***

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for the marking codes and the package outline drawings which were updated to the latest version.

## **Contact information**

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

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