Microprocessor Supervisory Circuit

ADM1232A

FEATURES

Precision 5 V voltage monitor with 5% or 10% tolerance options
Adjustable $\overline{\text{STROBE}}$ monitor with 150 ms, 600 ms, or 1.2 sec options
Fast (20 ns) $\overline{\text{STROBE}}$ pulse width
No external components required
Packaged in 8-Lead SOIC
Specified from −40°C to +85°C

APPLICATIONS

Microprocessor systems
Portable equipment
Computers
Controllers
Intelligent instruments
Automotive systems
Protection against damage caused by microprocessor failure

GENERAL DESCRIPTION

The ADM1232A is pin-compatible to the MAX1232, DS1232LP, and DS1232. The ADM1232A can detect strobe pulse widths as narrow as 20 ns, making it compatible with high speed microprocessors. The Analog Devices, Inc., ADM1232A is a microprocessor monitoring circuit that monitors microprocessor supply voltage. It can also detect if a microprocessor has locked up or an external interrupt has been issued. The ADM1232A is available in an 8-lead narrow body SOIC and is specified over the −40°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

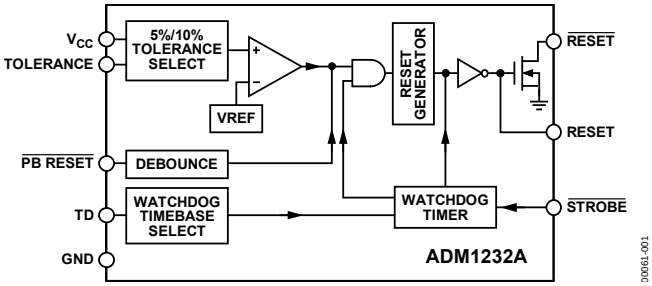

Figure 1.

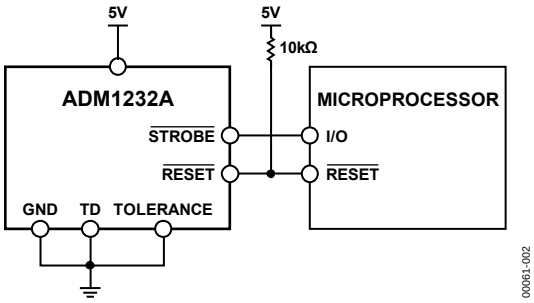

Figure 2. Typical Supply Monitoring Application

Rev. A
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REVISION HISTORY

1/09—Rev. 0 to Rev. A

Updated Format ... Universal
Deleted RM-8, N-8, R-16 Packages ... Universal
Changes to Features and General Description Sections ... 1
Changes to Table 3 ... 5
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Changes to Ordering Guide ... 8

7/99—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = full operating range, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE	−40		+85	°C	$T_A = T_{MIN}$ to T_{MAX}.
POWER SUPPLY					
Voltage	4.5	5.0	5.5	V	
Current		20	50	µA	V_{IL}, V_{IH} = CMOS levels.
		200	500	µA	V_{IL}, V_{IH} = TTL levels.
$\overline{\text{STROBE}}$ AND $\overline{\text{PB RESET}}$ INPUTS					
Input High Level	2.0		V_{CC} + 0.3	V	
Input Low Level	−0.3		+0.8	V	
INPUT LEAKAGE CURRENT					
($\overline{\text{STROBE}}$, TOLERANCE)	−1.0		+1.0	µA	
TD		1.6		µA	
OUTPUT CURRENT					
RESET	8	10		mA	When V_{CC} is at 4.5 V to 5.5 V.
$\overline{\text{RESET}}$, RESET	−8	−12		mA	When V_{CC} is at 4.5 V to 5.5 V.
OUTPUT VOLTAGE					
$\overline{\text{RESET}}$/RESET	V_{CC} − 0.5	V_{CC} − 0.1		V	While sourcing less than 500 µA, RESET remains within 0.5 V of V_{CC} on power-down until V_{CC} drops below 2.0 V. While sinking less than 500 µA, $\overline{\text{RESET}}$ remains within 0.5 V of GND on power-down until V_{CC} drops below 2.0 V.
$\overline{\text{RESET}}$/RESET High Level			0.4	V	
$\overline{\text{RESET}}$/RESET Low Level	2.4			V	
1 V OPERATION					
$\overline{\text{RESET}}$ Output Voltage		V_{CC} − 0.1		V	While sourcing less than 50 µA.
$\overline{\text{RESET}}$ Output Voltage		0.1		V	While sinking less than 50 µA.
V_{CC} TRIP POINT					
5%	4.5	4.62	4.74	V	TOLERANCE = GND.
10%	4.25	4.37	4.49	V	TOLERANCE = V_{CC}.
CAPACITANCE					
Input ($\overline{\text{STROBE}}$, TOLERANCE)			5	pF	T_A = 25°C.
Output (RESET, $\overline{\text{RESET}}$)			7	pF	T_A = 25°C.
$\overline{\text{PB RESET}}$					
Time	20			ms	$\overline{\text{PB RESET}}$ must be held low for a minimum of 20 ms to guarantee a reset.
Delay	1	4	20	ms	
RESET ACTIVE TIME	250	610	1000	ms	
$\overline{\text{STROBE}}$					
Pulse Width	20			ns	
Timeout Period	62.5	150	250	ms	TD = 0 V.
	250	600	1000	ms	TD = floating.
	500	1200	2000	ms	TD = V_{CC}.
V_{CC}					
Fall Time	10			µs	Guaranteed by design.
Rise Time	0			µs	Guaranteed by design.
V_{CC} FAIL DETECT TO RESET OUTPUT DELAY					
RESET and $\overline{\text{RESET}}$ Are Logically Correct			50	µs	After V_{CC} falls below the set tolerance voltage (see Figure 7).
	250	610	1000	ms	After V_{CC} rises above the set tolerance voltage.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	5.5 V
Logic Inputs	−0.3 V to V_{CC} + 0.3 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Power Dissipation	900 µW
Derate by 12 mW/°C Above 25°C	
θ_{JA} Thermal Impedance (Still Air)	153°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

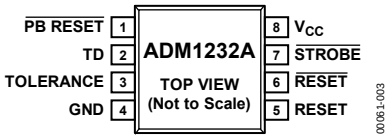

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{PB RESET}}$	Push Button Reset Input. This debounced input ignores pulses of less than 1 ms and is guaranteed to respond to pulses greater than 20 ms.
2	TD	Time Delay Set. This pin allows the user to select the maximum amount of time the ADM1232A allows the $\overline{\text{STROBE}}$ input to remain inactive (that is, $\overline{\text{STROBE}}$ is not receiving any high-to-low transitions), without forcing the ADM1232A to generate a RESET pulse. (See Table 1, the strobe timeout settings in Table 4, and Figure 6.)
3	TOLERANCE	Tolerance Input. This input determines how much the supply voltage will be allowed to decrease (as a percentage tolerance) before a RESET is asserted. Connect to V_{CC} for 10% tolerance and GND for 5% tolerance.
4	GND	0 V ground reference for all signals.
5	RESET	Active High Logic Output. This pin is asserted when V_{CC} decreases below the amount specified by the TOLERANCE input, or $\overline{\text{PB RESET}}$ is forced low, or if there are no high-to-low transitions within the limits set by TD at $\overline{\text{STROBE}}$, or during power-up.
6	$\overline{\text{RESET}}$	Open Drain, Active Low Logic Output. The inverse of RESET.
7	$\overline{\text{STROBE}}$	The $\overline{\text{STROBE}}$ input is used to monitor the activity of a microprocessor. If there are no high-to-low transitions within the time specified by TD, a reset is asserted.
8	V_{CC}	Power Supply Input +5 V.

CIRCUIT INFORMATION

PB RESET

The $\overline{\text{PB RESET}}$ input makes it possible to manually reset a system using either a standard push-button switch or a logic low input. An internal debounce circuit provides glitch immunity when used with a switch, reducing the effects of glitches on the line. The debounce circuit is guaranteed to cause the ADM1232A to assert a reset if $\overline{\text{PB RESET}}$ is brought low for more than 20 ms and is guaranteed to ignore low inputs of less than 1 ms.

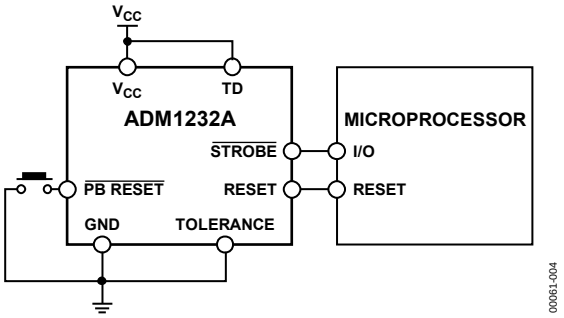

Figure 4. Typical Push-Button Reset Application

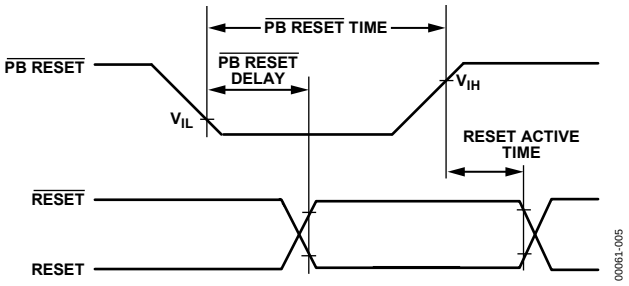

Figure 5. $\overline{\text{PB RESET}}$

$\overline{\text{STROBE}}$ TIMEOUT SELECTION

TD or time delay set is used to set the strobe timeout period. The strobe timeout period is defined as being the maximum time between high-to-low transitions that $\overline{\text{STROBE}}$ accepts before a reset is asserted (see Figure 6). The strobe timeout settings are listed in Table 4.

Table 4. Strobe Timeout Settings

Condition	Min	Typ	Max	Unit
TD = 0 V	62.5	150	250	ms
TD = floating	250	600	1000	ms
TD = V_{CC}	500	1200	2000	ms

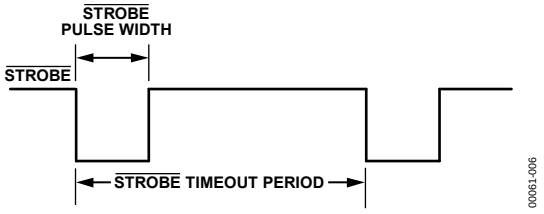

Figure 6. $\overline{\text{STROBE}}$ Parameters

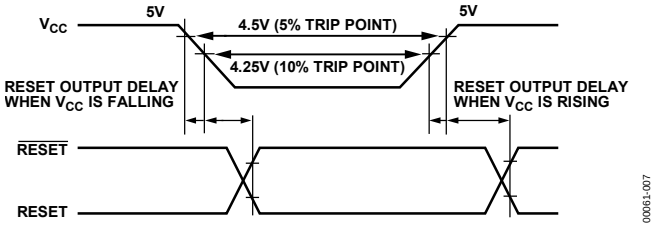

Figure 7. Reset Output Delay

TOLERANCE

The TOLERANCE input is used to determine the level V_{CC} can vary below 5 V without the ADM1232A asserting a reset. Connecting TOLERANCE to ground selects a −5% tolerance level and causes the ADM1232A to generate a reset if V_{CC} falls below 4.75 V. If TOLERANCE is connected to V_{CC}, a −10% tolerance level is selected and causes the ADM1232A to generate a reset if V_{CC} falls below 4.5 V. Check the parameters for the V_{CC} trip point in the Specifications section for more information.

RESET AND $\overline{\text{RESET}}$ OUTPUTS

While RESET is capable of sourcing and sinking current, $\overline{\text{RESET}}$ is an open drain MOSFET which sinks current only. Therefore, it is necessary to pull $\overline{\text{RESET}}$ output high.

OUTLINE DIMENSIONS

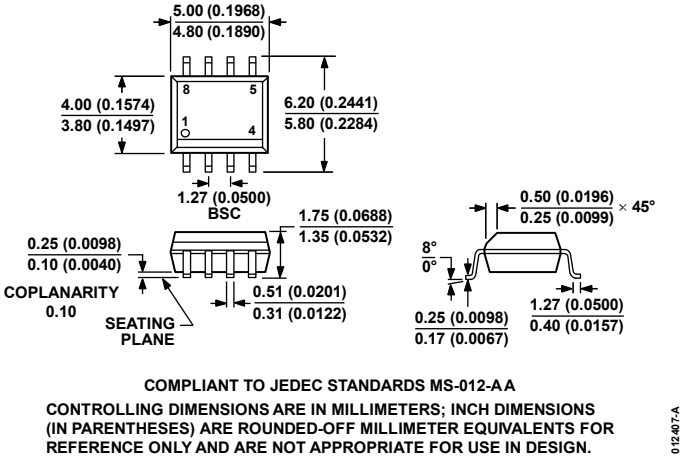

Figure 8. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1232AARNZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM1232AARNZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.

NOTES

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