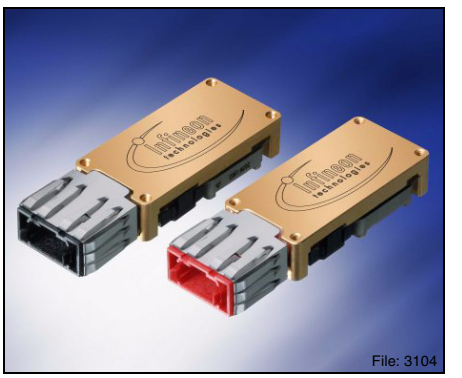
Parallel Optical Link Transmitter: PAROLI® 2 Tx AC, 1.25 Gbit/s — V23832-T2531-M101

Parallel Optical Link Receiver: PAROLI® 2 Rx AC, 1.25 Gbit/s — V23832-R511-M101

Design Benefits



- Relieve system bandwidth bottle necks
- Simplifies system design
- Enables system upgrades in field
- Low power consumption at increased board density
- Flat package for height critical application

Features

- Infineon's highly reliable 850 nm VCSEL technology
- Power supply 3.3 V
- Transmitter with multistandard electrical interface
- Receiver with Infineon's adjustable CML output
- 12 electrical data channels
- Asynchronous, AC-coupled optical link
- 12 optical data channels
- Internal power monitoring for constant power budget
- Transmission data rate of up to 1250 Mbit/s per channel, total link data rate up to 15 Gbit/s
- PIN diode array technology
- Optimized for 62.5 µm multimode graded index fiber
- MT based optical port (MPO connector)
- Plug-in module with ultra low profile
- IEC Class 1M laser eye safety compliant
- OIF[1)] compliant
- GBE mask compliant modules available
- EMI-shielding for front panel access
- Standard link length compliant
- Unused transmitter channels can be switched off
- DC or AC coupling of input data
- Telcordia compliant

[1)] OIF-VSR4-01.0 Implementation Agreement (VSR OC-192/STM-64).

PAROLI® is a registered trademark of Infineon Technologies AG

Optical Port

- Designed for the industry standard 12 fiber MT Connector (MPO)
- Alignment pins fixed in module port
- Integrated mechanical keying
- Module is provided with a dust cover

Features of MT Connector (MPO)

(as part of optional PAROLI fiber optic cables)

- Uses standardized MT ferrule
- MT compatible fiber spacing (250 µm) and alignment pin spacing (4600 µm)
- Push-pull mechanism
- Ferrule bearing spring loaded

Features of the PAROLI 2 Electrical Connector

- Pluggable version using BGA socket
- 100 pin positions (10x10)
- 4 mm stack height in mated conditions
- Plug and receptacle are provided with protective cap
- Standard BGA process for socket assembly
- Contact area plating made out of gold over nickel
- Module side: FCI-MEG-Array® -Plug (part no. 84512-202)
- PCB side: FCI-MEG-Array® -Receptacle (part no. 84513-201)

Applications

- Switches, routers, transport equipment
- Mass storage devices
- Access network
- Rack-to-rack/board-to-board interconnect
- Optical backplane interconnect

Pin Configuration

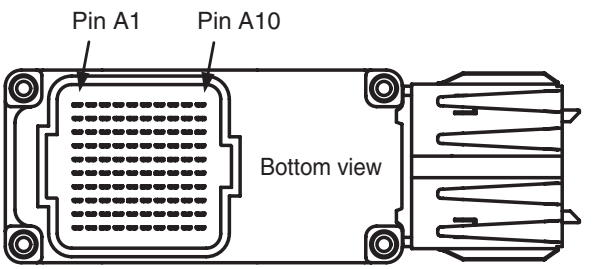


Figure 1 Pin Information Transmitter

Numbering Conventions Transmitter (bottom view)

	J	I	H	G	F	E	D	C	B	A
1	V_{EE}	DI05N	DI05P	DI06N	DI06P	DI07N	DI07P	DI08N	DI08P	V_{EE}
2	DI04P	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DI09N
3	DI04N	V_{EE}	Reserved	Reserved	t.b.l.o.	t.b.l.o.	Reserved	Reserved	V_{EE}	DI09P
4	DI01P	V_{EE}	Reserved	Reserved	t.b.l.o.	t.b.l.o.	Reserved	Reserved	V_{EE}	DI12N
5	DI01N	V_{EE}	V_{EE}	V_{EE}	t.b.l.o.	t.b.l.o.	V_{EE}	V_{EE}	V_{EE}	DI12P
6	DI02P	V_{EE}	V_{EE}	V_{EE}	t.b.l.o.	–LE	V_{EE}	V_{EE}	V_{EE}	DI11N
7	DI02N	V_{EE}	V_{EE}	V_{EE}	LCU	LE	V_{EE}	V_{EE}	V_{EE}	DI11P
8	DI03P	V_{EE}	V_{EE}	V_{EE}	V_{IN}	–RESET	V_{EE}	V_{EE}	V_{EE}	DI10N
9	DI03N	V_{EE}	V_{EE}	V_{EE}	V_{CC}	V_{CC}	V_{EE}	V_{EE}	V_{EE}	DI10P
10	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{CC}	V_{CC}	V_{EE}	V_{EE}	V_{EE}	V_{EE}

This edge towards MPO connector

Pin Description Transmitter

Symbol	Level/Logic	Description
V_{CC}		Power supply voltage of laser driver
V_{IN}		CML: V_{IN} = Reference supply (e.g. V_{CC}) LVDS, LVPECL: V_{IN} = V_{EE}
V_{EE}		Ground
LCU	LVCMOS Out	Laser Controller Up. High = normal operation. Low = laser fault or RESETlow.
DIxxN	Signal In	Data Input #xx, inverted
DIxxP	Signal In	Data Input #xx, non-inverted
–RESET	LVCMOS In	High = laser diode array is active. Low = switches laser diode array off. This input has an internal pull-down to ensure laser eye safety switch off in case of unconnected RESETinput.
LE	LVCMOS In	Laser ENABLE. High active. High = laser array is on if LE is also active. Low = laser array is off. This input has an internal pull-up, therefore can be left open.
–LE	LVCMOS In	Laser ENABLE. Low active. Low = laser array is on if LE is also active. This input has an internal pull-down, therefore can be left open.
t.b.l.o.		to be left open
Reserved		Reserved for future use

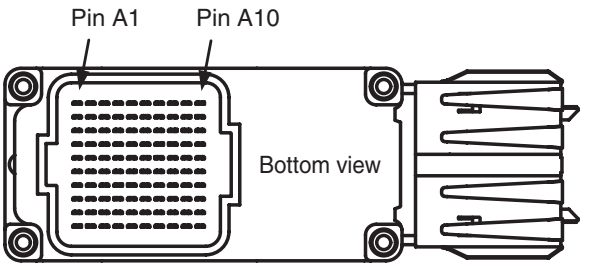


Figure 2 Pin Information Receiver

Numbering Conventions Receiver (bottom view)

	J	I	H	G	F	E	D	C	B	A
1	V_{EE}	DO05P	DO05N	DO06P	DO06N	DO07P	DO07N	DO08P	DO08N	V_{EE}
2	DO04N	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DO09P
3	DO04P	V_{EE}	Reserved	Reserved	t.b.l.o.	t.b.l.o.	Reserved	Reserved	V_{EE}	DO09N
4	DO01N	V_{EE}	Reserved	Reserved	OEN	ENSD	Reserved	Reserved	V_{EE}	DO12P
5	DO01P	V_{EE}	V_{EE}	V_{EE}	SD01	–SD12	V_{EE}	V_{EE}	V_{EE}	DO12N
6	DO02N	V_{EE}	V_{EE}	V_{EE}	Reserved	REFR	V_{EE}	V_{EE}	V_{EE}	DO11P
7	DO02P	V_{EE}	V_{EE}	V_{EE}	V_{CCO}	V_{CCO}	V_{EE}	V_{EE}	V_{EE}	DO11N
8	DO03N	V_{EE}	V_{EE}	V_{EE}	V_{CCO}	V_{CCO}	V_{EE}	V_{EE}	V_{EE}	DO10P
9	DO03P	V_{EE}	V_{EE}	V_{EE}	V_{CC}	V_{CC}	V_{EE}	V_{EE}	V_{EE}	DO10N
10	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{CC}	V_{CC}	V_{EE}	V_{EE}	V_{EE}	V_{EE}

This edge towards MPO connector

Pin Description Receiver

Symbol	Level/Logic	Description
V_{CC}		Power supply voltage of pre amplifier and analog circuitry
V_{CCO}		Power supply voltage of output stages
REFR		Adjustment of output current by connecting external resistor to V_{EE}
V_{EE}		Ground
OEN	LVCMOS In	Output Enable High = normal operation. Low = sets all Data Outputs to low. This input has an internal pull-up which pulls to high level when this input is left open.
ENSD	LVCMOS In	High = SD1 and –SD12 function enabled. Low = SD1 and –SD12 are set to permanent active. This input has an internal pull-up which pulls to high level when this input is left open.
SD1	LVCMOS Out	Signal Detect on fiber #1. High = signal of sufficient AC power is present on fiber #1. Low = signal on fiber #1 is insufficient.
–SD12	LVCMOS Out low active	Signal Detect on fiber #12. Low = signal of sufficient AC power is present on fiber #12. High = signal on fiber #12 is insufficient.
DOxxP	CML Out	Data Output #xx, non-inverted
DOxxN	CML Out	Data Output #xx, inverted
t.b.l.o.		to be left open
Reserved		Reserved for future use

Description

PAROLI is a parallel optical link for high-speed data transmission. A complete PAROLI link consists of a transmitter module, a 12-channel fiber optic cable, and a receiver module. The transmitter supports LVDS, CML and LVPECL differential signals. Two different receiver modules are available. Module V23832-R521-M101 is for LVDS electrical output only. This specification (V23832-R511-M101) describes a receiver for Infineon's adjustable CML output.

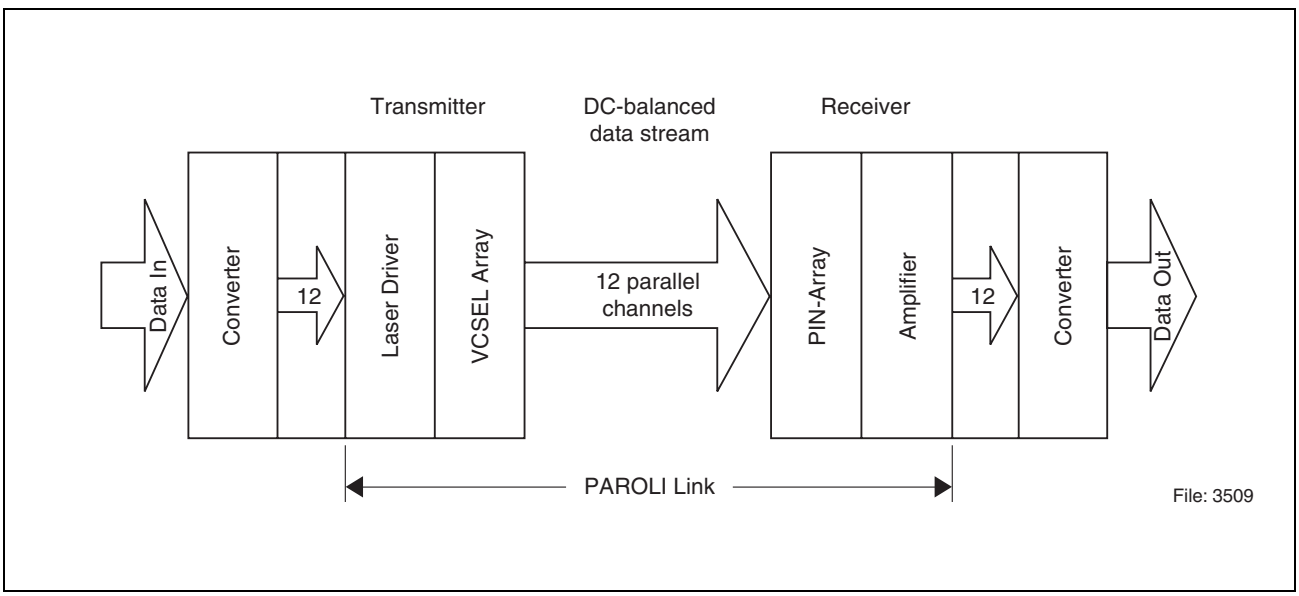


Figure 3 Example of a PAROLI Link

Transmitter V23832-T2531-M101

The transmitter module converts parallel electrical input signals via a laser driver and a Vertical Cavity Surface Emitting Laser (VCSEL) diode array into parallel optical output signals. All input data signals are Multistandard Differential Signals (LVDS compatible; LVPECL and CML is also supported because of the wide common input range). The electrical interface (LVDS, LVPECL or CML) is selected by the supply inputs V_{IN}. The data rate is up to 1250 Mbit/s for each channel. The transmitter module's min. data rate of 500 Mbit/s is specified for the CID[1)] worst case pattern (disparity 72) or any pattern with a lower disparity. The transmitter features active feedback of optical output power and extinction ratio, which guarantees a constant power budget.

Unused channels can be forced to a quiescent state by applying e.g. a constant high level to the input stage of these channels. The integrated alerter circuit (see **"Laser Eye Safety Design Considerations" on Page 12**) will switch off the corresponding transmitter output, which results also in a reduced power consumption. Unused transmitter input channels can also be left open. The integrated swing detection circuit will assure a quiescent output state for these channels.

A logic low level at –RESET switches all laser outputs off. During power-up –RESET must be used as a power-on reset which disables the laser driver and laser control until the power supply has reached a 3.135 V level.

The Laser Controller Up (LCU) output is low if a laser fault is detected or –RESET is forced to low.

All non data signals have LVCMOS levels.

Transmission delay of the PAROLI system is ≤ 1 ns for the transmitter, ≤ 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

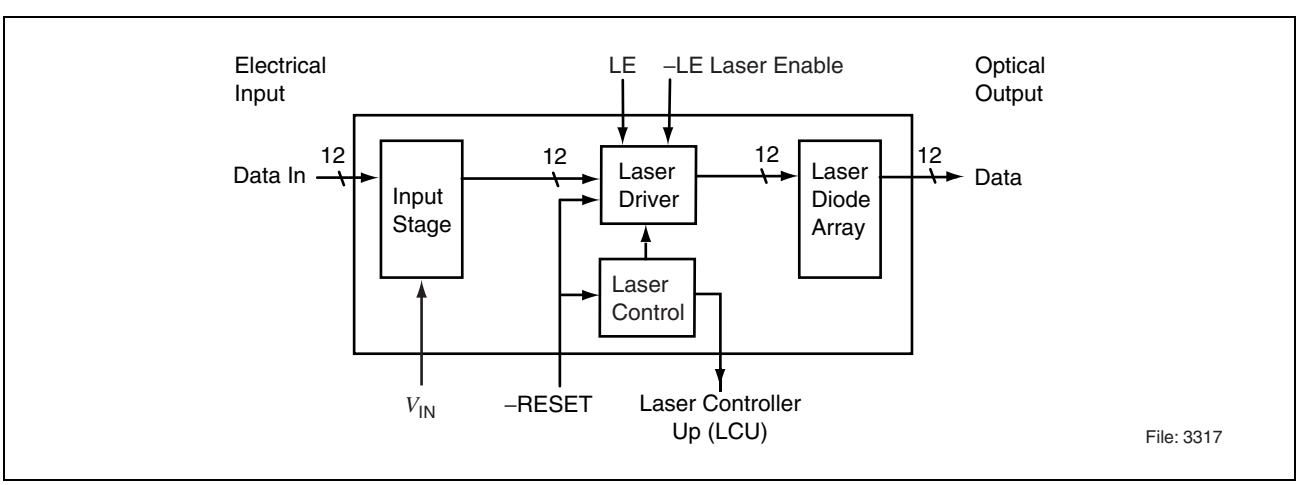


Figure 4 Transmitter Block Diagram

[1)] Consecutive Identical Digit (CID) immunity test pattern for STM-N signals, ITU-T recommendation G.957 sec. II.

Receiver V23832-R511-M101

The PAROLI receiver module converts parallel optical input signals into parallel electrical output signals. The optical signals received are converted into voltage signals by PIN diodes, trans impedance amplifiers, and gain amplifiers. The differential data outputs are Infineon's adjustable CML signals. A separate module (V23832-R521-M101) with LVDS output is also available. The output differential voltage (swing) is adjusted by an external resistor connected to the REFR module input, the output average is adjustable by external pull-up resistors.

The data rate is up to 1250 Mbit/s for each channel. The receiver module's min. data rate of 500 Mbit/s is specified for the CID[1)] worst case pattern (disparity 72) or any pattern with a lower disparity.

Additional Signal Detect outputs (SD1 active high / –SD12 active low) show whether an optical AC input signal is present at data input 1 and/or 12. The signal detect circuit can be disabled with a logic low at ENSD. The disabled signal detect circuit will permanently generate an active level at Signal Detect outputs, even if there is insufficient signal input. This could be used for test purposes.

A logic low at Output Enable sets all data outputs to logic low. SD outputs will not be effected.

All non data signals have LVCMOS levels. Transmission delay of the PAROLI system is ≤ 1 ns for the transmitter, ≤ 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

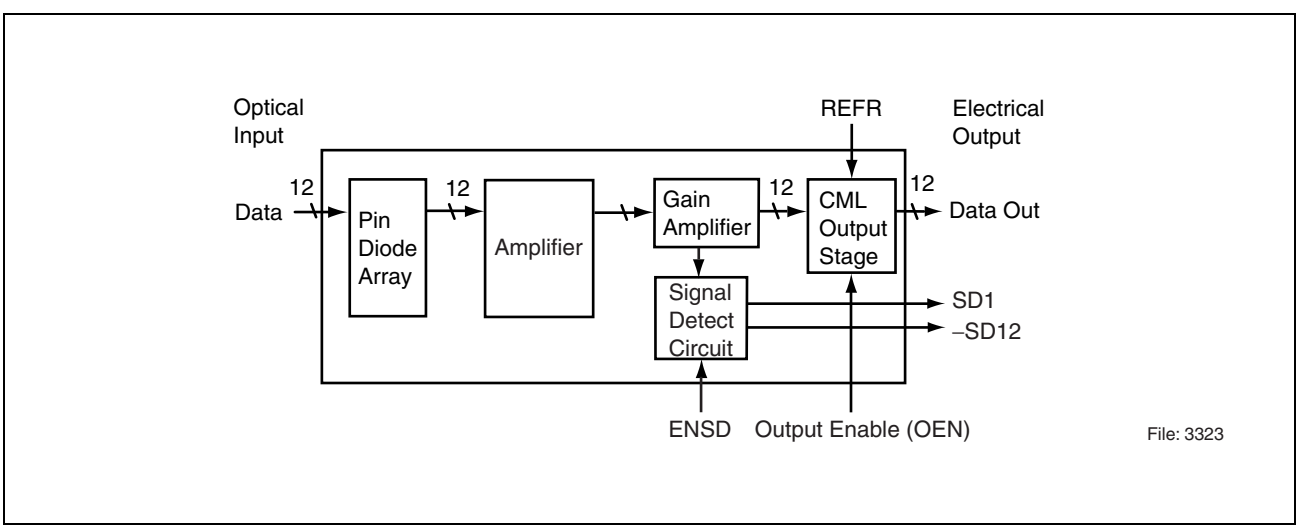


Figure 5 Receiver Block Diagram

[1)] Consecutive Identical Digit (CID) immunity test pattern for STM-N signals, ITU-T recommendation G.957 sec. II.

Regulatory Compliance

The following table shows industry standard test methods and results obtained from the indicated test methods. (The overall system design will affect the electromagnetic interference (EMI), electrostatic discharge (ESD) and immunity).

Feature	Standard	Comments
ESD: Electrostatic Discharge to the Electrical Pins (HBM)	JEDEC Human Body Model (HBM) Test Method EIA/JESD22-A114-B (MIL-STD 883D method 3015.7)	Class 1C
Immunity: Against Electrostatic Discharge (ESD) to the Module Receptacle	EN 61000-4-2 IEC 61000-4-2	Discharges ranging from ±2 kV to ±15 kV on the front end/face-plate/ receptacle cause no damage to module (under recommended mounting conditions).
Immunity: Against Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 61000-4-3	With a field strength of 3 V/m, noise frequency ranges from 10 MHz to 2 GHz[1]. No effect on module performance between the specification limits.
Emission: Electromagnetic Interference (EMI)	FCC 47 CFR Part 15, Class B EN 55022 Class B CISPR 22	Noise frequency range: 30 MHz to 18 GHz; Radiated Emission does not exceed specified limits when measured inside a shielding enclosure with recommended cutout dimensions. Typically pass with > 11 dB margin to the limit (under recommended mounting conditions).

[1] This test covers high frequency bands of mobile phones.

EMI Recommendations

EMI behavior of each PAROLI module revision is evaluated and measured - in order to ensure a good and sufficient EMI performance of all PAROLI modules. As the total EMI performance will also depend on system design and to avoid electromagnetic radiation exceeding the required limits set by the standards, please take note of the following recommendations.

When Gigabit switching components are found on a PCB (e.g. multiplexer, serializer-deserializer, clock data recovery, etc.), any opening of the chassis may leak radiation; this may also occur at chassis slots other than that of the device itself. Thus every mechanical opening or aperture should be as small as feasible and its length carefully considered.

On the board itself, every data connection should be an impedance matched line (e.g. micro strip, strip line or coplanar strip line). Data (D) and Data-not (Dn) should be routed symmetrically. Vias should be avoided. Where internal termination inside an IC or a PAROLI module is not present, a line terminating resistor must be provided.

The decision of how best to establish a ground depends on many boundary conditions. This decision may turn out to be critical for achieving lowest EMI performance. At RF frequencies the ground plane will always carry some amount of RF noise. Thus the ground and V_{CC} planes are often major radiators inside an enclosure.

As a general rule, for small systems such as PCI cards placed inside poorly shielded enclosures, the common ground scheme has often proven to be most effective in reducing RF emissions. In a common ground scheme, the PCI card becomes more equipotential with the chassis ground. As a result, the overall radiation will decrease. In a common ground scheme, it is strongly recommended to provide a proper contact between signal ground and chassis ground at every location where possible. This concept is designed to avoid hotspots which are places of highest radiation, caused when only a few connections between chassis and signal grounds exist. Compensation currents would concentrate at these connections, causing radiation.

However, as signal ground may be the main cause for parasitic radiation, connecting chassis ground and signal ground at the wrong place may result in enhanced RF emissions. For example, connecting chassis ground and signal ground at a front panel/bezel/chassis by means of a fiber optic module may result in a large amount of radiation especially where combined with an inadequate number of grounding points between signal ground and chassis ground. Thus the fiber optic module becomes a single contact point increasing radiation emissions. Even a capacitive coupling between signal ground and chassis ground may be harmful if it is too close to an opening or an aperture. For a number of systems, enforcing a strict separation of signal ground from chassis ground may be advantageous, providing the housing does not present any slots or other discontinuities. This separate ground concept seems to be more suitable in huge systems.

The return path of RF current must also be considered. Thus a split ground plane between Tx and Rx paths may result in severe EMI problems.

The bezel opening for a transceiver should be sized so that all contact springs of the transceiver cage make good electrical contact with the face plate.

Please consider that the PCB may behave like a dielectric waveguide. With a dielectric constant of 4, the wavelength of the harmonics inside the PCB will be half of that in free space. Thus even the smallest PCBs may have unexpected resonances.

Laser Eye Safety

The transmitter of the AC coupled Parallel Optical Link (PAROLI) is an IEC 60825-1 Amend. 2 Class 1M laser product. It complies with FDA performance standards (21 CFR 1040.10 and 1040.11) for laser products except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.

The PAROLI module must be operated under the specified operating conditions (supply voltage can be adjusted between 3.0 V and 3.6 V) under any circumstances to ensure laser eye safety.

Class 1M Laser Product

Attention: Invisible laser radiation. Do not view directly with optical instruments.

Note: Any modification of the module will be considered an act of "manufacturing", and will require, under law, recertification of the product under FDA (21 CFR 1040.10 (i)).

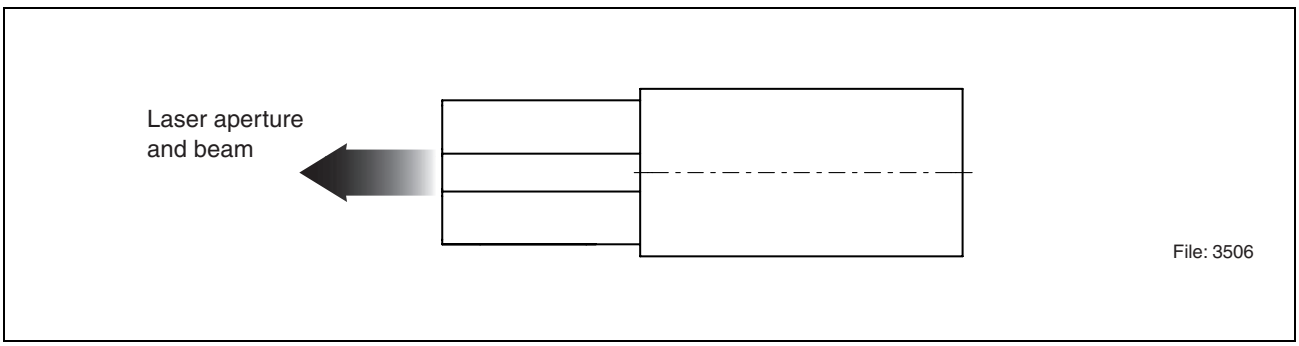


Figure 6 Laser Emission

Laser Eye Safety Design Considerations

To ensure laser eye safety for all input data patterns each channel is controlled internally and will be switched off if the laser eye safety limits are exceeded. A channel alerter switches the respective data channel output off if the input duty cycle permanently exceeds 57% (switching range 57 % min. - 65 % max.). The alerter will not disable the channel below an input duty cycle of 57% under all circumstances.

The minimum alerter response time is 1 µs with a constant high input, i.e. in the input pattern the time interval of excessive high input (e.g. '1's in excess of a 57% duty cycle, consecutive or non-consecutive) must not exceed 1 µs, otherwise the respective channel will be switched off. The alerter switches the respective channel from off to on without the need of resetting the module if the input duty cycle is no longer violated.

All of the channel alerters operate independently, i.e. an alert within a channel does not affect the other channels. To decrease the power consumption of the module unused channel inputs can be tied to high input level. In this way a portion of the supply current in this channel is triggered to shut down by the corresponding alerter.

Laser Eye Safety Measurement Conditions

Laser Data	Symbol	Values			Unit	Condition
		min.	typ.	max.		
Center wavelength	λ_C	830	850	860	nm	T_{case} 0...80°C
Array size			12		channels	
Divergence angle/ Numerical Aperture	Θ/NA	44/0.22			°/rad	Θ full / NA half angle
IEC class 1M Accessible Emission Limit	AEL			6.36	dBm	7 mm aperture @ 100 mm distance
Applying penalties (safety margin)	ΔP_{opt}			4.2	dB	
Test limit				2.16	dBm	

Technical Data

Absolute Maximum Ratings

Stress beyond the values stated below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Performance between absolute maximum ratings and recommended operating conditions is not guaranteed.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply Voltage	V_{CC}–V_{EE}	–0.3	4.5	V
Data/Control Input Levels[1]	V_{IN}	–0.5	V_{CC}+0.5	V
Data Input Differential Voltage[2]	$\|V_{ID}\|$		2.0	V
Operating Case Temperature[3]	T_{case}	0	90	°C
Storage Ambient Temperature	T_{stg}	–40	100	°C
Relative Humidity (non condensing)		5	95	%
ESD Resistance (all pins to V_{EE}, human body model)[4] (see table **“Regulatory Compliance” on Page 10**)			1	kV

1) At Data and LVCMOS inputs.
2) $|V_{ID}|$ = |(input voltage of non-inverted input minus input voltage of inverted input)|.
3) Measured at case temperature reference point (see **Figure 18** on **Page 31**).
4) To avoid electrostatic damage, handling cautions similar to those used for MOS devices must be observed.

Recommended Operating Conditions[1)]

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Transmitter					
Operating Case Temperature	T_{case}	0	45	80	°C
Power Supply Voltage	V_{CC}	3.135	3.3	3.6	V
Noise on Power Supply[2)]	N_{PS}			200	mV
Data Input Voltage Range (DC-coupled)[3), 4)]	V_{DATAI}	500		V_{CC}	mV
Data Input Differential Voltage (DC- or AC-coupled)[4), 5)]	$\|V_{ID}\|$	80		1000	mV
Data Input Skew[6)]	t_{SPN}			0.5 x $t_{R\text{-}DI}$, $t_{F\text{-}DI}$	ps
Data Input Rise/Fall Time[7)]	$t_{R\text{-}DI}$, $t_{F\text{-}DI}$	50		360	ps
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0		V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}		0.8	V
LVCMOS Input Rise/Fall Time[8)]	$t_{R\text{-}LVCMOSI}$, $t_{F\text{-}LVCMOSI}$			20	ns
Receiver					
Power Supply Voltages	V_{CC}, V_{CCO}	3.0	3.3	3.6	V
Noise on Power Supply[2)]	N_{PS}			200	mV
Output Current[9)]	I_{out}	3		9	mA
Output Voltage (DC-coupled)[10)]	V_{out}	V_{CCO}–1.8		V_{CCO}+0.5	V
Output Differential Voltage (DC- or AC-coupled)[10), 11)]	$\|V_{OD}\|$	80		800	mV
Output Load RC Time Constant	t_{RC}			150	ps
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0		V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}		0.8	V
LVCMOS Input Rise/Fall Time[8)]	$t_{R\text{-}LVCMOSI}$, $t_{F\text{-}LVCMOSI}$			20	ns
Optical Input Rise/Fall Time[12)]	$t_{R\text{-}OI}$, $t_{F\text{-}OI}$			400	ps
Input Extinction Ratio	ER	6.0			dB
Input Center Wavelength	λ_C	830		860	nm

Voltages refer to V_{EE} = 0 V.

1) Recommended range of input parameters for specified module functional performance.
2) Noise frequency is 1 kHz to f_{max}, where f_{max} is equal to the maximum data rate in units of MHz. E.g. for a maximum data rate of 2700 Mbit/s, f_{max} = 2700 MHz. Power supply noise is defined with the recommended filter in place at the supply side of the filtering circuit (see **Figure 9** on **Page 17**).
3) The input stage can also be AC-coupled.
4) Input level diagram: see **Figure 7** on **Page 16**.
5) $|V_{ID}|$ = |(input voltage of non-inverted input minus input voltage of inverted input)|.
6) Skew between positive and negative inputs measured at 50% level.
7) 20% - 80% level.
8) Measured between 0.8 V and 2.0 V.
9) $I_{out} \approx 10*1.15\ V/R_{external}$. Resistor $R_{external}$ to be connected externally between REFR and V_{EE}.
10) Output level diagram: see **Figure 8** on **Page 16**.
11) $|V_{OD}| = I_{out}*(300\ \Omega \parallel R_{LOAD})$. The output current range of 3 mA to 9 mA corresponds to $|V_{OD}|$ = 130 mV to 385 mV for R_{LOAD} = 50 Ω.
$|V_{OD}|$ = |(output voltage of non-inverted output minus output voltage of inverted output)|.
12) 20% - 80% level. Non filtered values.

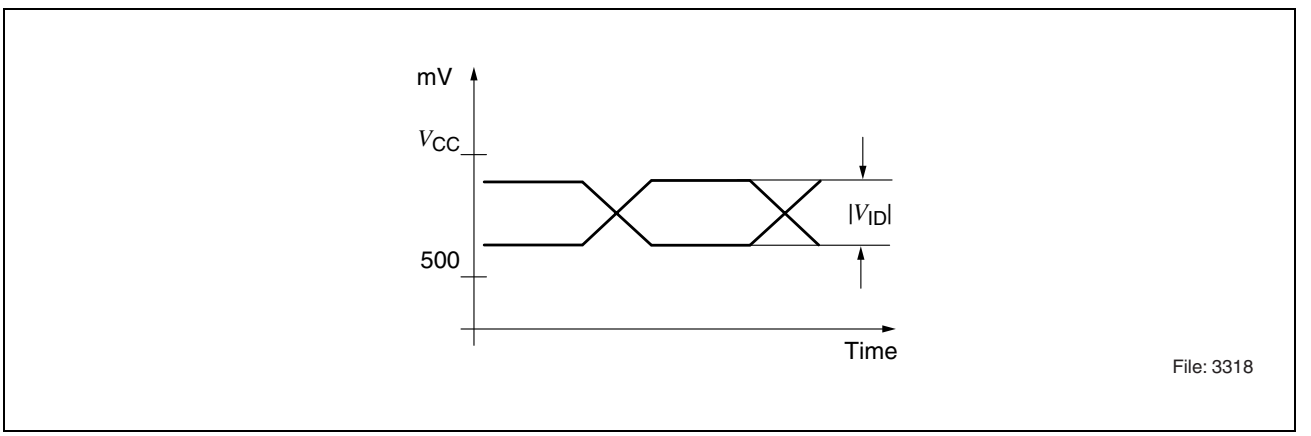


Figure 7 Input Level Diagram, DC-coupling

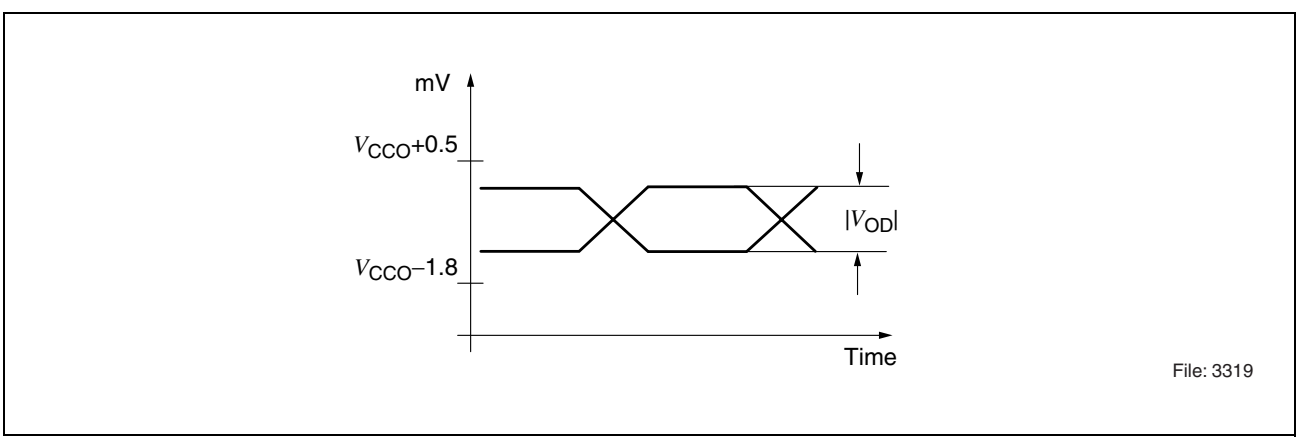


Figure 8 Output Level Diagram, DC-coupling

Recommended Power Supply Filtering

A power supply filtering is recommended for the transmitter and the receiver module. A possible filtering scheme is shown in **Figure 9**. The module signal and chassis ground refer to a common ground plane, which can be contacted to the PCB ground by the mounting screws (see **Figure 17 “PCB Layout” on Page 28**).

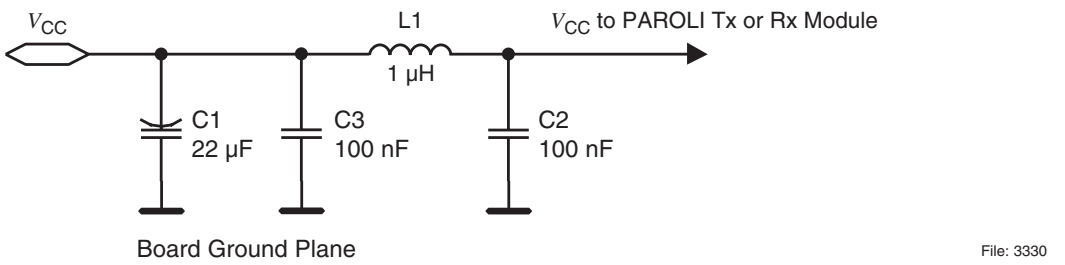


Figure 9 Filtering Scheme

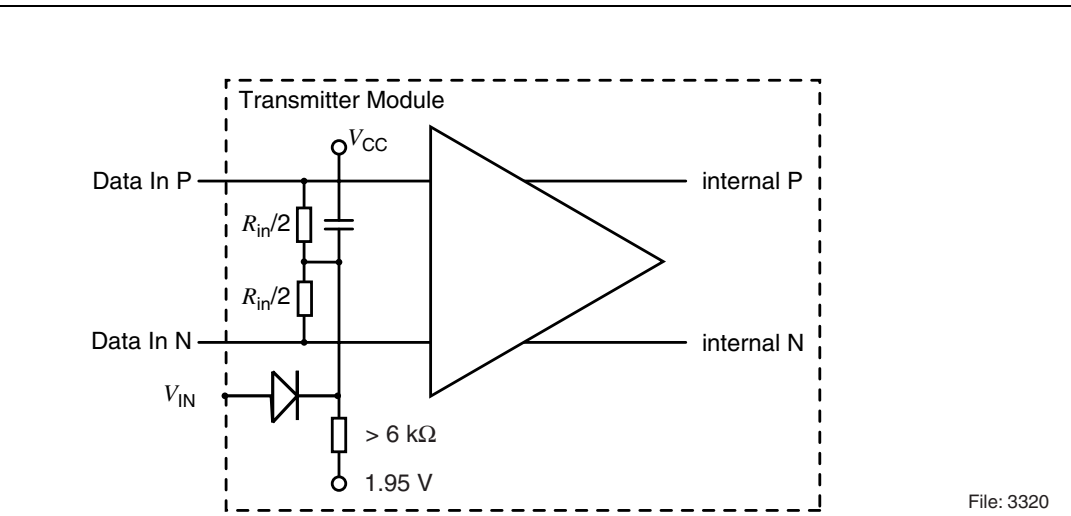


Figure 10 Transmitter - Input Stage

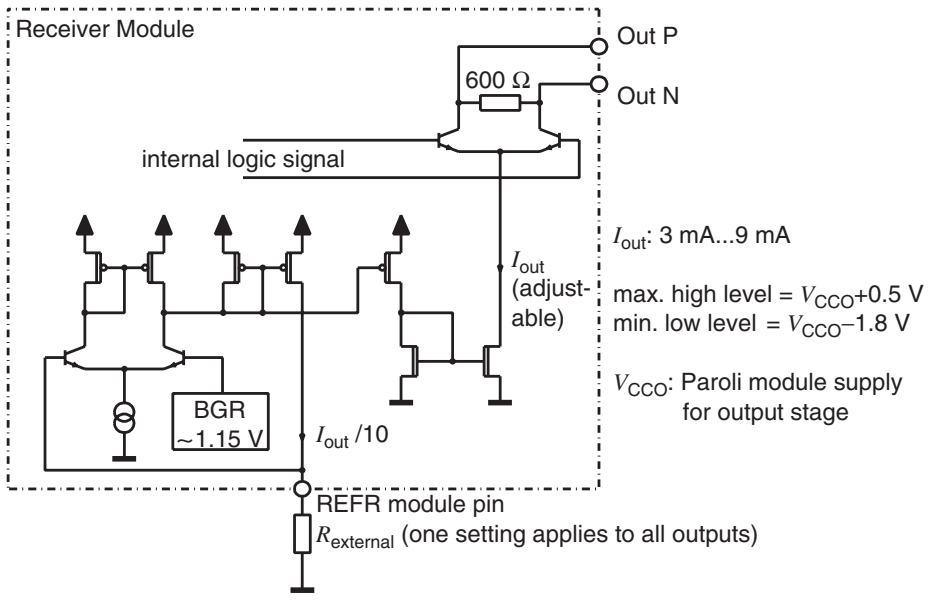


Figure 11 Receiver - CML Output Stage

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

Transmitter Electrical Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Supply Current[1]	I_{CC}		400	450	mA
Power Consumption[1]	P		1.3	1.6	W
Data Rate per Channel	DR	500[2]		1250	Mbit/s
LVCMOS Output Voltage Low	$V_{LVCMOSOL}$			0.4	V
LVCMOS Output Voltage High	$V_{LVCMOSOH}$	2.5			V
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	–100		100	µA
LVCMOS Output Current High[3]	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output Current Low[4]	$I_{LVCMOSOL}$			4.0	mA
Data Differential Input Impedance[5]	R_{IN}	80	100	120	Ω

[1] Measured at the recommended case temperature of T_{case} = 45°C. For T_{case} = 0°C a decrease of approximately 10% and for T_{case} = 80°C an increase of approximately 15% can be expected.

[2] Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity. The minimum data rate depends on the disparity of the used data pattern. For example, a regular clock signal (1-0 sequence) can be transmitted down to a data rate as low as 1 Mbit/s.

[3] Source current.

[4] Sink current.

[5] Data input stage.

Transmitter Electro-Optical Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Optical Rise Time[1)]	t_R			200	ps
Optical Fall Time[1)]	t_F			200	ps
Total Jitter[2), 3)]	TJ			0.284	UI
Deterministic Jitter[3), 4)]	DJ			0.1	UI
Channel-to-channel skew[5)]	t_{CSK}			100	ps
Launched Average Power[6)]	P_{AVG}	–8.0	–5.0	–3.0	dBm
Launched Power Shutdown	P_{SD}			–30.0	dBm
Center Wavelength[7)]	λ_C	830	850	860	nm
Spectral Width (rms)[8)]	$\Delta\lambda$		0.35	0.65	nm
Relative Intensity Noise[9)]	RIN			–117	dB/Hz
Extinction Ratio (dynamic)	ER	6.0			dB
Optical Modulation Amplitude[10), 11)]	OMA	0.19[12)]	0.46[13)]		mW
Eye mask compliance		GBE			

Electro-optical parameters valid for each channel and measured at the highest specified data rate.
All optical parameters are measured with a 62.5 µm multimode fiber.

1) 20% - 80% level, non filtered values.
2) The Total Jitter (TJ) is composed of Random Jitter (RJ) and Deterministic Jitter (DJ) according to:
TJ = RJ (14 Sigma value) + DJ.
The TJ is specified at a BER of 10^{-12} from TP1 to TP2 according to IEEE 802.3, sec. 38.5.
The RJ is measured at the 50% level of the optical signal as the mean of the rising and falling edge measurement value.
3) UI (Unit Interval) is equal to the length of one bit. For example, 2.72 Gbit/s corresponds to 368 ps.
4) The DJ consists of Duty Cycle Distortion and Data Dependent Jitter and is measured according to IEEE 802.3 using a K28.5 pattern.
5) With input channel-to-channel skew 0 ps and a maximum data channel-to-channel average deviation and swing deviation of 5%.
6) The specified output power is compliant with IEC 60825-1, Amendment 2, Class 1M Accessible Emission Limits (AEL).
7) Wavelength is measured according to IEEE 802.3, sec. 38.6.1.
8) Spectral width is measured according to IEEE 802.3, sec. 38.6.1.
9) RIN is measured according to IEEE 802.3, sec. 38.6.4.
10) Peak to peak values.
11) OMA is defined as the difference of the optical high state ('1') and the optical low state ('0'):
OMA = P_{opt}('1') – P_{opt}('0').
12) Corresponds to a minimum extinction ratio of 6 dB.
13) Corresponds to a typical extinction ratio of 8 dB.

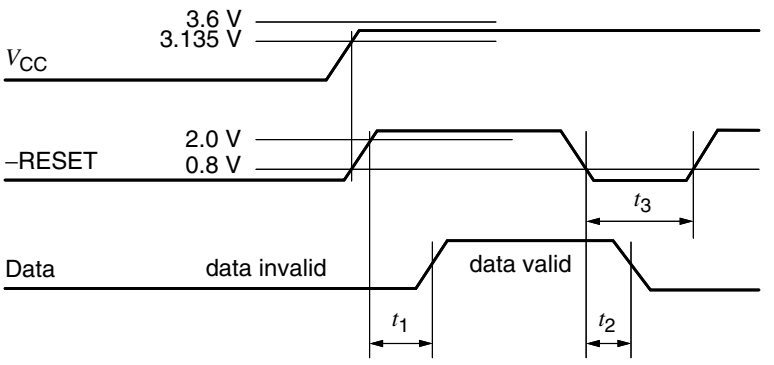


Figure 12 Timing Diagram

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
–RESET on delay time	t_1		15	50	ms
–RESET off delay time	t_2		100	500	ns
–RESET low duration[1)]	t_3	10			µs

[1)] Only when not used as power on reset. At any failure recovery, –RESET must be brought to low level for at least t_3.

Receiver Electrical Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Supply Current[1)]	I_{CC}		170 +15 I_{out}	200 +15 I_{out}	mA
Power Consumption[1), 2)]	P		0.7	0.9	W
Data Output Rise/Fall Time[3)]	$t_{R\text{-}DO}$, $t_{F\text{-}DO}$			250	ps
LVCMOS Output Voltage Low	$V_{LVCMOSOL}$			400	mV
LVCMOS Output Voltage High	$V_{LVCMOSOH}$	2500			mV
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	–100		100	µA
LVCMOS Output Current High[4)]	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output Current Low[5)]	$I_{LVCMOSOL}$			4.0	mA
Total Jitter[6), 7), 8), 9), 10)]	TJ			0.33	UI
Deterministic Jitter[6), 9), 11)]	DJ			0.08	UI
Channel-to-channel skew[12)]	t_{CSK}			100	ps

1) Typical value is measured at T_{case} = 45°C and 3.3 V, maximum value is measured at T_{case} = 80°C and 3.6 V.
2) Calculated for I_{out} = 3 mA.
3) Measured between 20% and 80% level. Maximum value is related to a maximum RC load time constant of t_{RC} = 150 ps.
4) Source current.
5) Sink current.
6) With no optical input jitter.
7) Measured with an optical input power of 3 dB above minimum receiver sensitivity.
8) Unused channels shall be terminated by 50 Ω.
9) UI (Unit Interval) is equal to the length of one bit. For example, 2.72 Gbit/s corresponds to 368 ps.
10) The Total Jitter (TJ) is the sum from Random Jitter (RJ) and Deterministic Jitter (DJ) according to:
TJ = RJ (14 Sigma value) + DJ.
The TJ is specified at a BER of 10^{-12} from TP3 to TP4 according to IEEE 802.3, sec. 38.5.
The RJ is measured at the 50% level of the optical signal as the mean of the rising and falling edge RJ measurement value.
11) The DJ consists of Duty Cycle Distortion and Data Dependent Jitter and is measured according to IEEE 802.3 using a K28.5 pattern.
12) With input channel-to-channel skew 0 ps.

Receiver Electro-Optical Characteristics

Parameter	Symbol	Values		Unit
		min.	max.	
Data Rate Per Channel	DR	500[1)]	1250	Mbit/s
Sensitivity (Average Power)[2)]	P_{IN}		–16.0	dBm
Optical Modulation Amplitude[3)]	OMA	0.030[4)]		mW
Saturation (Average Power)[5)]	P_{SAT}	–2.0		dBm
Signal Detect Assert Level[6)]	P_{SDA}		–17.0	dBm
Signal Detect Deassert Level[6)]	P_{SDD}	–27.0		dBm
Signal Detect Hysteresis[6)]	$P_{SDA} - P_{SDD}$	1.0	4.0	dB
Return Loss of Receiver [7)]	ORL	12		dB

Electro-optical parameters valid for each channel and measured at the highest specified data rate.
All optical parameters are measured with a 62.5 µm multimode fiber.

1) Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity. The minimum data rate depends on the disparity of the used data pattern. For example, a regular clock signal (1-0 sequence) can be received down to a data rate as low as 6 Mbit/s.

2) Sensitivity is measured for BER = 10^{-12} with a Pseudo Random Bit sequence of length 2^{23}–1 (PRBS23) and a test pattern source with RIN of –117 dB/Hz or better. Sensitivity is specified for the worst case extinction ratio and maximum cross talk possibility. The maximum crosstalk possibility is defined as the “victim” receiver channel operating at its sensitivity limit and the neighboring channels operating at 6 dB higher incident optical power.

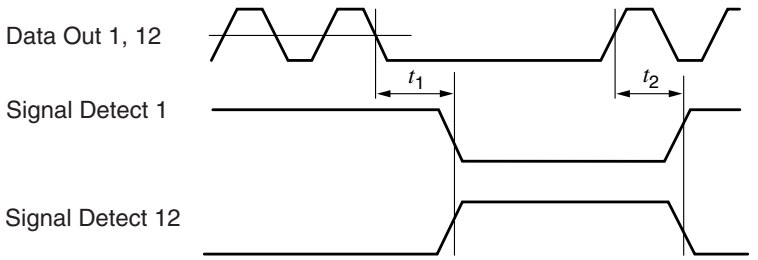
3) Peak to peak value.

4) Corresponds to a maximum sensitivity (average power) of –16 dBm at an extinction ratio of 6 dB.

5) Saturation is specified with a Pseudo Random Bit sequence of length 2^{23}–1 (PRBS23) and ER ≥ 6 dB.

6) P_{SDA}: Average optical power when SD switches from inactive to active.
P_{SDD}: Average optical power when SD switches from active to inactive.

7) Return loss is specified as the ration of the received optical power to the reflected optical power back into the link fiber.



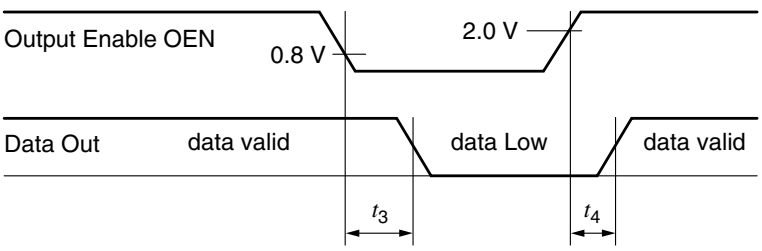


Figure 13 Timing Diagrams

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Signal Detect Deassert Time	t_1		3	10	µs
Signal Detect Assert Time	t_2		2	10	µs
Output Enable off Delay Time	t_3		14	20	µs
Output Enable on Delay Time	t_4		18	20	µs

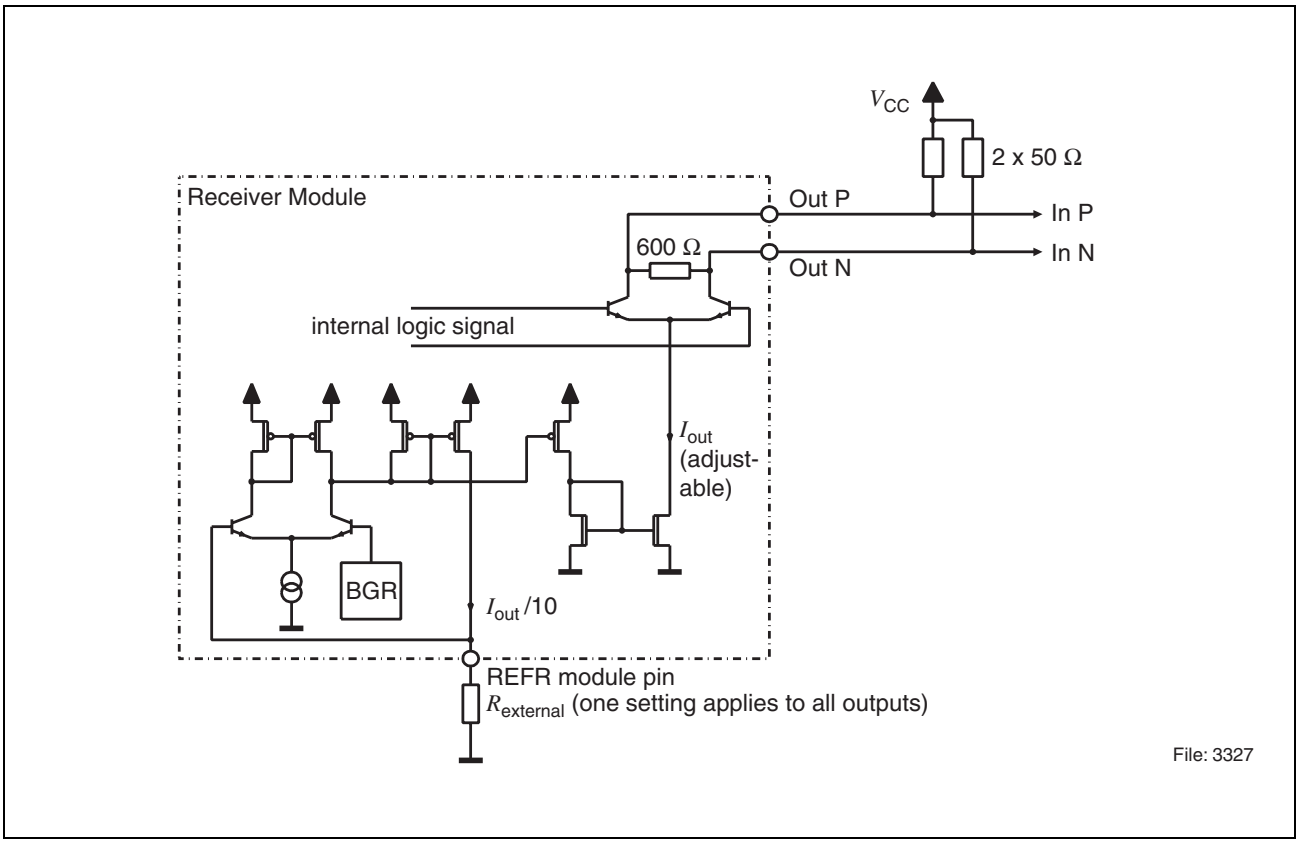
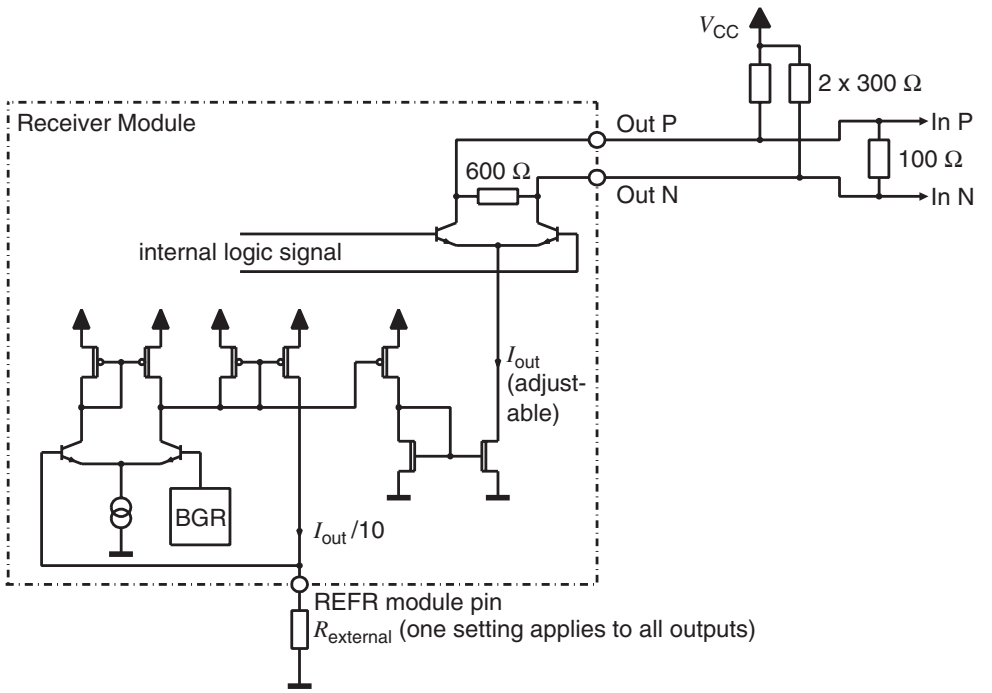


Figure 14 Interfacing to CML



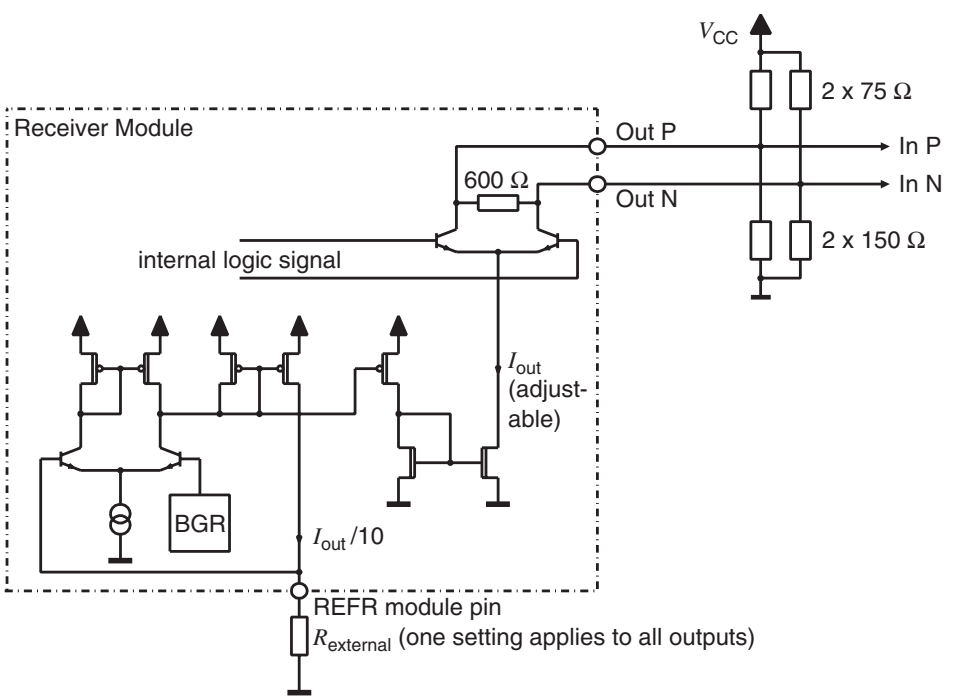


Figure 15 Interfacing to LVPECL

Host Face-Plate Layout for Panel Accessed Modules

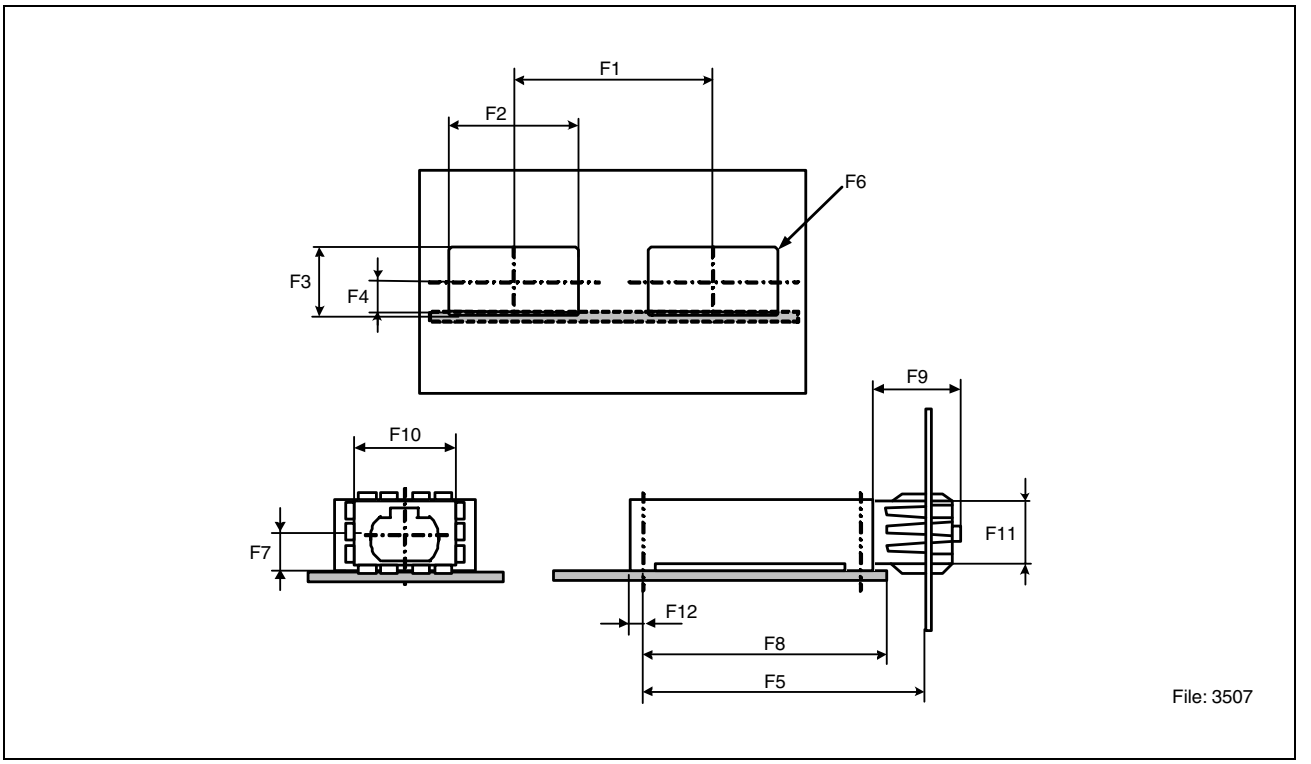


Figure 16

Key	Values			Unit	Comments
	min.	typ.	max.		
F1	18.42	20		mm	Cutout center spacing
F2	16.7	16.8	16.9	mm	Cutout width
F3	9.1	9.2	9.3	mm	Cutout height
F4	4.42	4.52	4.62	mm	Center of cutout and center of receptacle to top of PCB
F5	44.5		46	mm	Face-plate placement
F6			1	mm	Radius
F7		4.25		mm	Opt. reference plane to top of PCB
F8			38	mm	Limitation for PCB length
F9		16.8		mm	Length of receptacle
F10	15.3			mm	Including shield, without spring contacts
F11	7.6				Including shield, without spring contacts
F12		1.7		mm	See Package Outlines **Figure 18** on **Page 31**

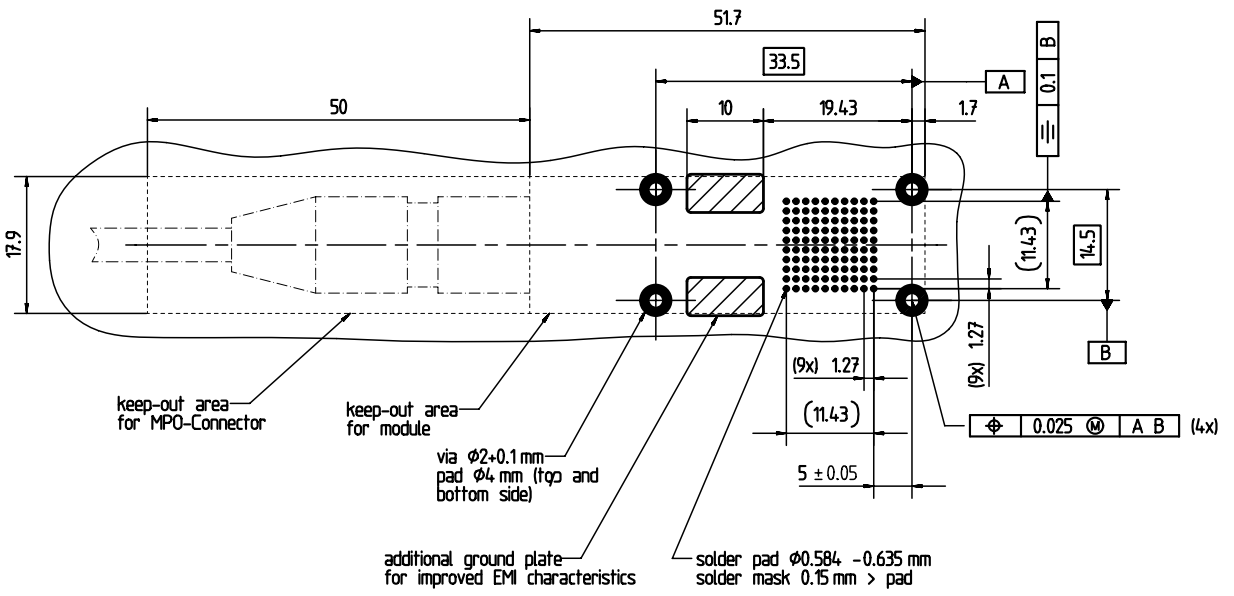


Figure 17 PCB Layout

1. **Figure 17** describes the recommended customer board layout for the PAROLI 2 modules.
2. The holes for the screwing leads and ground plates must be tied to signal ground.
3. Modules must be screwed on the 4 indicated positions (tightening torque should be typically 10 cNm).
4. Screw size for PCB or heat sink mounting = M1.6.
5. Screw length (PCB mounting) = PCB thickness + $5.2_{-0.5}$ mm.
6. Screw length (heat sink mounting) = heat sink thickness + $3.1_{-0.5}$ mm.
7. Modules can be mounted directly side by side.
8. The dashed lines in **Figure 17** indicate the typical keep out area for straight MPO connectors as well as for the module MPO receptacle in case of central board placement of the module.

Thermal Characteristics

The thermal behaviour of PAROLI modules (transmitter and receiver) depends on the operating conditions for different applications.

The following table gives a guideline for system designers.

The thermal resistance R_{th} ($R_{th} = \frac{T_{case} - T_{ambient}}{P_{el}}$; P_{el} = electrical power consumption)

can be used for calculating the module case temperature under different operating conditions and is displayed for two different module options:

a) Baseplate module without heat sink.
b) Baseplate module with customer designed heat sink
(e.g. height = 9 mm, length = 41 mm, width = 18 mm, no. of cooling fins = 9).

Air Velocity[1)]	**0 m/s**	**1.5 m/s**	**3 m/s**	**4 m/s**	**Unit**
R_{th} - Option a)	23.3	10.3	8.6	7.5	K/W
R_{th} - Option b)	20.0	5.2	4.2	4.0	K/W

[1)] The air velocity is applied along the shortest side of the module in parallel to the direction of the heat sinks.

Link Length

The link length calculations are based on the most conservative assumption of PAROLI modules working on their worst case specification limits. Multimode fibers of different types (modal bandwidth at 850 nm) are shown. The stated link length is valid under all specified operating conditions and includes 2 dB of additional connector loss.

Fiber Type Diameter Core/Cladding [µm]	**Modal Bandwidth** [MHz*km]	**Link Distance at 0.5 Gbit/s** [m]	**Link Distance at 1.25 Gbit/s** [m]
62.5 / 125	200	850	360
62.5 / 125	400	1300	640

Channel Description

Transmitter Module

(front view as looking into the MPO connector receptacle of the module)

Ch 12	Ch 11	Ch 10	Ch 9	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1

Host PCB below

Receiver Module

(front view as looking into the MPO connector receptacle of the module)

Ch 12	Ch 11	Ch 10	Ch 9	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1

Host PCB below

The MPO connector provides a keying functionality, which requires a 180 degree twist of fiber cable, if used as a direct connection between transmitter and receiver module. (For example the transmitter channel 1 is directly connected to the receiver cannel 1).

Handling Instructions

Washing Process

The PAROLI mating BGA connector can be handled according to standard industry wave solder, hand solder and washing processes.

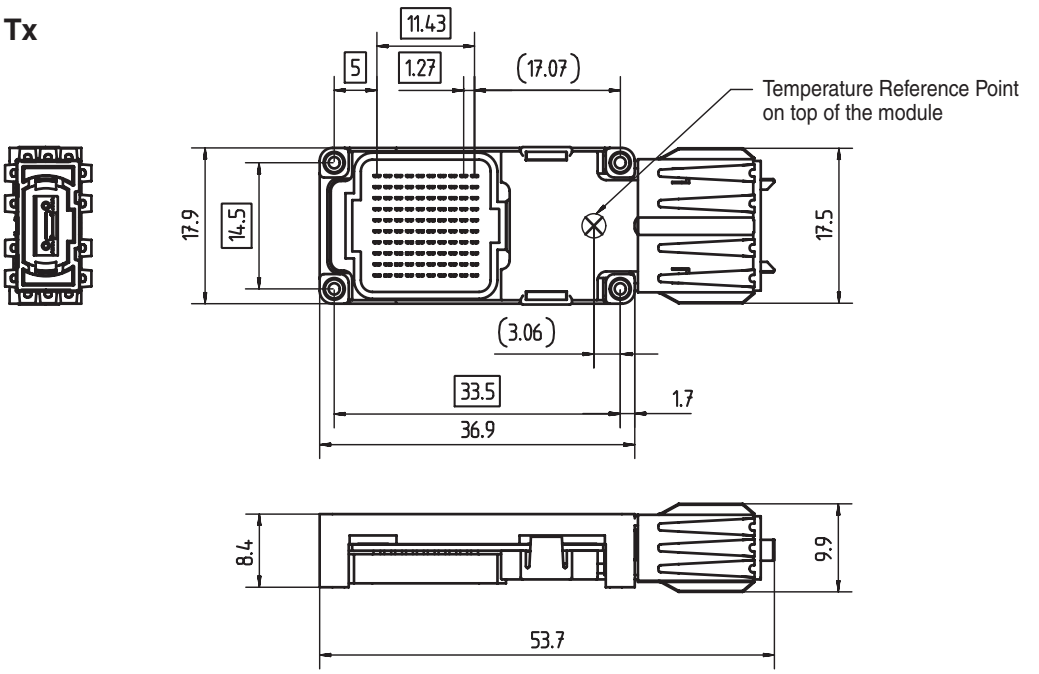
The PAROLI modules shall not be washed, due to possible influence on module performance.

Dust Cover

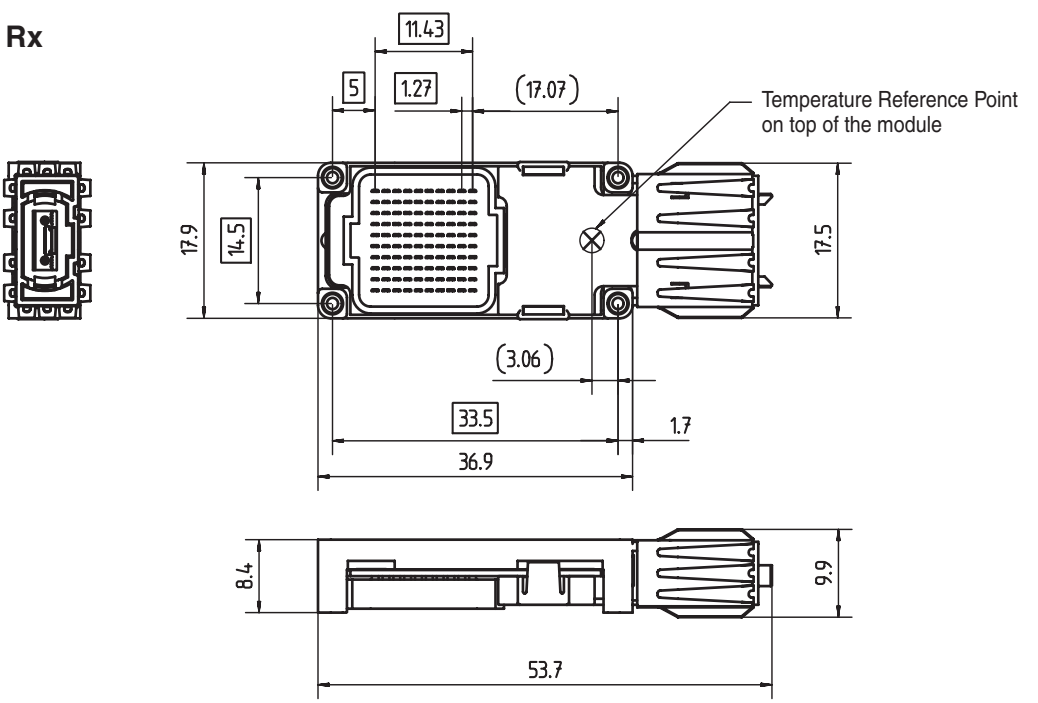
The optical connector is provided with a dust cover, which protects the optical interface from potential damage and contamination from dust during handling. The dust cover should always remain in the module, when no connector is used.

Package Outlines

PAROLI 2 Tx



PAROLI 2 Rx



Typical module mass approximately 10.4 grams
The front collar EMI shield is electrically separated from module signal ground

Dimensions in mm

File: 3203

Figure 18

Ordering Information

Part Number	Description
V23832-T2531-M101	PAROLI Transmitter, 12 x 1.25 Gbit/s, multistandard electrical interface
V23832-T2131-M101	PAROLI Transmitter, 12 x 1.6 Gbit/s, multistandard electrical interface
V23832-T2431-M101	PAROLI Transmitter, 12 x 2.7 Gbit/s, multistandard electrical interface
V23832-T2331-M101	PAROLI Transmitter, 12 x 3.125 Gbit/s, multistandard electrical interface
V23832-R521-M101	PAROLI Receiver, 12 x 1.25 Gbit/s, LVDS electrical interface
V23832-R121-M101	PAROLI Receiver, 12 x 1.6 Gbit/s, LVDS electrical interface
V23832-R421-M101	PAROLI Receiver, 12 x 2.7 Gbit/s, LVDS electrical interface
V23832-R321-M101	PAROLI Receiver, 12 x 3.125 Gbit/s, LVDS electrical interface
V23832-R511-M101	PAROLI Receiver, 12 x 1.25 Gbit/s, CML electrical interface
V23832-R111-M101	PAROLI Receiver, 12 x 1.6 Gbit/s, CML electrical interface
V23832-R411-M101	PAROLI Receiver, 12 x 2.7 Gbit/s, CML electrical interface
V23832-R311-M101	PAROLI Receiver, 12 x 3.125 Gbit/s, CML electrical interface

V23832-T2531-M101
V23832-R511-M101

Revision History:	**2003-11-19**	DS2
Previous Version:	2003-05-21	

Page	**Subjects (major changes since last revision)**
	Document completely revised

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