2W STEREO AUDIO POWER AMPLIFIER WITH SHUTDOWN AA4003

General Description

The AA4003 is a Class AB stereo Audio Power Amplifier which can deliver 2.0W into 4Ω speakers with limitation of THD+N less than 1%. The chip is designed specially for Portable DVD player, Portable Media Player, LCD monitor and Digital Photo Frame applications.

AA4003 is available in package of SOIC-16 and TSSOP-20 (EDP).

Features

- Output Power,
  BTL: 2.0W/CH (4Ω, THD+N≤1%)
  SE: 160mW/CH (16Ω, THD+N≤1%)
- Supply Voltage Range: 2.7V to 5.5V
- External Feedback Loop for Flexible Gain Set-up
- Low Power Consumption at Shutdown Mode 0.7μA Typical
- SE, BTL Mode Switchable
- Optimized Click/POP Noise Suppression
- Thermal Shutdown Protection

Applications

- Portable DVD Player
- Portable Media Player
- LCD Monitor
- Digital Photo Frame

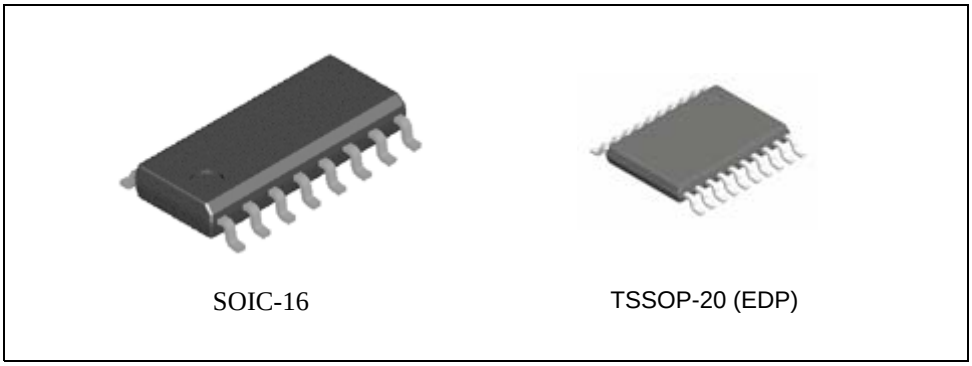
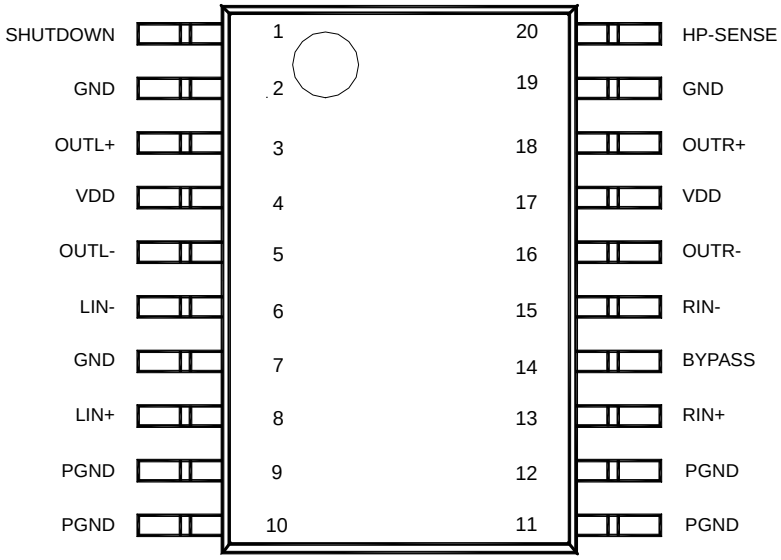


Figure 1. Packages Type of AA4003

Pin Configuration

G Package
(TSSOP-20 (EDP))



M Package
(SOIC-16)

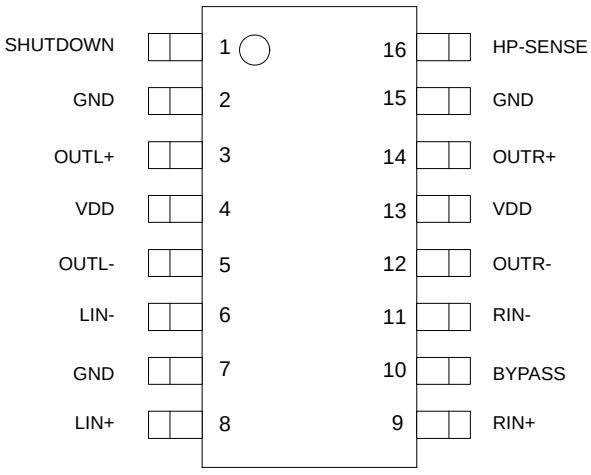
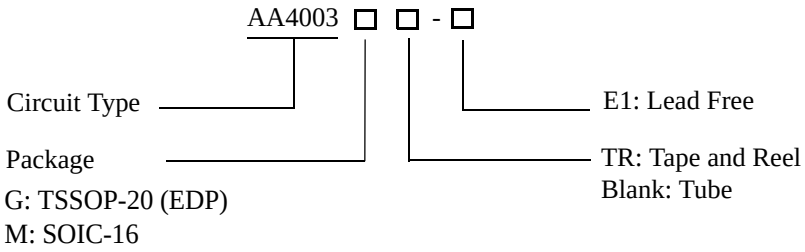


Figure 2. Pin Configurations of AA4003 (Top View)

Pin Description

Pin Number		Pin Name	Function
G Package	M Package		
1	1	SHUTDOWN	Shutdown mode enable pin, active High
2, 7, 19	2, 7, 15	GND	Signal ground
3	3	OUTL+	Left channel positive output
4, 17	4, 13	VDD	Power supply pin
5	5	OUTL-	Left channel negative output
6	6	LIN-	Left channel negative input
8	8	LIN+	Left channel positive input
9, 10, 11, 12		PGND	Power ground, used for thermal release
13	9	RIN+	Right channel positive input
14	10	BYPASS	Internal reference voltage pin, connect a 1.0μF capacitor to GND
15	11	RIN-	Right channel negative input
16	12	OUTR-	Right channel negative output
18	14	OUTR+	Right channel positive output
20	16	HP-SENSE	SE, BTL Mode switch pin, L – BTL Mode H – SE Mode

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
TSSOP-20 (EDP)	-40 to 85 ℃	AA4003G-E1	AA4003G-E1	Tube
		AA4003GTR-E1	AA4003G-E1	Tape & Reel
SOIC-16	-40 to 85 ℃	AA4003M-E1	AA4003M-E1	Tube
		AA4003MTR-E1	AA4003M-E1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "E1" suffix in the part number, are RoHS compliant.

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value		Unit
Supply Voltage	V_{DD}	6		V
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3		V
Power Dissipation	P_D	Internally limited		
Package Thermal Resistance	$R_{\theta JA}$	M Package	90	$^oC/W$
		G Package	50 (Note 2)	
Operating Junction Temperature	T_J	150		^oC
Storage Temperature Range	T_{STG}	-65 to 150		^oC
Lead Temperature 1.6mm from Case for 10 Seconds	T_{LEAD}	260		^oC
ESD (Human Body Model)		2000		V
ESD (Machine Model)		300		V

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operation is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Note 2: Chip is soldered to 200mm^2 copper (top side solder mask) of 1oz. on PCB with 8 x 0.5mm vias..

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	2.7	5.5	V
Operating Ambient Temperature	T_A	-40	85	^oC

Electrical Characteristics

(V_{DD}=5V, T_A=25°C, C_I=1μF, C_{OUT}=220μF and R_I=R_F=20kΩ unless otherwise specified. For SE Mode, HP_SENSE=5V, for BTL Mode, HP_SENSE=0V.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Current	I_{DD}	SE Mode, V_{IN}=0, I_O=0		3	10	mA
		BTL Mode, V_{IN}=0, I_O=0		6	20	
Shutdown Current	I_{SD}	$V_{SHUTDOWN}$=5V		0.7	2.0	μA
HP_SENSE LOGIC	V_{IH}		4			V
	V_{IL}				0.8	V
SHUTDOWN LOGIC	V_{IH}		3			V
	V_{IL}				0.8	V
Thermal Shutdown Temperature				170		°C
Hysteresis Temperature Window				25		°C
SE Mode						
Output Power	P_O	THD+N=1%, R_L=32Ω		80		mW
		THD+N=10%, R_L=32Ω		110		
		THD+N=1%, R_L=16Ω		160		
		THD+N=10%, R_L=16Ω		220		
Total Harmonic Distortion + Noise	THD+N	P_O=75mW, R_L=32Ω,		0.2		%
Signal to Noise Ratio	SNR	P_O=75mW, R_L=32Ω,		90		dB
Crosstalk	X_{TALK}	P_O=75mW, R_L=32Ω, f=1kHz		-80		dB
Power Supply Rejection Ratio	PSRR	C_b=1μF, f=1KHz, V_{RIPPLE}=0.2VRMS, R_L=16Ω		60		dB
BTL Mode						
Output Offset Voltage	V_{OS}	V_{IN}=0V, No load		± 5	± 50	mV
Output Power	P_O	THD+N=1%, R_L=4Ω		2		W
		THD+N=10%, R_L=4Ω		2.5		
		THD+N=1%, R_L=8Ω		1.1		
		THD+N=10%, R_L=8Ω		1.5		
Total Harmonic Distortion + Noise	THD+N	P_O=1W, R_L=4Ω,		0.1		%
Signal to Noise Ratio	SNR	P_O=1W, R_L=8Ω,		95		dB
Crosstalk	X_{TALK}	P_O=1W, R_L=8Ω, f=1kHz		-80		dB
Power Supply Rejection Ratio	PSRR	C_b=1μF, f=1KHz, V_{RIPPLE}=0.2VRMS, R_L=8Ω		67		dB

Typical Performance Characteristics

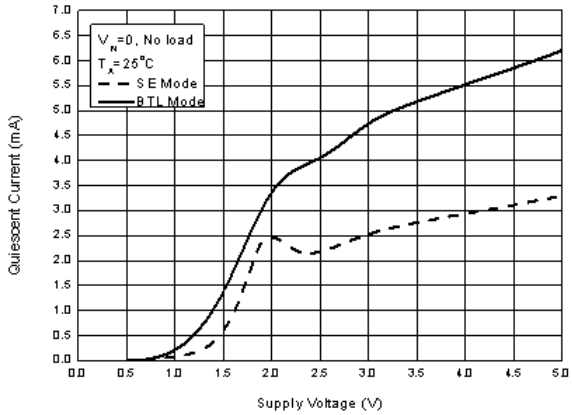


Figure 3. Quiescent Current vs. Supply Voltage

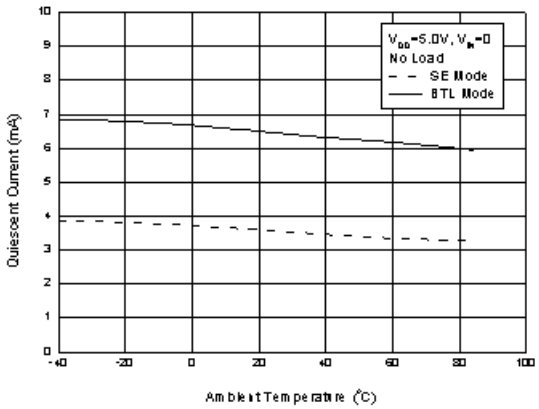


Figure 4. Quiescent Current vs. Ambient Temperature

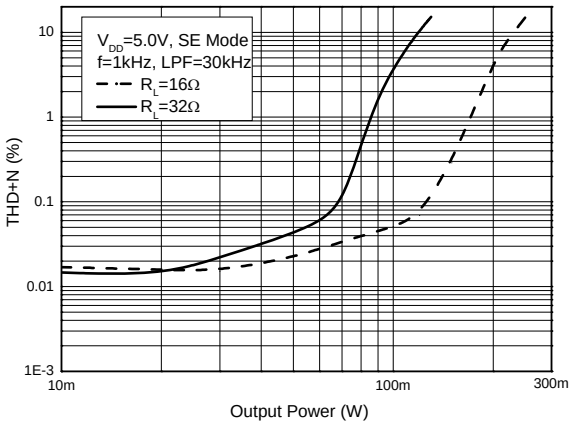


Figure 5. THD+N vs. Output Power
@ SE Mode

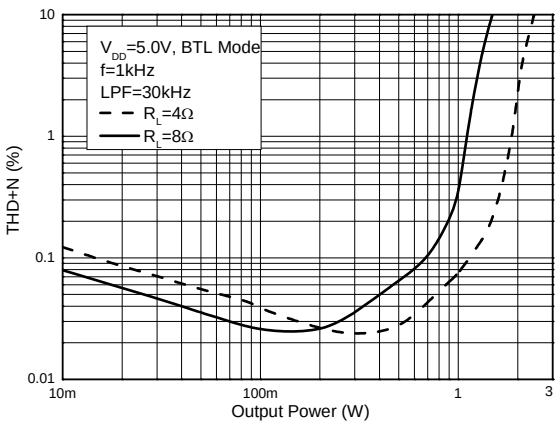


Figure 6. THD+N vs. Output Power
@ BTL Mode

Typical Performance Characteristics

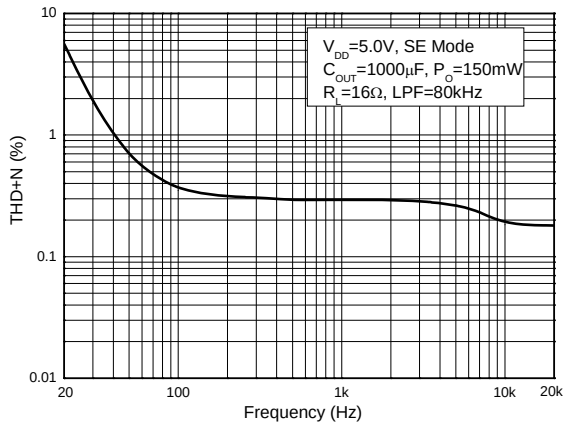


Figure 7. THD+N vs. Output Power
@ SE Mode

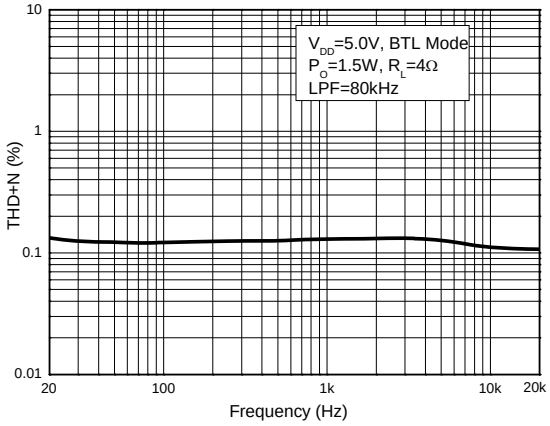


Figure 8. THD+N vs. Output Power
@ BTL Mode

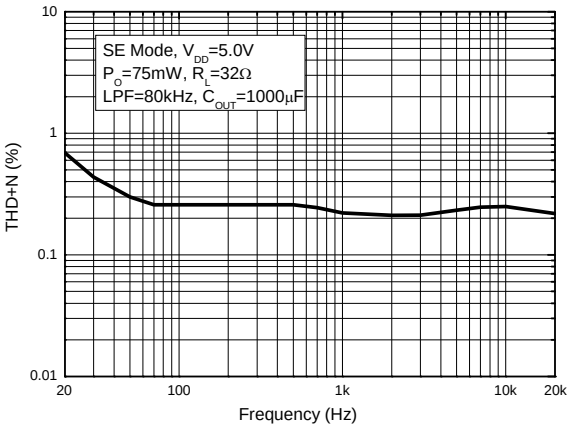


Figure 9. THD+N vs. Frequency
@ SE Mode

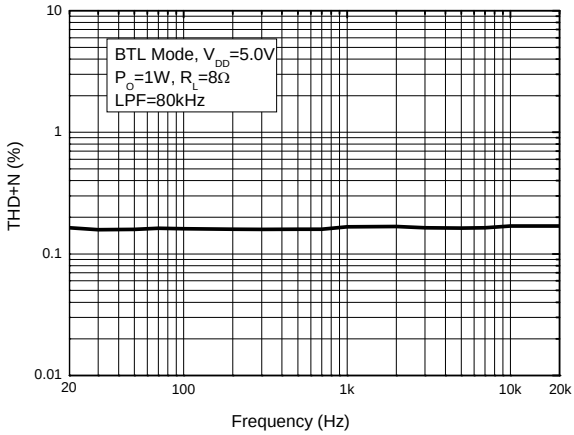


Figure 10. THD+N vs. Frequency
@ BTL Mode

Typical Performance Characteristics (Continued)

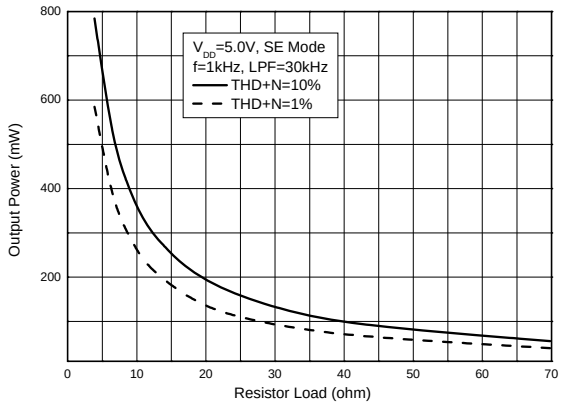


Figure 11. Output Power vs. Resistor Load @ SE Mode

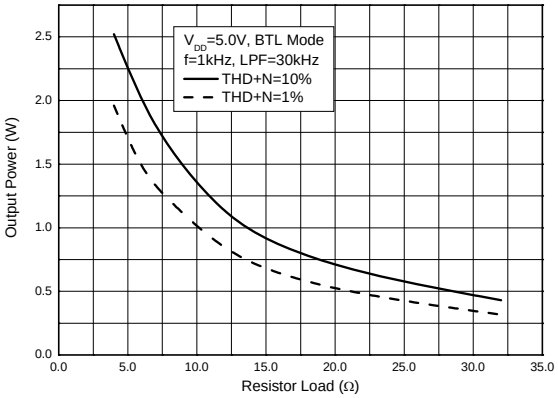


Figure 12. Output Power vs. Resistor Load @ BTL Mode

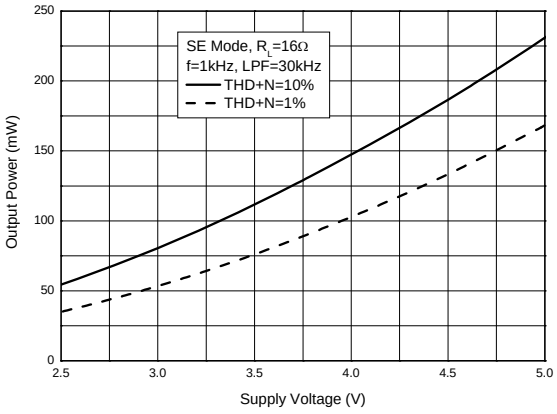


Figure 13. Output Power vs. Supply Voltage @ SE Mode

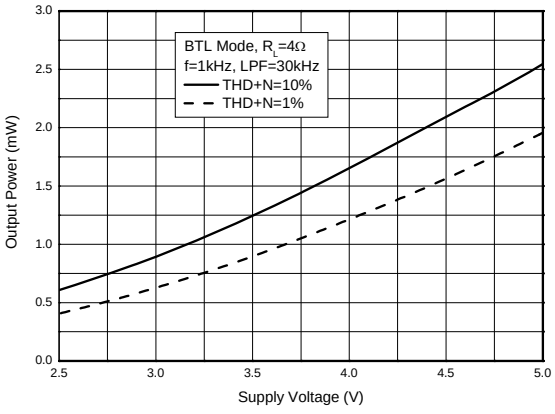


Figure 14. Output Power vs. Supply Voltage @ BTL Mode

Typical Performance Characteristics (Continued)

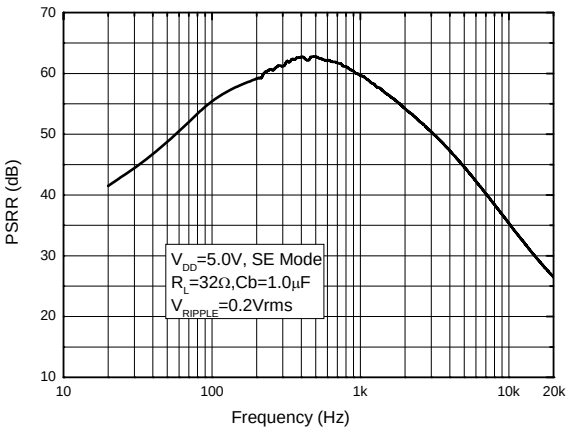


Figure 15. PSRR vs. Frequency
@ SE Mode

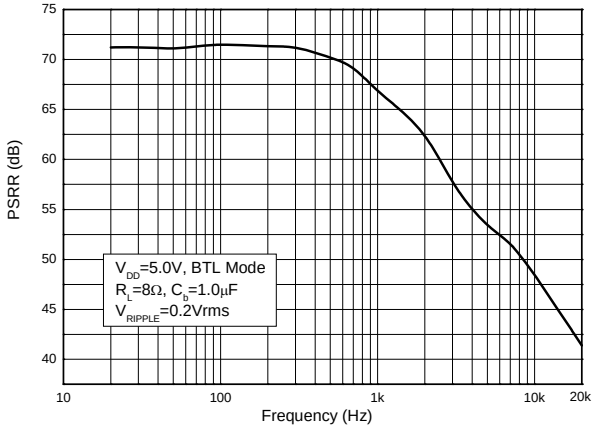


Figure 16. PSRR vs. Frequency
@ BTL Mode

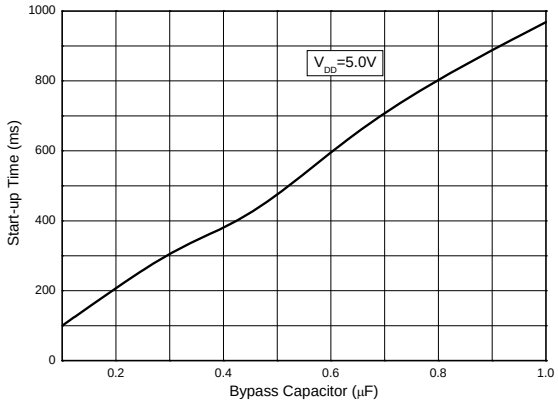


Figure 17. Start-up Time vs. Bypass Capacitor

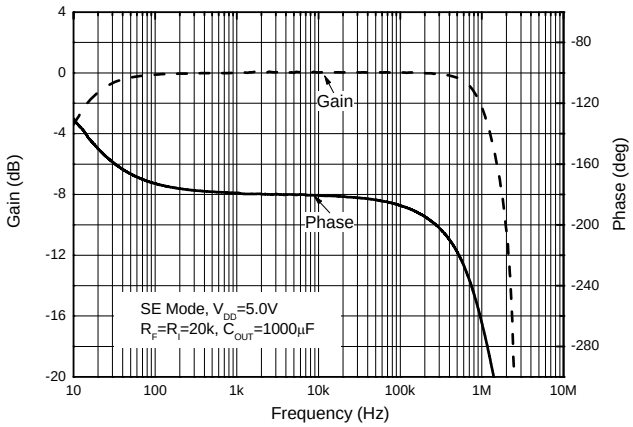


Figure 18. Closed Loop Frequency Response

Application Information

SE/BTL Mode, HP_SENSE Pin

The AA4003 can operate under 2 types of output configuration, BTL (Bridged-Tied-Load) mode and SE (Single-Ended) mode, determined by HP_SENSE pin's logic level. (Here is the discussion about left channel only, it equally applies to right channel.)

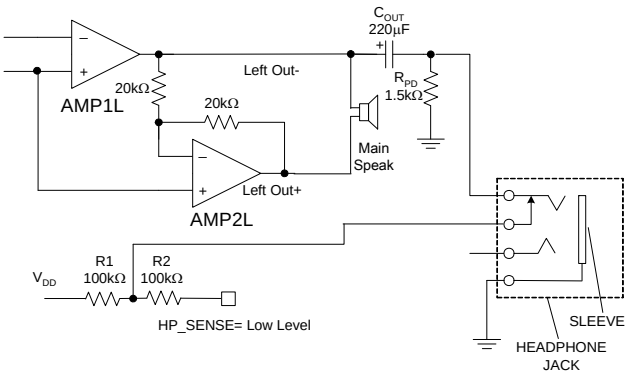


Figure 19. Output Configuration for Left Channel in BTL Mode

When HP_SENSE pin is held low which sets the chip in BTL mode, the AMP2L unit is turned on. AMP2L has fixed unity gain internally, AC signal at OUT+ is 180 degree phase shifted from OUT-. Because the DC component (Output Bias voltage, approx 1/2 V_{DD}) between OUT+ and OUT- is canceled, there is no necessity to use DC block capacitors for main speak. In BTL mode, output voltage swing across main speaker is about 2 times that in SE mode, so there is 4 times output power compared to SE mode with same load and input. (see Figure 19)

If applying high level to HP_SENSE pin which sets the chip in SE mode, the AMP2L unit is in high impedance state. There is no current loop between OUT+ and OUT-, the main speak is naturally disabled without any hardware change. The output audio signal rides on bias voltage at OUT- (Output Bias voltage, approx 1/2 V_{DD}) , so it has to use a capacitor C_{OUT} to block DC bias and couple AC signal to headphone speak. (See Figure 20)

It is recommended to connect HP_SENSE to the headphone jack switch pin illustrated in Figure 19.

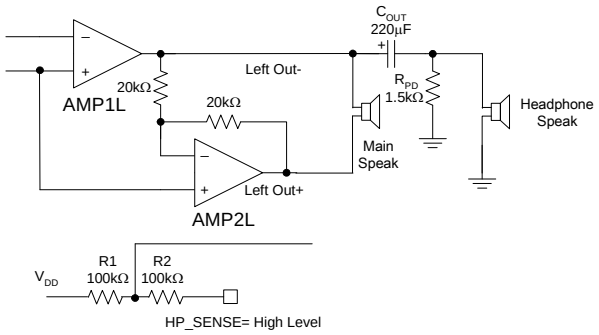


Figure 20. Output Configuration for Left Channel in SE Mode

When headphone plug is not inserted, the voltage of HP_SENSE pin is determined by voltage divider formed by R1 and R_{PD}. For given resistor's value in Figure 19, R1=100kΩ, R_{PD}=1.5kΩ, DC voltage at HP_SENSE is about 74mV. AC signal equals output amplitude of OUT- through C_{OUT}, so signal at HP_SENSE node is 74mV DC plus AC signal. The maximum peak-to-peak voltage at OUT- is no greater than V_{DD} (supply voltage 5.0V), so the positive maximum voltage of HP_SENSE node will be no greater than 2.5V+75mV≈2.575V, which is less than HP_SENSE input high level minimum value (4.0V). That means the chip is in BTL mode and there is no risk of operation mode switch between SE and BTL. When headphone plug is inserted, as the R_{PD} is disconnected from R1, the voltage of HP_SENSE pin is pulled up by R1 to V_{DD} and sets the chip in SE mode.

HP_SENSE pin can also be connected to MCU I/O port to control the mode switch through MCU.

It is necessary to note that AA4003 still can drive headphone even in BTL mode because OUT- is always active whatever the chip is in SE or BTL mode.

C_{IN}, C_{OUT}, Cb and C_S (Power Supply) Selection

For input stages of AA4003, input capacitors C_I is used to accommodate different DC level between input source and AA4003 bias voltage (about 2.31V). Input capacitors C_I and input resistors R_I form a first order High Pass Filter, which determines the lower corner frequency according to the classic equation below,

Application Information (Continued)

$$f_{CIL} = \frac{1}{2\pi R_I * C_I} \quad \text{.....(1)}$$

Similarly, for output stage in SE mode, output capacitor (C_{OUT}), and headphone load also form a first order High Pass Filters, and its cut-off frequency is determined by equation 2.

$$f_{COL} = \frac{1}{2\pi R_{HP} * C_{OUT}} \quad \text{.....(2)}$$

The purpose of bypass capacitor (Cb) is to filter internal noise, reduce harmonic distortion, and improve power supply rejection ratio performance. Tantalum or ceramic capacitor with low ESR is recommended, and it should be placed as close as possible to the chip in PCB layout. The chip will not work until internal DC bias is set up completely. So the size of Cb will also affect the chip start up time, which is approx linearly proportional to the value of bypass capacitor. For AA4003, here are various start-up times for several typical capacitor values. (see Figure 17)

Cb (μF)	Start up Time (ms)
0.33	340
0.47	420
1.0	970

For AA4003 power supply, it is better to use an individual power source generated from voltage regulator split from video, digital circuit units in system. The power supply bypass capacitors, C_S, is recommended to use one low ESR electrolytic capacitor between 4.7μF to 10μF with a parallel 0.1μF ceramic capacitor which is located close to the chip.

Setup Proper Gain, Design Example

The closed loop gain of AA4003 is determined by the ratio of feedback resistor (R_F) to input resistor (R_I).

$$A_V = \frac{R_F}{R_I} \quad \text{.....(3)}$$

Example:

V_{DD}=5V, R_L=8Ω, BTL configuration, Desired output power P_O=1.0W (each channel), THD+N ≤ 1%.
Input signal, V_{IN}=1.0VRMS from D-A converter.

Step 1,

To check if the chip can deliver 1W to 8Ω load with the limitation of THD+N ≤ 1%, V_{DD}=5V. From Figure 6, Figure 12, AA4003 can deliver 1W to 8Ω load each channel.

Step 2,

If yes, to calculate output voltage,

$$V_{OUT} = \sqrt{P_O * R_L} = \sqrt{1*8} = 2.83V_{RMS}$$

So pass-band gain, AV=V_{OUT}/V_{IN}=2.83x.

Step 3,

Assuming input resistor is 20kΩ, the feedback resistor=20kΩ*1.415=28.3kΩ. Select the closest standard value 28kΩ.

Shutdown

AA4003 has a shutdown feature to reduce power consumption. If apply high level to shutdown pin, output amplifiers will be turned off, bias circuit is also disabled, the maximum current drawn from V_{DD} is less than 2.0μA. A logic low level will enable the device.

Optimizing CLICK/POP Noise

The AA4003 includes optimized circuits to suppress CLICK/POP noise during power up/power down transition.

In BTL mode the AA4003 can effectively reduce most common mode signal including CLICK/POP noise.

In SE mode, optimized ramp for rise/fall edge of BIAS can significantly reduce click/pop noise due to charge and/or discharge output capacitor (C_{OUT}). Furthermore, increasing bypass capacitor value (Cb) can slower ramp of charging bypass capacitor, prolong start-up time, mask most of transient noises before bias voltage is set up completely. It is recommended to use 1.0μF capacitor with lower ESR.

Application Information (Continued)

Power Dissipation, Efficiency and Thermal Design Consideration

For Class AB amplifiers, Formula 4 is the basic equation of efficiency worked in BTL configuration,

$$\eta = \frac{\pi V_P}{4V_{DD}} \quad \text{.....(4)}$$

here V_P is output peak voltage across the load.

Thermal dissipation becomes major concern when delivering more output power especially in BTL mode. The maximum power dissipation can be calculated by following equation.

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}} \quad \text{.....(5)}$$

Here T_{JMAX} is maximum operating junction temperature, 150°C, T_A is ambient temperature, θ_{JA} is thermal resistance from junction to ambient, which is 50°C/W for TSSOP-20 (EDP), given in datasheet.

Assuming T_A is 25°C, the maximum power dissipation P_{DMAX} is about 2.5W according to formula 6.

There is an other formula about power dissipation which is determined by supply voltage and load resistance.

$$P_{DBTLMAX} = \frac{2V_{DD}^{\ 2}}{\pi^2 R_L} \quad \text{.....(6)}$$

If power dissipation calculated in an application is larger than that package permitted, there will be a need to assemble an additional heat sink, or keep ambient temperature around the chip low, or increase load resistance, or decrease power supply voltage.

Here is an example. Assuming V_{DD}=5.0V, R_L=4Ω, stereo in BTL mode,

$$P_{DBTLMAX} = \frac{2V_{DD}^{\ 2}}{\pi^2 R_L} = \frac{2\times 5^2}{3.14^2 \times 4} = 1.266W$$

per channel, total power dissipation P_{DTOTAL}=2* $P_{DBTLMAX}$=2.53W. According to formula 6, maximum ambient temperature is,

$$T_A = T_{JMAX} - \theta_{JA} * P_{DBTLMAX} \quad \text{=150-50*2.53=23.5 °C}$$

That is to say, if user wants AA4003 to delivery 2W power per channel to 4Ω load at V_{DD}=5.0V, BTL mode, ambient temperature has to hold lower than 23.5°C. When junction temperature exceeds about 170°C, OTSD feature will be enabled, and shutdown the device to limit total power dissipation.

There is an exposed thermal pad on bottom of the chip to provide the direct thermal path from die to heat sink. It is recommended to use copper on the surface of Printed Circuit Board as heat sink. To dig some matrix regular holes under chip, remove mask of this area copper, and make sure to keep them contact well when soldering on PCB are also recommended. (See Figure 21)

Recommended PCB Layout for AA4003

Using wide traces for power supply to reduce power losses caused by parasitic resistance in all outputs is useful to help releasing heat away from the chip. It is recommended to place bypass capacitor, power supply bypass capacitors as close as possible to the chip. Figure 21 and Figure 22 show the recommended layout for double layer PCB.

Application Information (Continued)

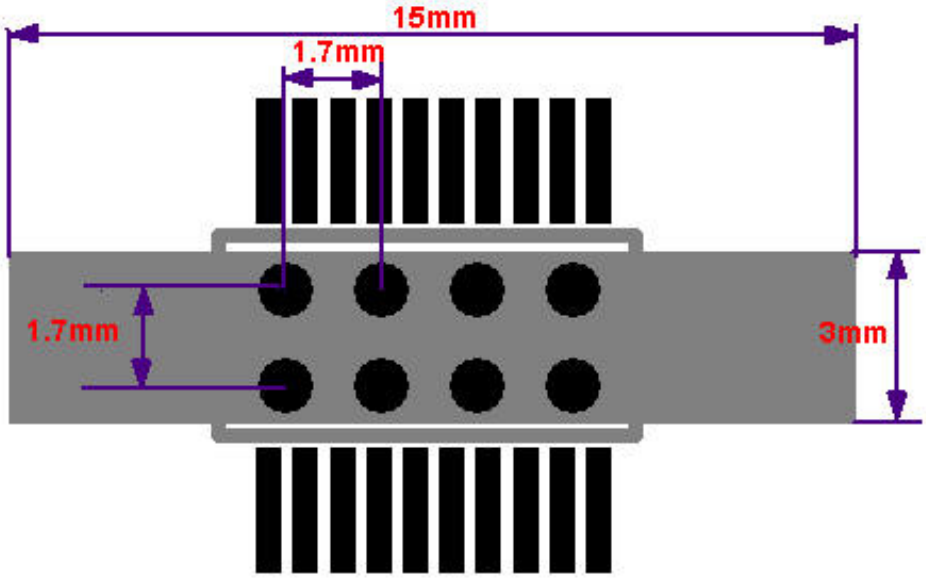


Figure 21. Copper and Holes under Part

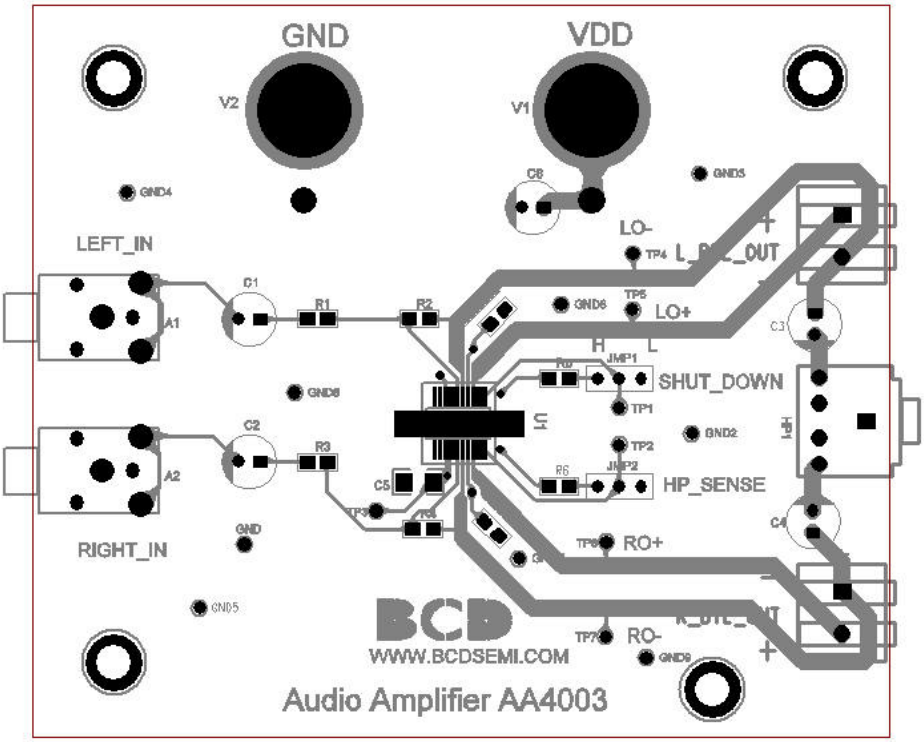


Figure 22. Top Route and Silk Screens

Typical Application

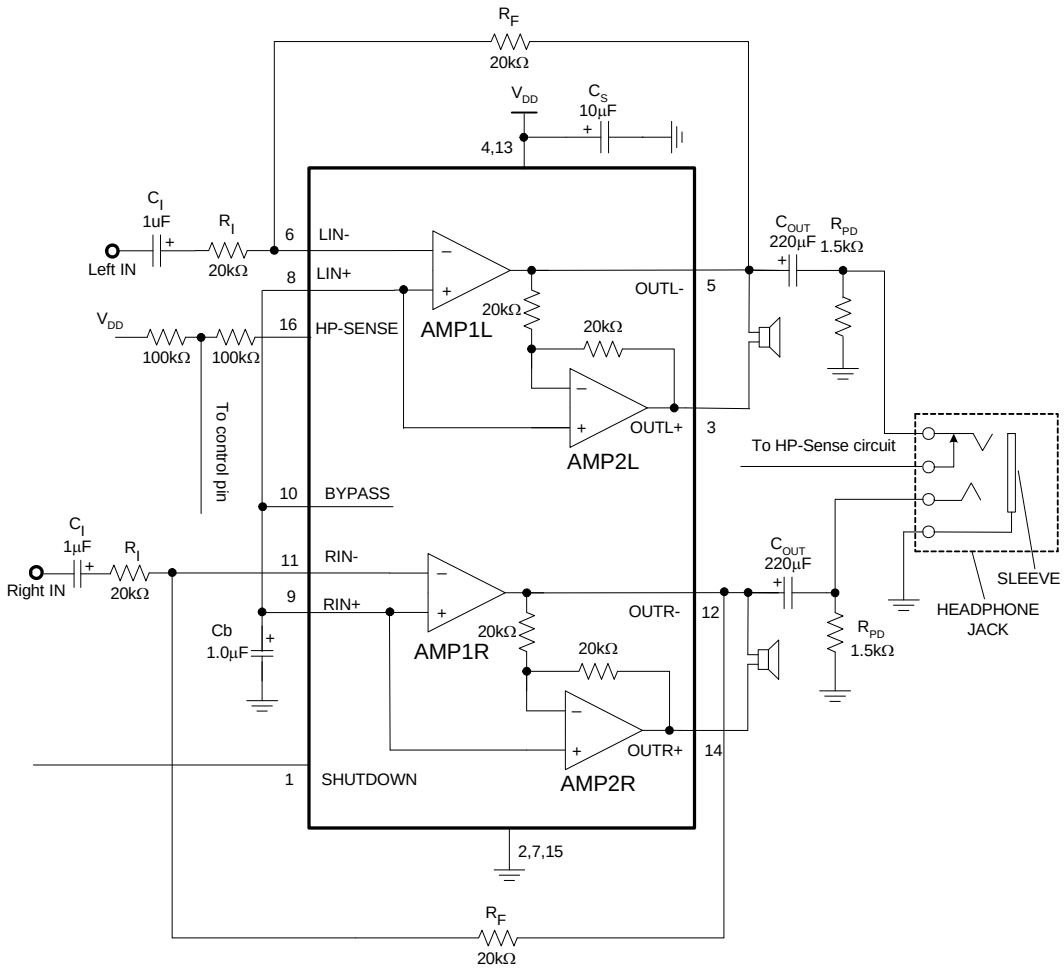
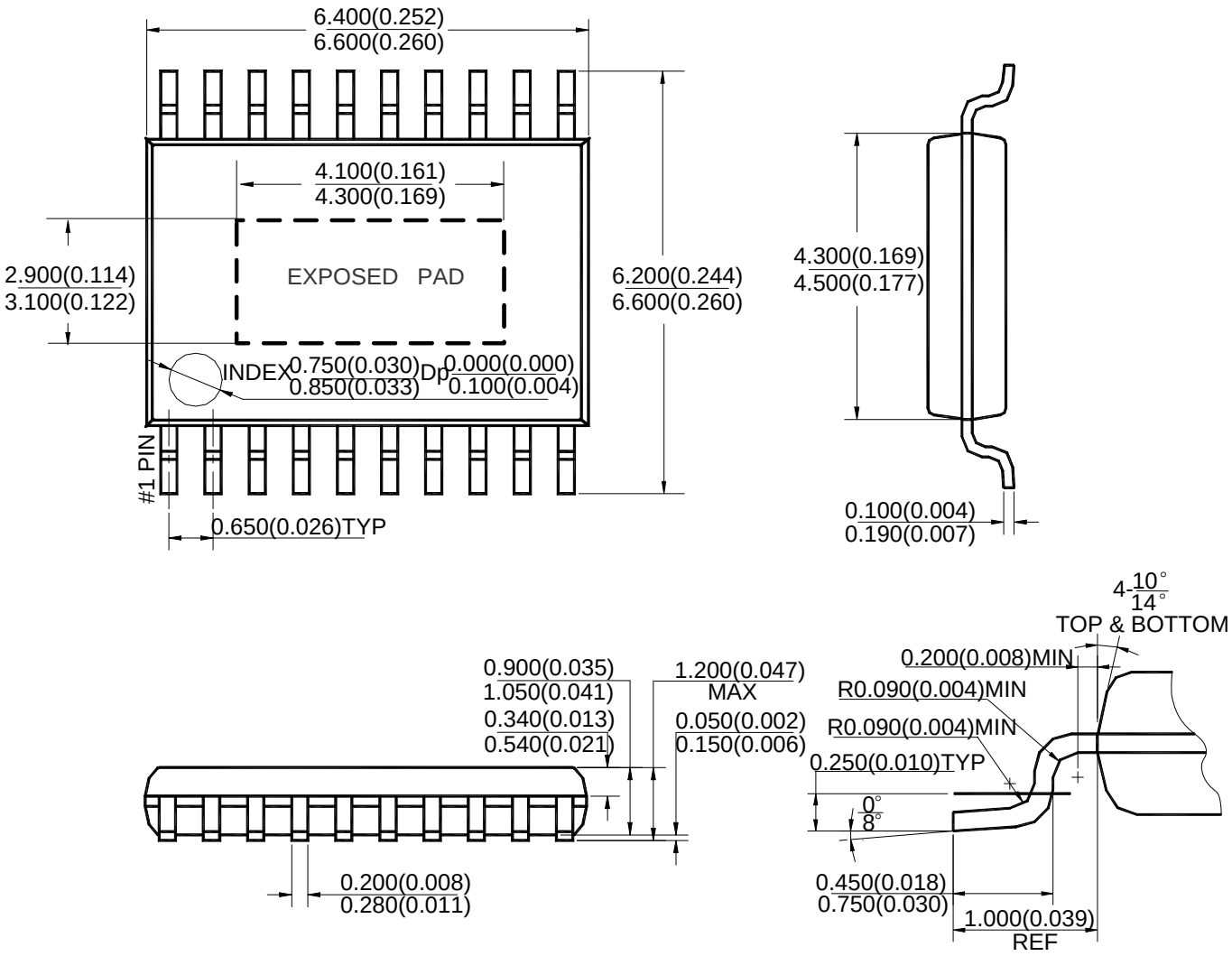


Figure 23. Typical Application Circuit of AA4003 (M Package)

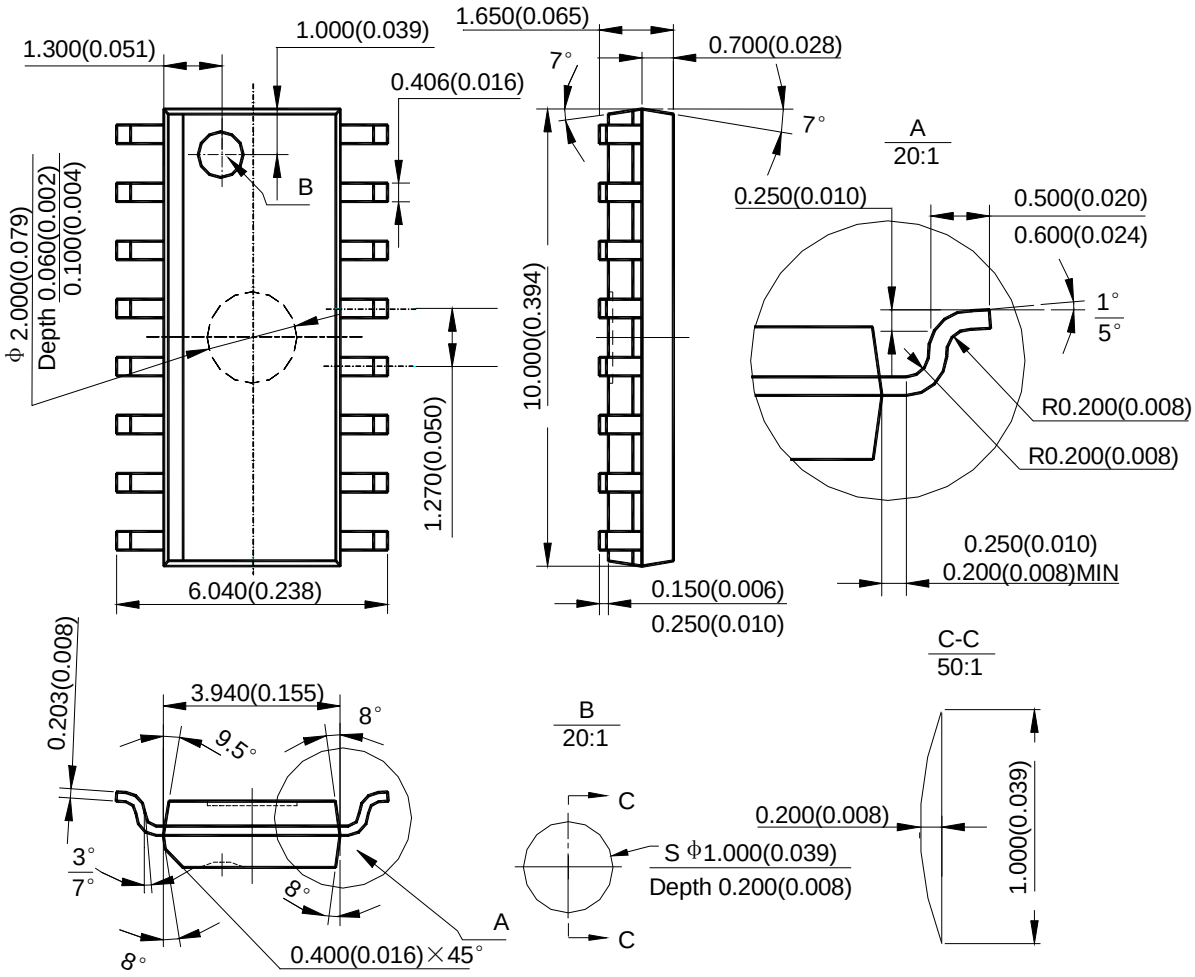
Mechanical Dimensions

TSSOP-20(EDP) **Unit: mm(inch)**



Mechanical Dimensions (Continued)

SOIC-16 **Unit: mm(inch)**



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