Features

- Ultra High Performance
  - System Speeds to 100 MHz
  - Array Multipliers > 50 MHz
  - 10 ns Flexible SRAM
  - Internal Tri-state Capability in Each Cell
- FreeRAM™
  - Flexible, Single/Dual Port, Synchronous/Asynchronous 10 ns SRAM
  - 2,048 - 18,432 Bits of Distributed SRAM Independent of Logic Cells
- 128 - 384 PCI Compliant I/Os
  - 3V/5V Capability
  - Programmable Output Drive
  - Fast, Flexible Array Access Facilitates Pin Locking
  - Pin-compatible with XC4000, XC5200 FPGAs
- 8 Global Clocks
  - Fast, Low Skew Clock Distribution
  - Programmable Rising/Falling Edge Transitions
  - Distributed Clock Shutdown Capability for Low Power Management
  - Global Reset/Asynchronous Reset Options
  - 4 Additional Dedicated PCI Clocks
- Cache Logic® Dynamic Full/Partial Re-configurability In-System
  - Unlimited Re-programmability via Serial or Parallel Modes
  - Enables Adaptive Designs
  - Enables Fast Vector Multiplier Updates
  - QuickChange™ Tools for Fast, Easy Design Changes
- Pin-compatible Package Options
  - Plastic Leaded Chip Carriers (PLCC)
  - Thin, Plastic Quad Flat Packs (LQFP, TQFP, PQFP)
  - Ball Grid Arrays (BGAs)
- Industry-standard Design Tools
  - Seamless Integration (Libraries, Interface, Full Back-annotation) with Concept®, Everest, Exemplar™, Mentor®, OrCAD®, Synario™, Synopsys®, Verilog®, Veribest®, Viewlogic®, Synplicity®
  - Timing Driven Placement & Routing
  - Automatic/Interactive Multi-chip Partitioning
  - Fast, Efficient Synthesis
  - Over 75 Automatic Component Generators Create 1000s of Reusable, Fully Deterministic Logic and RAM Functions
- Intellectual Property Cores
  - Fir Filters, UARTs, PCI, FFT and Other System Level Functions
- Easy Migration to Atmel Gate Arrays for High Volume Production
- Supply Voltage 5V for AT40K, and 3.3V for AT40KLV

5K - 50K Gates Coprocessor FPGA with FreeRAM™

AT40K05
AT40K05LV
AT40K10
AT40K10LV
AT40K20
AT40K20LV
AT40K40
AT40K40LV

Rev. 0896C–FPGA–04/02

Table 1. AT40K/AT40KLV Family[1]

Device	AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV
Usable Gates	5K - 10K	10K - 20K	20K - 30K	40K - 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	256[1]	576[1]	1,024[1]	2,304[1]
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1. Packages with FCK will have 8 less registers.

Description

The AT40K/AT40KLV is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 352-ball Square BGA, and support 5V designs for AT40K and 3.3V designs for AT40KLV.

The AT40K/AT40KLV is designed to quickly implement high-performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC or Sun platform. Atmel's design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar and Viewlogic.

The AT40K/AT40KLV can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40K/AT40KLV FPGA offers a patented distributed 10 ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array and Vector Multipliers

The AT40K/AT40KLV's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40K/AT40KLV's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40K/AT40KLV, AT6000 and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40K/AT40KLV can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40K/AT40KLV FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40K/AT40KLV series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 2,304 registers. Pin locations are consistent throughout the AT40K/AT40KLV series for easy design migration in the same package footprint. The AT40K/AT40KLV series FPGAs utilize a reliable 0.6µ single-poly, CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40K/AT40KLV series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells, see Figure 1. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells, see Figure 2 on page 5. At the intersection of each repeater row and column there is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM[1], with either synchronous or asynchronous operation.

Note: 1. The right-most column can only be used as single-port RAM.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20)

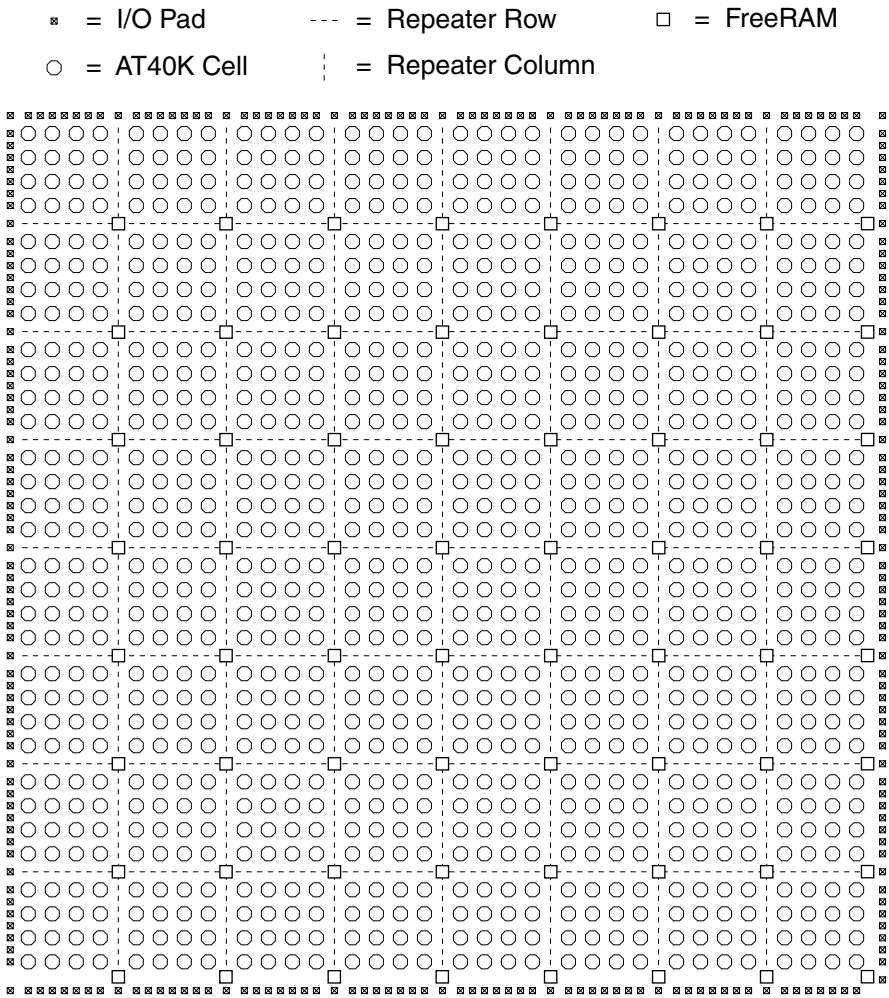
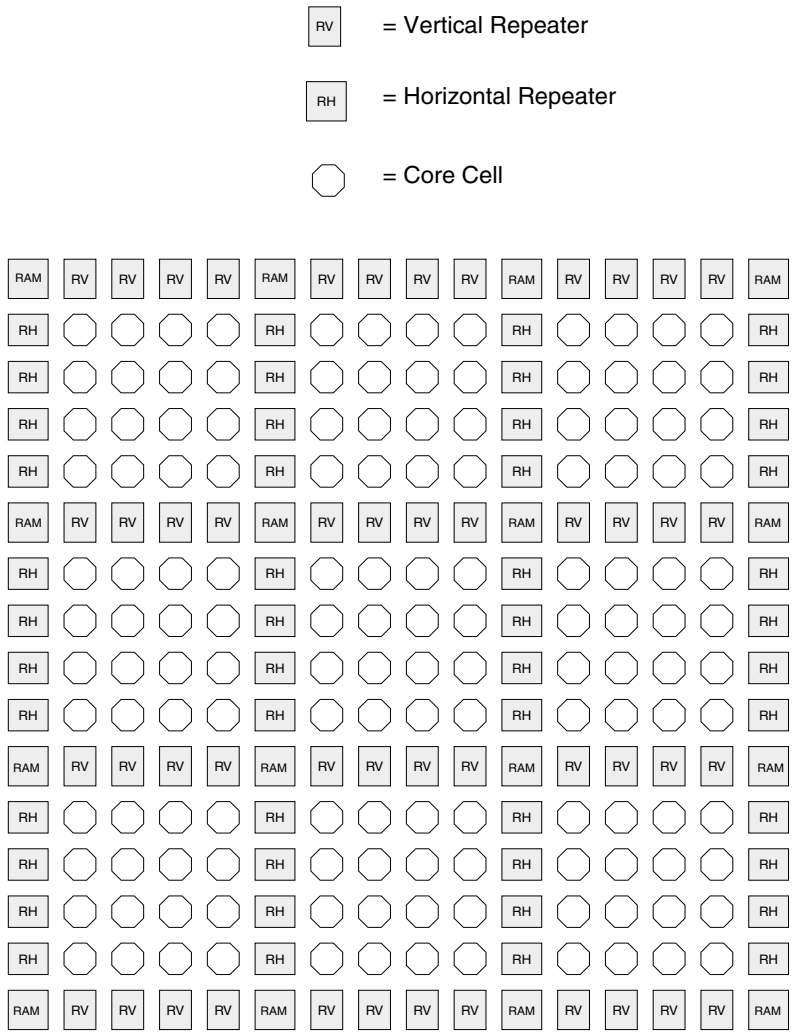


Figure 2. Floor Plan (Representative Portion)[1]



Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

The Busing Network

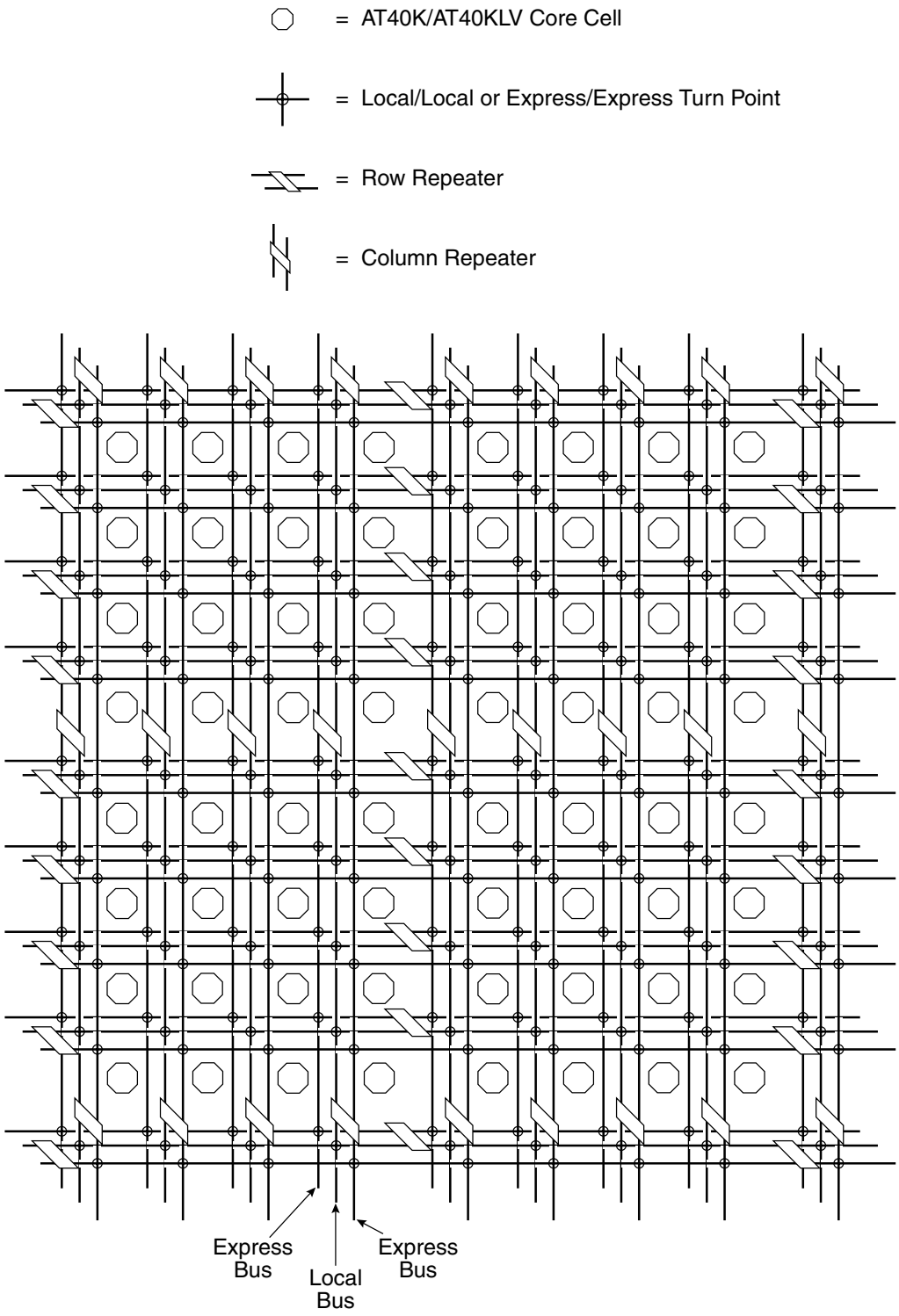
Figure 3 on page 7 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and "leapfrogs" or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface. Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resources on the AT40K/AT40KLV are used as a dual-function resources. Table 2 shows which buses are used in a dual-function mode and which bus plane is used. The AT40K/AT40KLV software tools are designed to accommodate dual-function buses in an efficient manner.

Table 2. Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1 - 5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	Data In connects to local bus plane 1
RAM Data Out	Local	2	Horizontal	Data out connects to local bus plane 2
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

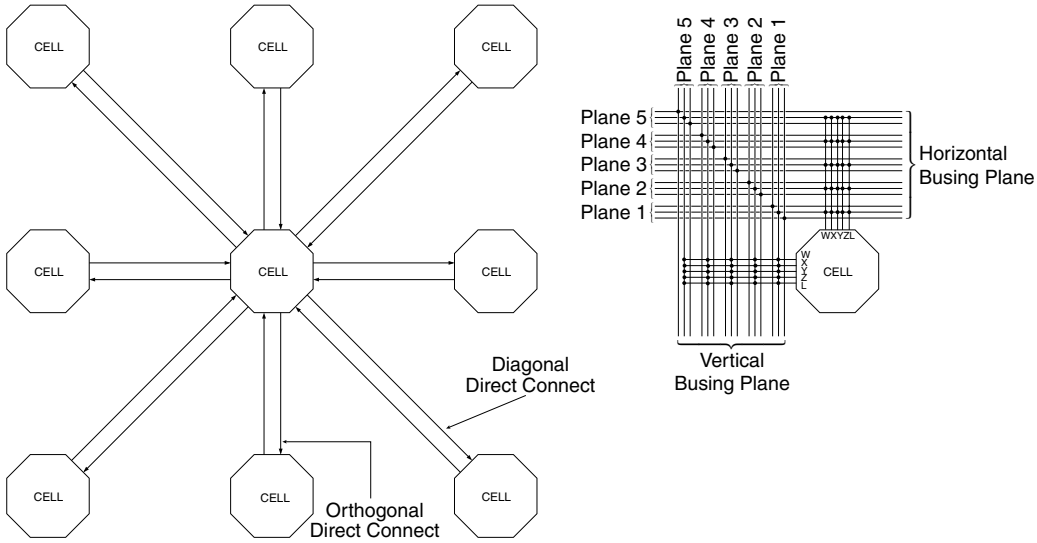
Figure 3. Busing Plane (One of Five)



Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell and five horizontal local buses (1 per busing plane) and five vertical local buses (1 per busing plane).

Figure 4. Cell Connections



(a) Cell-to-cell Connections

(b) Cell-to-bus Connections

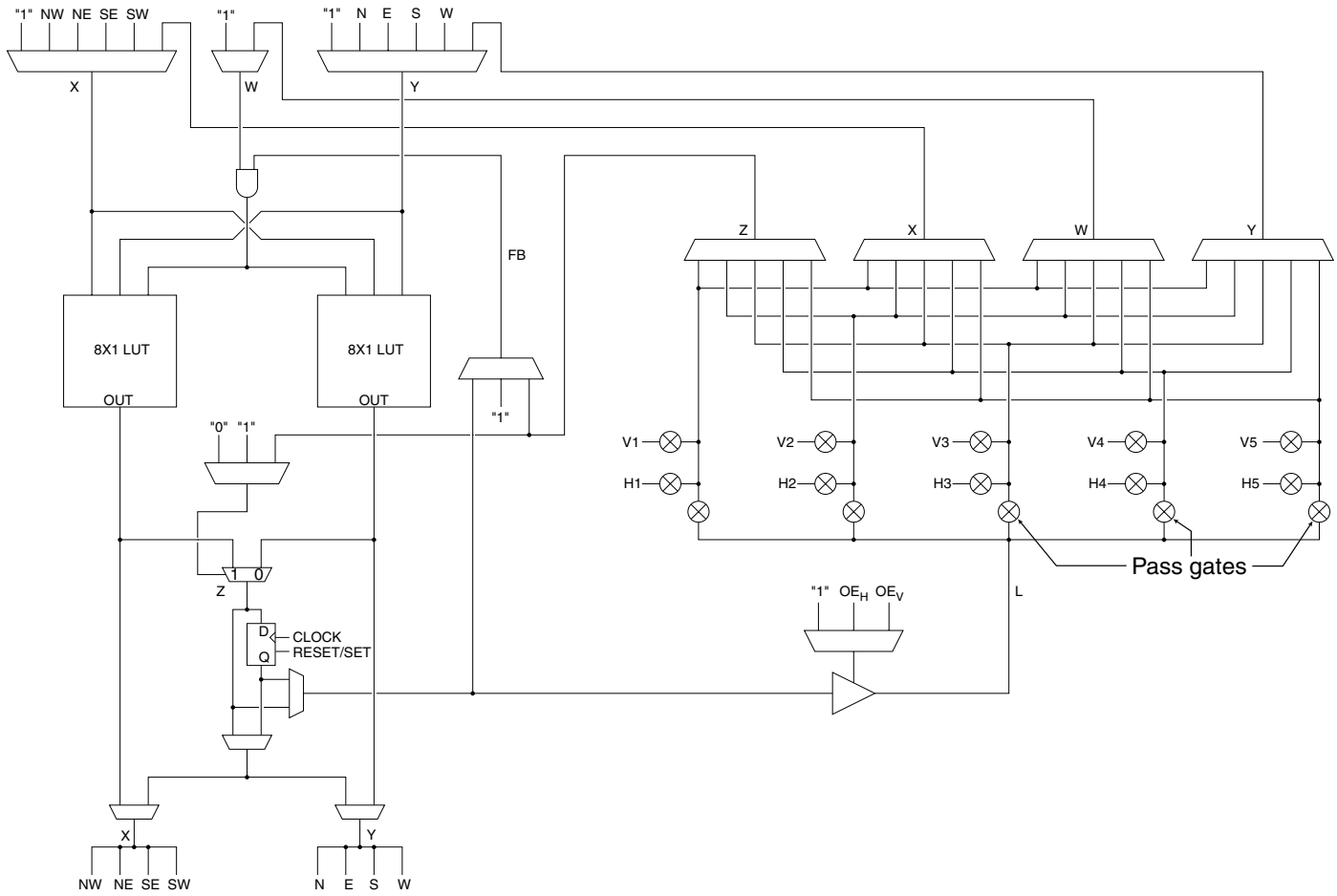
The Cell

Figure 5 depicts the AT40K/AT40KLV cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n (V_1 - V_5) is connected to the vertical local bus in plane n. H_n (H_1 - H_5) is connected to the horizontal local bus in plane *n*. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater route ability. Up to five simultaneous local/local turns are possible.

The AT40K/AT40KLV FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of 3 inputs or one function of 4 inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

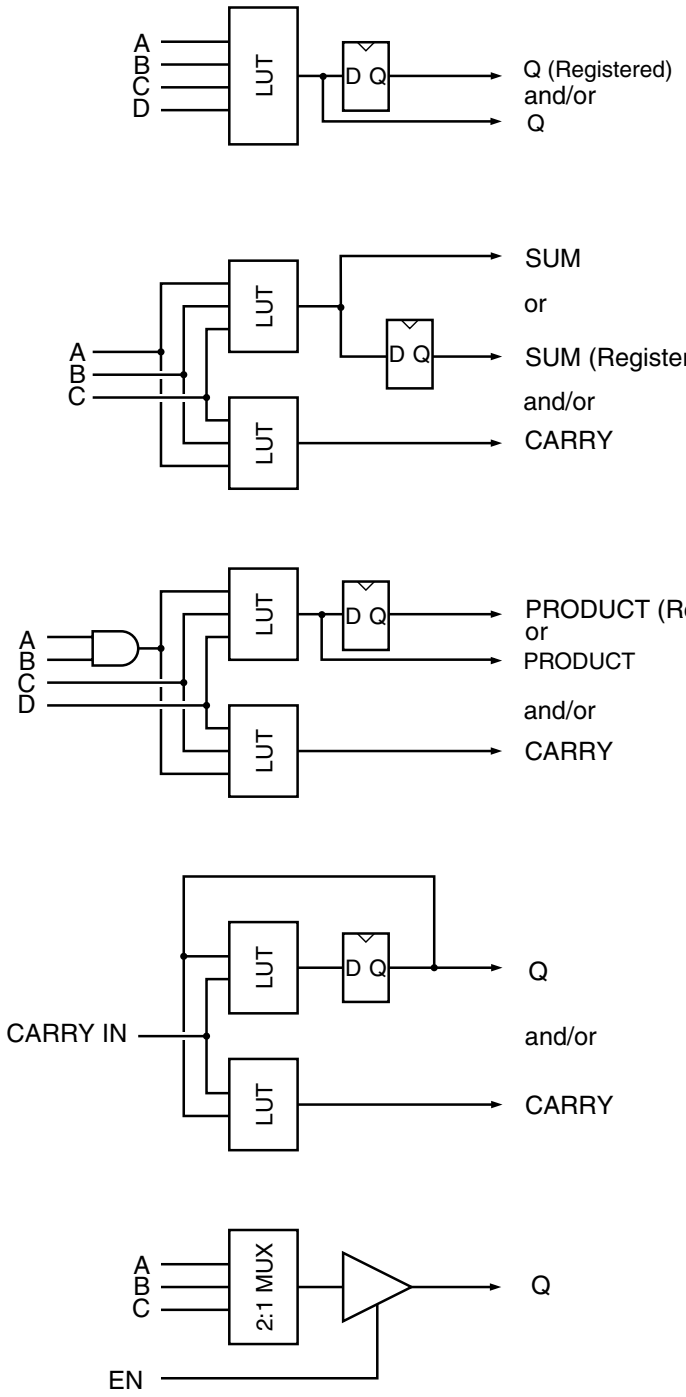
With this functionality in each core cell, the core cell can be configured in several “modes”. The core cell flexibility makes the AT40K/AT40KLV architecture well suited to most digital design application areas, see Figure 6.

Figure 5. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

Figure 6. Some Single Cell Modes



Synthesis Mode. This mode is particularly important for the use of VHDL/Verilog design. VHDL/Verilog Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

Arithmetic Mode is frequently used in many designs. As can be seen in the figure, the AT40K/AT40KLV core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40K/AT40KLV architecture.

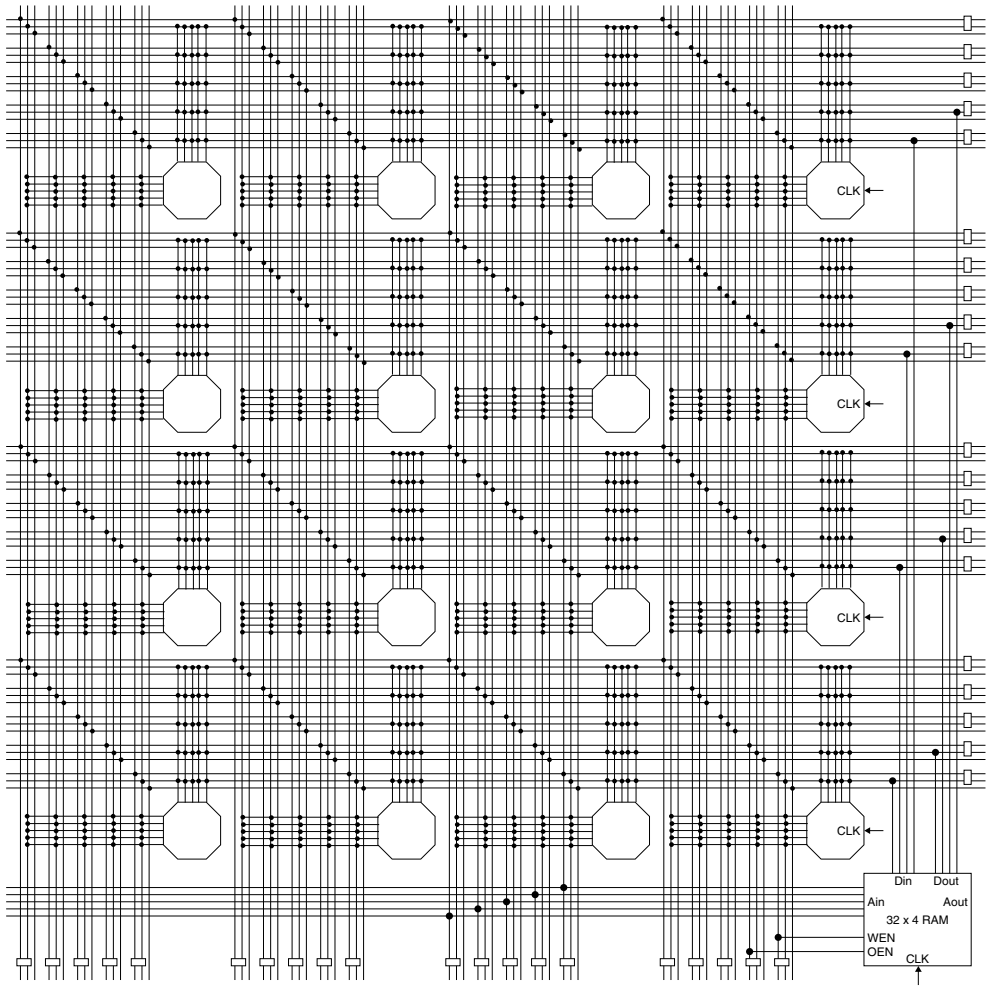
Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

RAM

32 x 4 dual-ported RAM blocks are dispersed throughout the array, see Figure 7. A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sectors in the same column. A 5-bit Output Address Bus connects to five vertical express buses in the same column. Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, Aout is on the left and Ain is on the right. For the right-most RAM blocks, Ain is on the left and Aout is tied off, thus it can only be configured as a single port. For single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. WEN and OEN connect to the vertical express buses in the same column.

Figure 7. RAM Connections (One Ram Block)



Reading and writing of the 10 ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. These latches are used to synchronize Write Address, $\overline{\text{Write Enable Not}}$, and Din signals for a synchronous RAM. Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble (bit = 7) is (Write) addressed and LOAD is logic 1 and $\overline{\text{WE}}$ is logic 0, data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{\text{WE}}$ is logic 1, data is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select "1" (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM clear byte during configuration clears the RAM (see the "*AT40K Configuration Series"* application note at www.atmel.com).

Figure 8. RAM Logic

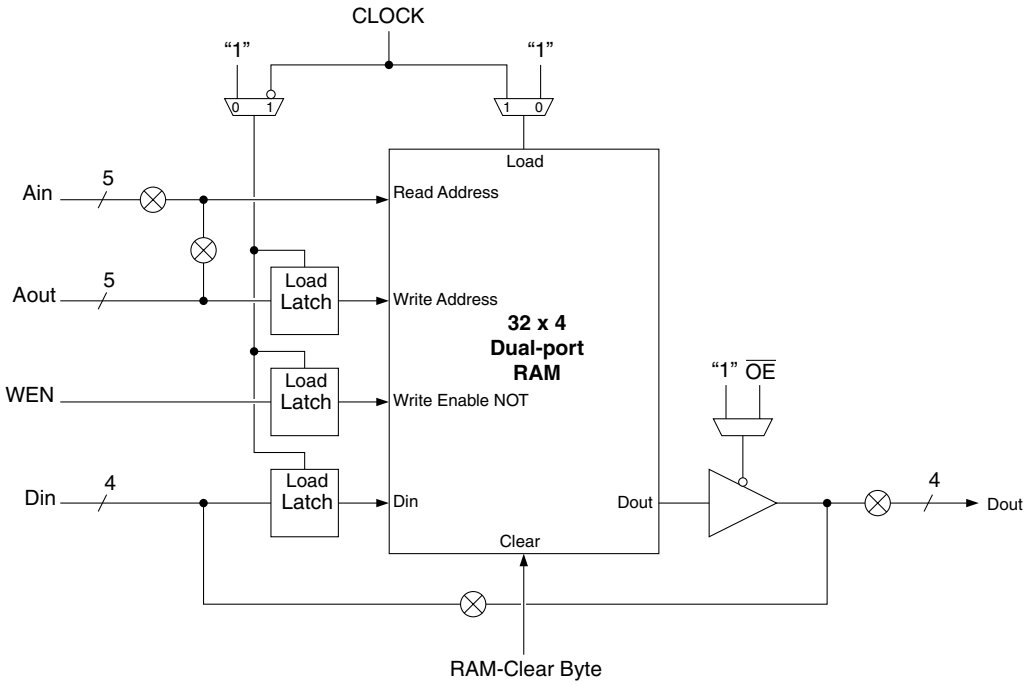
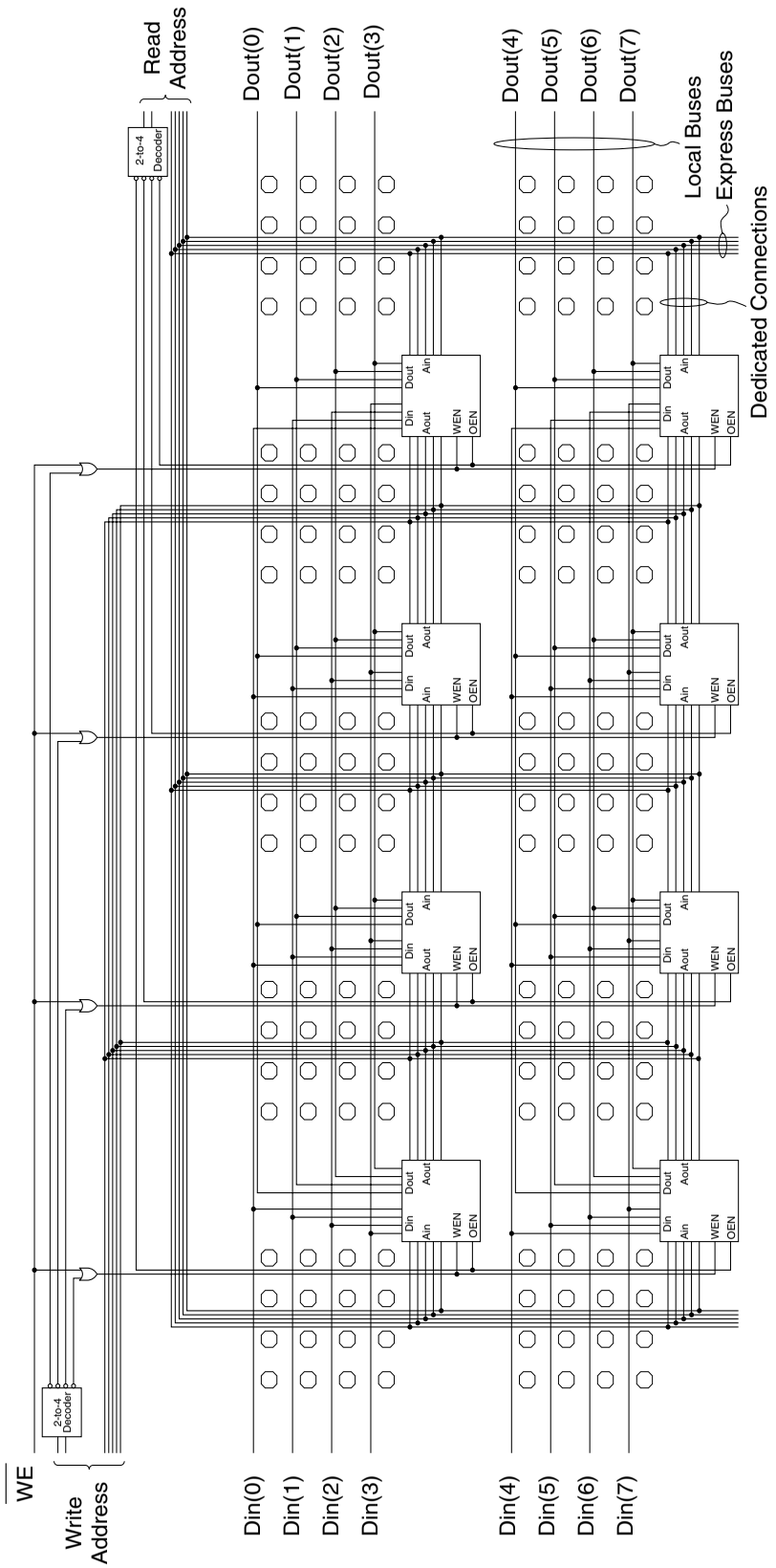


Figure 9 on page 13 shows an example of a RAM macro constructed using the AT40K/AT40KLV's FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM. Note the very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells (core cells) in the sectors occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

Figure 9. RAM Example: 128 x 8 Dual-ported RAM (Asynchronous)



Clocking Scheme

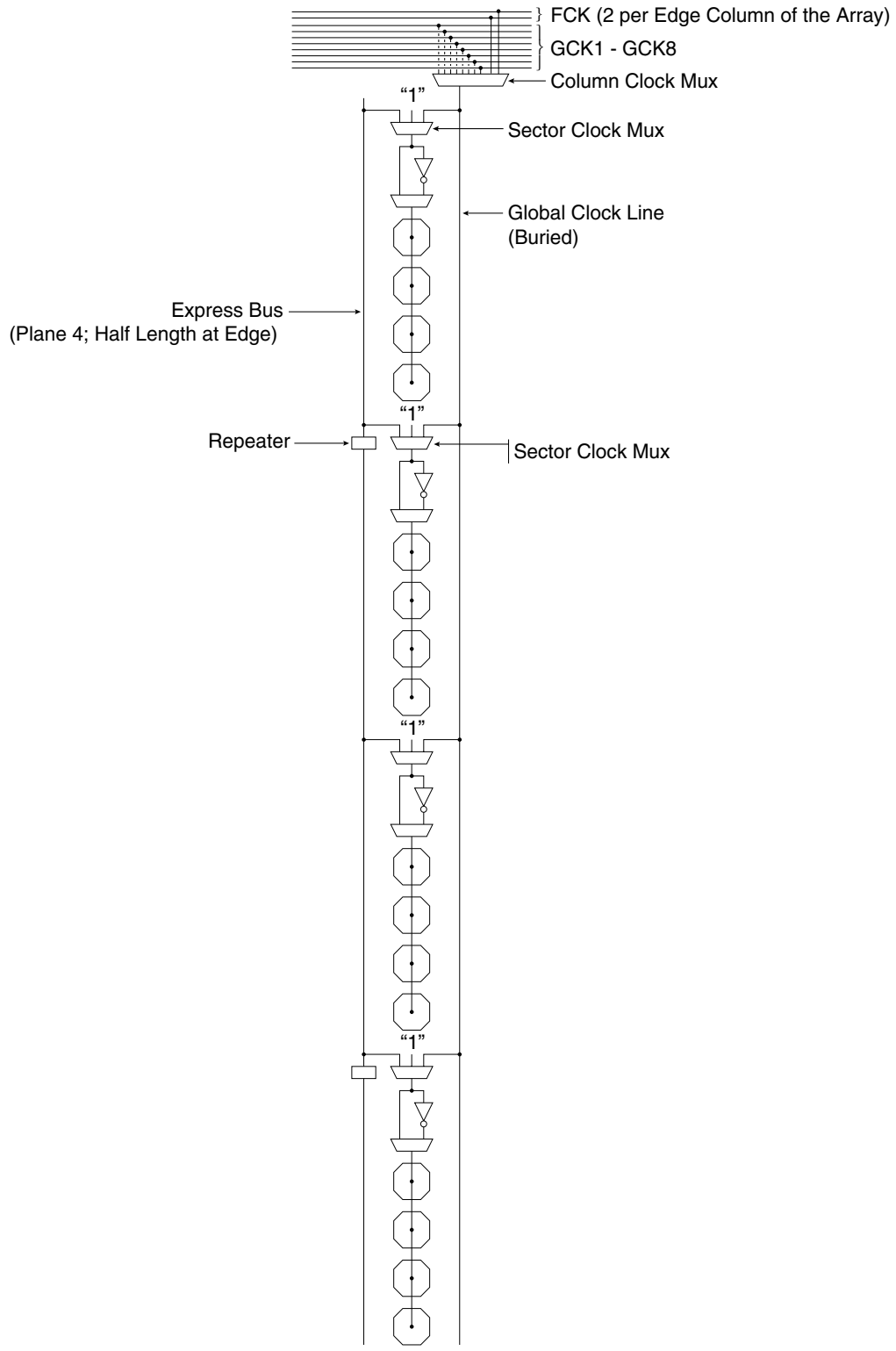
There are eight Global Clock buses (GCK1 - GCK8) on the AT40K/AT40KLV FPGA. Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible: this can be done by using Assign Pin Locks to lock the clocks to the Global Clock locations. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 - FCK4), two per edge column of the array for PCI specification.

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks. The clock can either come from the Column Clock or from the Plane 4 express bus, see Figure 10 on page 15. The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration on power-up, constant “0” is provided to each register’s clock pins. After configuration on power-up, the registers either set or reset, depending on the user’s choice.

The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Figure 10. Clocking (for One Column of Cells)



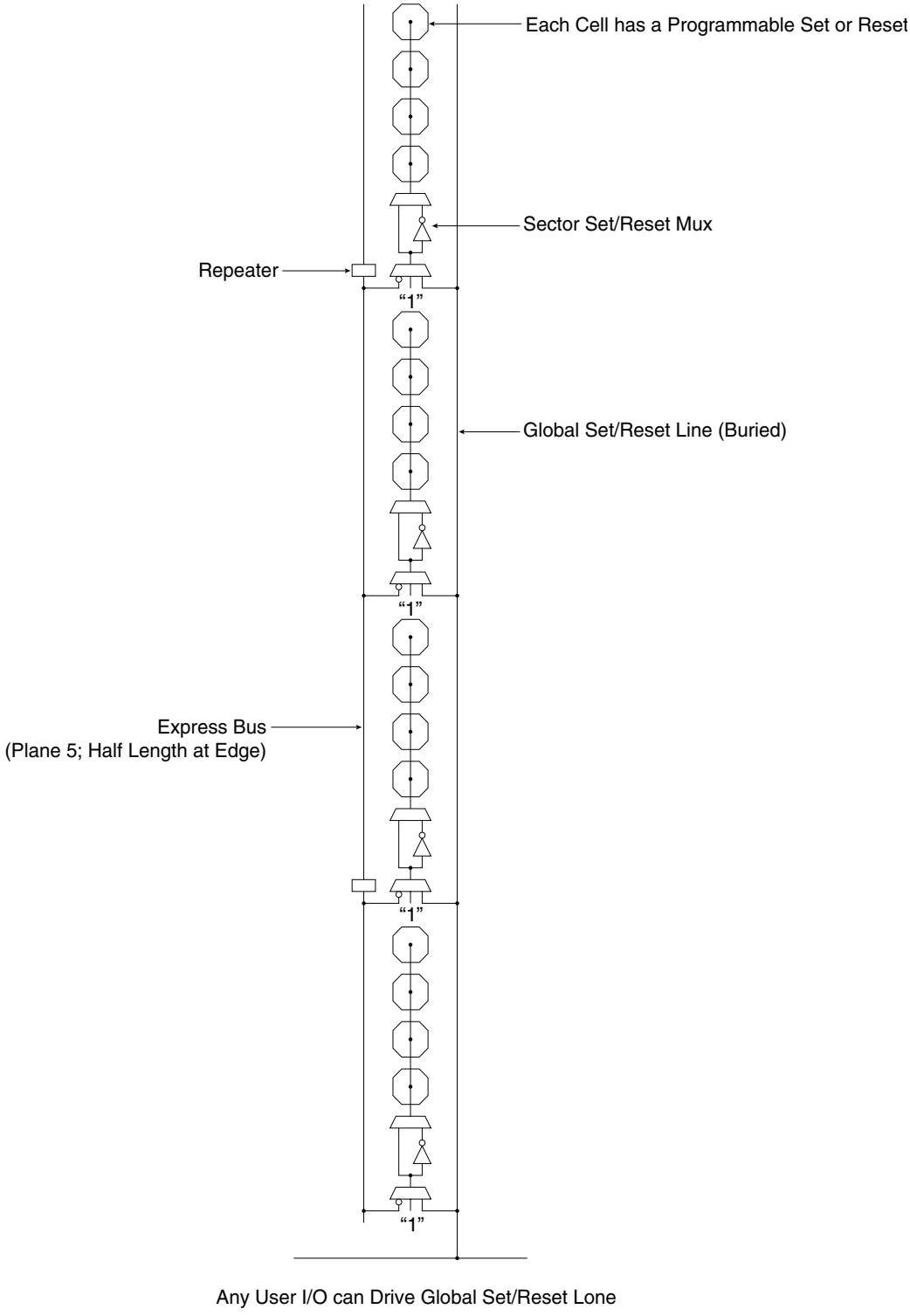
Set/Reset Scheme

The AT40K/AT40KLV family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 11 on page 17. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 11. Set/Reset (for One Column of Cells)



I/O Structure

PAD

The I/O pad is the one that connects the I/O to the outside world. Note that not all I/Os have pads: the ones without pads are called Unbonded I/Os. The number of unbonded I/Os varies with the device size and package. These unbonded I/Os are used to perform a variety of bus turns at the edge of the array.

PULL-UP/PULL-DOWN

Each pad has a programmable pull-up and pull-down attached to it. This supplies a weak “1” or “0” level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

The input stage of each I/O cell has a number of parameters that can be programmed either as properties in schematic entry or in the I/O Pad Attributes editor in IDS.

TTL/CMOS

The threshold level can be set to either TTL/CMOS-compatible levels.

SCHMITT

A Schmitt trigger circuit can be enabled on the inputs. The Schmitt trigger is a regenerative comparator circuit that adds 1V hysteresis to the input. This effectively improves the rise and fall times (leading and trailing edges) of the incoming signal and can be useful for filtering out noise.

DELAYS

The input buffer can be programmed to include four different intrinsic delays as specified in the AC timing characteristics. This feature is useful for meeting data hold requirements for the input signal.

DRIVE

The output drive capabilities of each I/O are programmable. They can be set to FAST, MEDIUM or SLOW (using IDS tool). The FAST setting has the highest drive capability (20 mA at 5V) buffer and the fastest slew rate. MEDIUM produces a medium drive (14 mA at 5V) buffer, while SLOW yields a standard (6 mA at 5V) buffer.

TRI-STATE

The output of each I/O can be made tri-state (0, 1 or Z), open source (1 or Z) or open drain (0 or Z) by programming an I/O’s Source Selection mux. Of course, the output can be normal (0 or 1), as well.

SOURCE SELECTION MUX

The Source Selection mux selects the source for the output signal of an I/O, see Figure 12 on page 20.

Primary, Secondary and Corner I/Os

The AT40K/AT40KLV has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40K/AT40KLV has access to one Primary I/O and two Secondary I/Os.

Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figures 12a on page 20 and 13a on page 21.

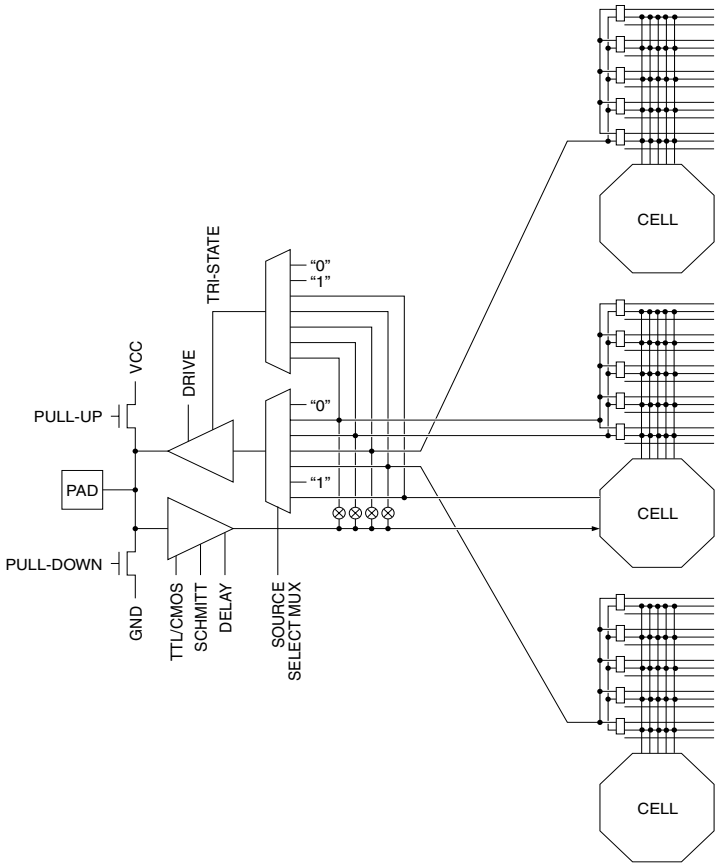
Secondary I/O

Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 12b on page 20 and Figure 13b.

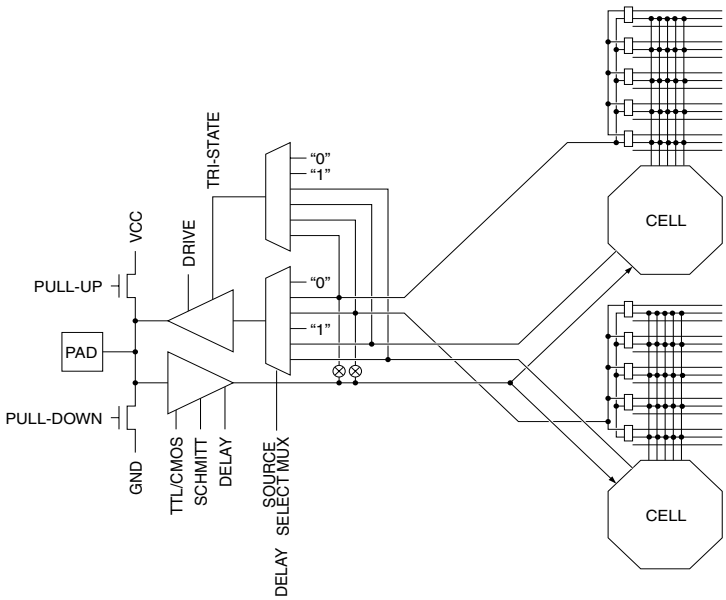
Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os: 2 Primary, 2 Secondary and 1 Corner I/O. Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40K/AT40KLV FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 14 on page 22.

Figure 12. West I/O (Mirrored for East I/O) AT40K/AT40KLV

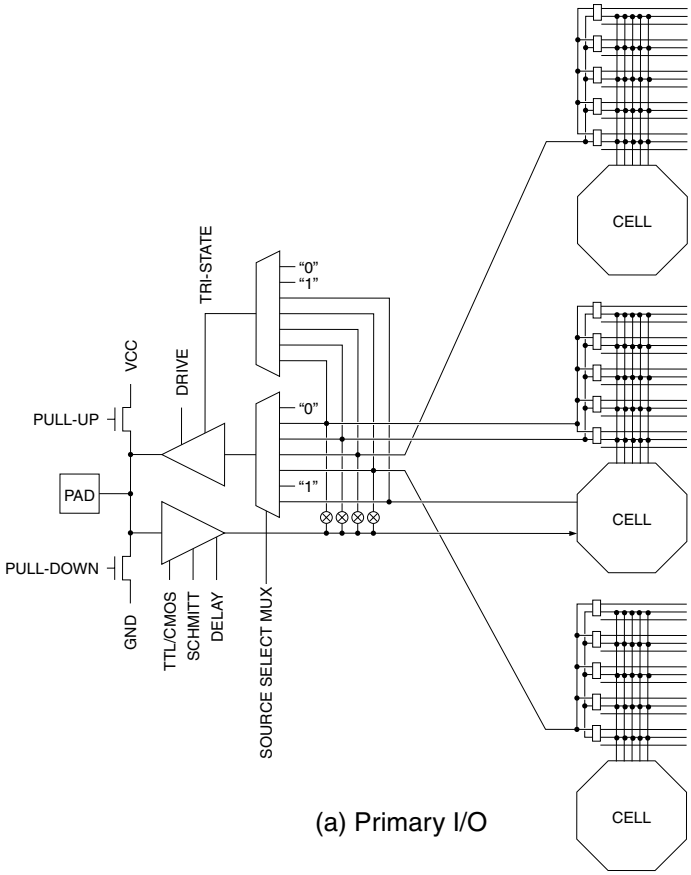


(a) Primary I/O

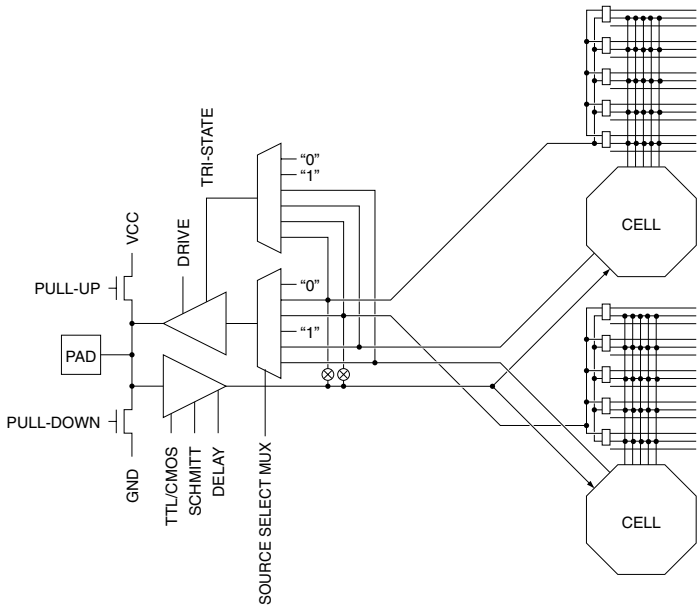


(b) Secondary I/O

Figure 13. South I/O (Mirrored for North I/O) AT40K/AT40KLV

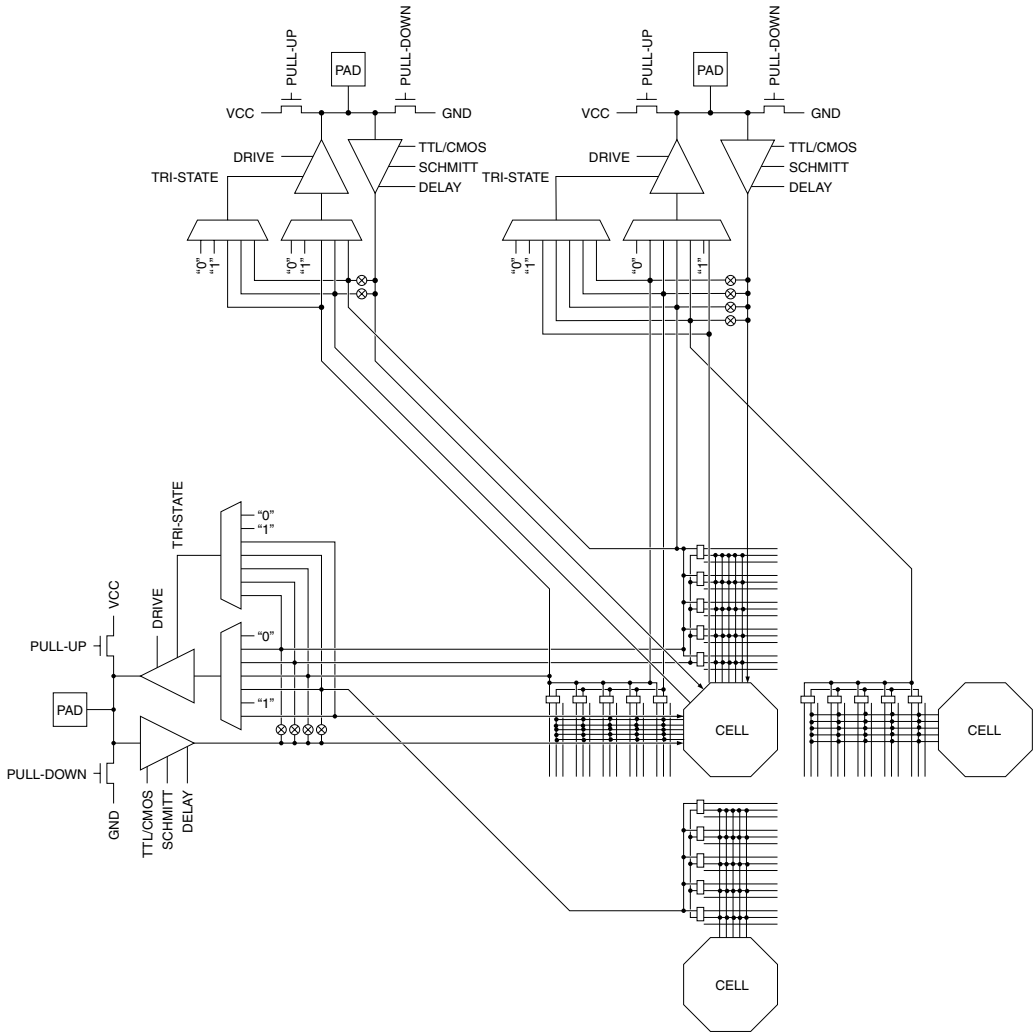


(a) Primary I/O



(a) Secondary I/O

Figure 14. Northwest Corner (Similar for NE/SE/SW Corners) AT40K/AT40KLV



Absolute Maximum Ratings – 5V Commercial/Industrial* AT40K

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to V_{CC} +7V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Range – 5V Operation AT40K

		Commercial -2	Industrial -2	Military -2
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}	2.0V - V_{CC}	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V	0V - 0.8V	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}	0 - 30% V_{CC}

DC Characteristics – 5V Operation Commercial/Industrial/Military AT40K

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = 6mA V_{CC} = V_{CC} Minimum	Ind. = 3.15 4.0 Con = 3.325			V
		I_{OH} = 14mA V_{CC} = V_{CC} Minimum	Ind. = 3.15 4.0 Con = 3.325			V
		I_{OH} = 20mA Commercial = 4.75V Industrial/Military = 4.5V	Ind. = 3.15 4.0 Con = 3.325			V
V_{OL}	Low-level Output Voltage	I_{OL} = -6mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
		I_{OL} = -14mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
		I_{OL} = -20mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC}	125.0	250.0	500.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10.0			µA
		With pull-up, V_{IN} = V_{SS}	CON = -1 mA to -250 µA	-250.0	CON = -1 mA to -250 µA	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC}			10.0	µA
		With pull-down, V_{IN} = V_{CC}	125.0	250.0	500.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS} Maximum	-10.0			µA
		With pull-up, V_{IN} = V_{SS} Maximum	-500.0	-250.0	-125.0	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

AC Timing Characteristics – 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2	Units	Notes
Core					
2-input Gate	t_{PD} (Maximum)	x/y -> x/y	1.8	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.1	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/w -> x/y	2.2	ns	1 unit load
4-input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> y	1.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> y	1.7	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> x	1.8	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> x	1.5	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> x	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> y	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> x	1.7	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> x/y	1.8	ns	1 unit load
DFF	t_{PD} (Maximum)	R -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	S -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> w	1.8	ns	
Incremental -> L	t_{PD} (Maximum)	x/y -> L	1.5	ns	1 unit load
Local Output Enable	t_{PZX} (Maximum)	oe -> L	1.4	ns	1 unit load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	1.8	ns	

AC Timing Characteristics – 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> IO	0.8	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.2	ns	No extra delay
Input	t_{PD} (Maximum)	pad -> x/y	3.6	ns	1 extra delay
Input	t_{PD} (Maximum)	pad -> x/y	7.3	ns	2 extra delays
Input	t_{PD} (Maximum)	pad -> x/y	10.8	ns	3 extra delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	5.9	ns	50 pf load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	4.8	ns	50 pf load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	3.9	ns	50 pf load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	6.2	ns	50 pf load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	1.3	ns	50 pf load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	4.8	ns	50 pf load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	1.9	ns	50 pf load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	3.7	ns	50 pf load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	1.6	ns	50 pf load

AC Timing Characteristics – 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-2	Units	Notes
Global Clocks and Set/Reset						
GCLK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05	1.1	ns	Rising edge clock
		pad -> clock	AT40K10	1.2	ns	
		pad -> clock	AT40K20	1.2	ns	
		pad -> clock	AT40K40	1.4	ns	
FCLK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05	0.7	ns	Rising edge clock
		pad -> clock	AT40K10	0.8	ns	
		pad -> clock	AT40K20	0.8	ns	
		pad -> clock	AT40K40	0.8	ns	
Clock Column Driver	t_{PD} (Maximum)	clock -> colclk	AT40K05	0.8	ns	Rising edge clock
		clock -> colclk	AT40K10	0.9	ns	
		clock -> colclk	AT40K20	1.0	ns	
		clock -> colclk	AT40K40	1.1	ns	
Clock Sector Driver	t_{PD} (Maximum)	colclk -> secclk	AT40K05	0.5	ns	Rising edge clock
		colclk -> secclk	AT40K10	0.5	ns	
		colclk -> secclk	AT40K20	0.5	ns	
		colclk -> secclk	AT40K40	0.5	ns	
GSRN Input Buffer	t_{PD} (Maximum)	pad -> GSRN	AT40K05	3.0	ns	From any pad to Global Set/Reset network
		pad -> GSRN	AT40K10	3.7	ns	
		pad -> GSRN	AT40K20	4.3	ns	
		pad -> GSRN	AT40K40	5.6	ns	
Global Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05	8.3	ns	Rising edge clock
		clock pad -> out	AT40K10	8.4	ns	Fully loaded clock tree
		clock pad -> out	AT40K20	8.6	ns	Rising edge DFF
		clock pad -> out	AT40K40	8.8	ns	20 mA output buffer
						50 pf pin load
Fast Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05	7.9	ns	Rising edge clock
		clock pad -> out	AT40K10	8.0	ns	Fully loaded clock tree
		clock pad -> out	AT40K20	8.1	ns	Rising edge DFF
		clock pad -> out	AT40K40	8.3	ns	20 mA output buffer
						50 pf pin load

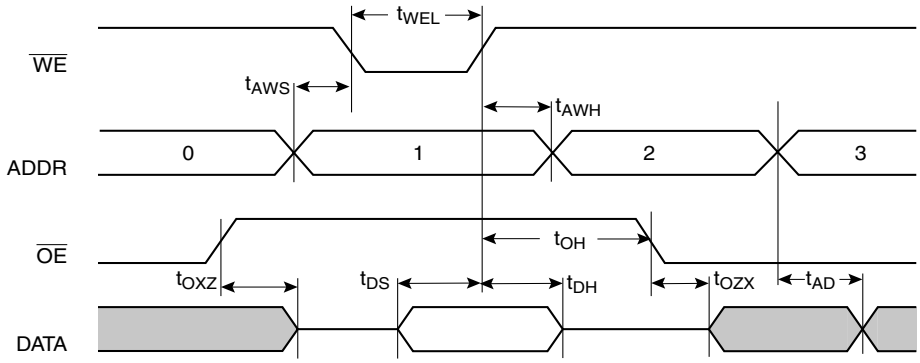
AC Timing Characteristics – 5V Operation AT40K

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

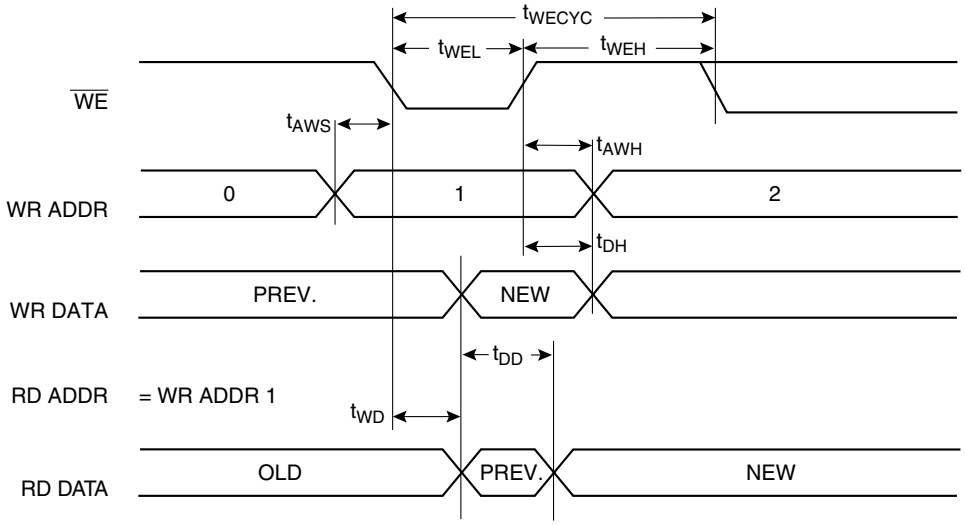
Cell Function	Parameter	Path	-2	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	8.0	ns	
Write	t_{WEL} (Minimum)	we	3.0	ns	Pulse width low
Write	t_{WEH} (Minimum)	we	3.0	ns	Pulse width high
Write	t_{AWS} (Minimum)	wr addr setup -> we	2.0	ns	
Write	t_{AWH} (Minimum)	wr addr hold -> we	0.0	ns	
Write	t_{DS} (Minimum)	din setup -> we	2.0	ns	
Write	t_{DH} (Minimum)	din hold -> we	0.0	ns	
Write/Read	t_{DD} (Maximum)	din -> dout	4.6	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	3.1	ns	
Read	t_{OZX} (Maximum)	oe -> dout	1.6	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	2.0	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	8.0	ns	
Write	t_{CLKL} (Minimum)	clk	3.0	ns	Pulse width low
Write	t_{CLKH} (Minimum)	clk	3.0	ns	Pulse width high
Write	t_{WCS} (Minimum)	we setup -> clk	2.0	ns	
Write	t_{WCH} (Minimum)	we hold -> clk	0.0	ns	
Write	t_{ACS} (Minimum)	wr addr setup -> clk	2.0	ns	
Write	t_{ACH} (Minimum)	wr addr hold -> clk	0.0	ns	
Write	t_{DCS} (Minimum)	wr data setup -> clk	2.0	ns	
Write	t_{DCH} (Minimum)	wr data hold -> clk	0.0	ns	
Write/Read	t_{CD} (Maximum)	clk -> dout	3.5	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	3.1	ns	
Read	t_{OZX} (Maximum)	oe -> dout	1.6	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	2.0	ns	

FreeRAM Asynchronous Timing Characteristics

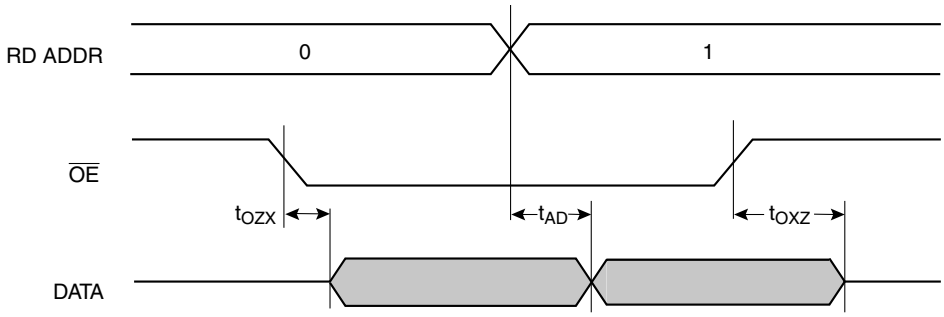
Single-port Write/Read



Dual-port Write with Read

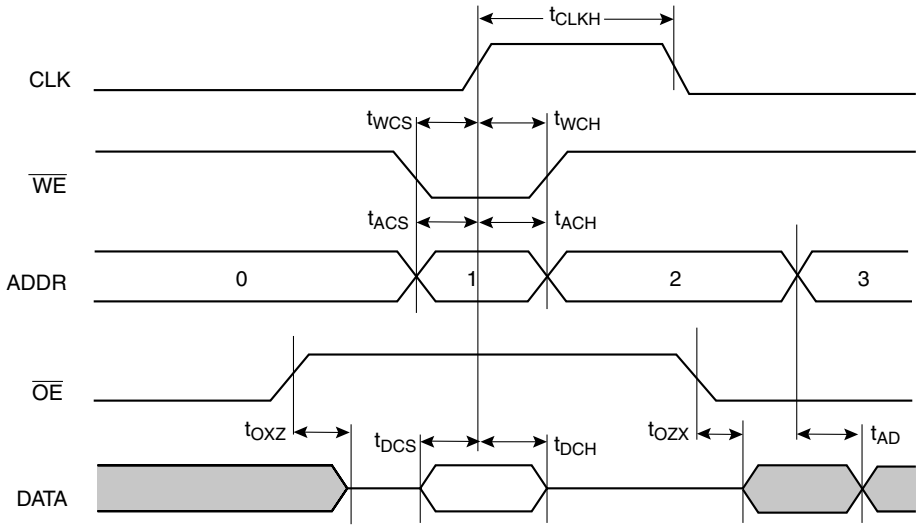


Dual-port Read

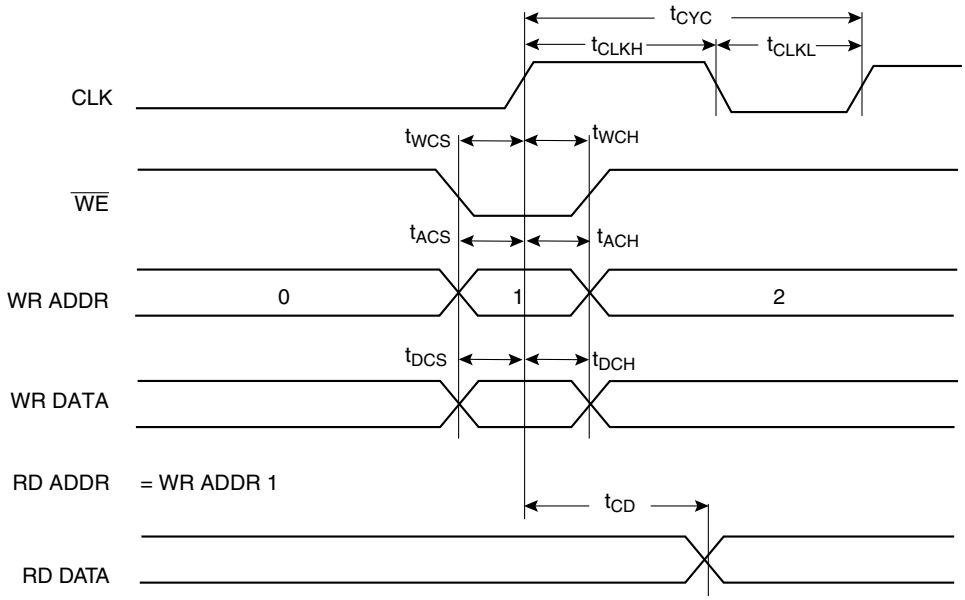


FreeRAM Synchronous Timing Characteristics

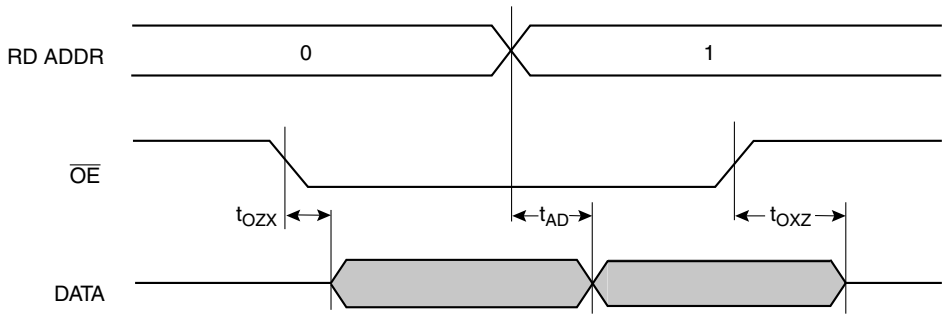
Single-port Write/Read



Dual-port Write with Read



Dual-port Read



Absolute Maximum Ratings – 3.3V Commercial/Industrial* AT40KLV

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to V_{CC} +7V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Range – 3.3V Operation AT40KLV

		Commercial	Industrial
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

DC Characteristics – 3.3V Operation Commercial/Industrial AT40KLV

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = 4 mA V_{CC} = V_{CC} Minimum	2.1			V
		I_{OH} = 12 mA V_{CC} = 3.0V	2.1			V
		I_{OH} = 16 mA V_{CC} = 3.0V	2.1			V
V_{OL}	Low-level Output Voltage	I_{OL} = -4 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -12 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -16 mA V_{CC} = 3.0V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC}	75.0	150.0	300.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10.0			µA
		With pull-up, V_{IN} = V_{SS}	-300.0	-150.0	-75.0	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC} Maximum	75.0	150.0	300.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS}	-10.0			mA
		With pull-up, V_{IN} = V_{SS}	CON = -500 µA TO -125 µA	-150.0	CON = -500 µA TO -125 µA-	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

AC Timing Characteristics – 3.3V Operation AT40KLV

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.00V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.60V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-3	Units	Notes
Core					
2-input Gate	t_{PD} (Maximum)	x/y -> x/y	2.9	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.8	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/w -> x/y	3.4	ns	1 unit load
4-input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	3.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> y	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> y	2.9	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> x	3.0	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> x	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> y	3.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> x	3.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> y	3.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> x	2.4	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> x/y	2.8	ns	1 unit load
DFF	t_{PD} (Maximum)	R -> x/y	3.2	ns	1 unit load
DFF	t_{PD} (Maximum)	S -> x/y	3.0	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> w	2.7	ns	
Incremental -> L	t_{PD} (Maximum)	x/y -> L	2.4	ns	1 unit load
Local Output Enable	t_{PZX} (Maximum)	oe -> L	2.8	ns	1 unit load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	2.4	ns	

AC Timing Characteristics – 3.3V Operation AT40KLV

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-3	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	2.2	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> E	2.2	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> L	2.2	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> L	2.2	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> IO	1.4	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> IO	1.4	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-3	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.9	ns	No extra delay
Input	t_{PD} (Maximum)	pad -> x/y	5.8	ns	1 extra delay
Input	t_{PD} (Maximum)	pad -> x/y	11.5	ns	2 extra delays
Input	t_{PD} (Maximum)	pad -> x/y	17.4	ns	3 extra delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	9.1	ns	50 pf load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	7.6	ns	50 pf load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	6.2	ns	50 pf load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	9.5	ns	50 pf load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	2.1	ns	50 pf load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	7.4	ns	50 pf load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	2.7	ns	50 pf load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	5.9	ns	50 pf load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	2.4	ns	50 pf load

AC Timing Characteristics – 3.3V Operation AT40KLV

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-3	Units	Notes
Global Clocks and Set/Reset						
GCK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05LV	1.3	ns	Rising edge clock
		pad -> clock	AT40K10LV	1.5	ns	
		pad -> clock	AT40K20LV	1.6	ns	
		pad -> clock	AT40K40LV	1.9	ns	
FCK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05LV	0.7	ns	Rising edge clock
		pad -> clock	AT40K10LV	0.8	ns	
		pad -> clock	AT40K20LV	0.8	ns	
		pad -> clock	AT40K40LV	0.9	ns	
Clock Column Driver	t_{PD} (Maximum)	clock -> colclk	AT40K05LV	1.5	ns	Rising edge clock
		clock -> colclk	AT40K10LV	1.8	ns	
		clock -> colclk	AT40K20LV	2.0	ns	
		clock -> colclk	AT40K40LV	2.5	ns	
Clock Sector Driver	t_{PD} (Maximum)	colclk -> secclk	AT40K05LV	1.0	ns	Rising edge clock
		colclk -> secclk	AT40K10LV	1.0	ns	
		colclk -> secclk	AT40K20LV	1.0	ns	
		colclk -> secclk	AT40K40LV	1.0	ns	
GSRN Input Buffer	t_{PD} (Maximum)	pad -> GSRN	AT40K05LV	4.5	ns	
		pad -> GSRN	AT40K10LV	5.4	ns	
		pad -> GSRN	AT40K20LV	6.3	ns	
		pad -> GSRN	AT40K40LV	8.2	ns	
Global Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05LV	13.0	ns	Rising edge clock
		clock pad -> out	AT40K10LV	13.4	ns	Fully loaded clock tree
		clock pad -> out	AT40K20LV	13.8	ns	Rising edge DFF
		clock pad -> out	AT40K40LV	14.5	ns	20 mA output buffer
						50 pf pin load
Fast Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05LV	12.4	ns	Rising edge clock
		clock pad -> out	AT40K10LV	12.7	ns	Fully loaded clock tree
		clock pad -> out	AT40K20LV	13.0	ns	Rising edge DFF
		clock pad -> out	AT40K40LV	13.5	ns	20 mA output buffer
						50 pf pin load

AC Timing Characteristics – 3.3V Operation AT40KLV

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-3	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	12.0	ns	
Write	t_{WEL} (Minimum)	we	5.0	ns	Pulse width low
Write	t_{WEH} (Minimum)	we	5.0	ns	Pulse width high
Write	t_{AWS} (Minimum)	wr addr setup -> we	5.3	ns	
Write	t_{AWH} (Minimum)	wr addr hold -> we	0.0	ns	
Write	t_{DS} (Minimum)	din setup -> we	5.0	ns	
Write	t_{DH} (Minimum)	din hold -> we	0.0	ns	
Write/Read	t_{DD} (Maximum)	din -> dout	8.7	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	12.0	ns	
Write	t_{CLKL} (Minimum)	clk	5.0	ns	Pulse width low
Write	t_{CLKH} (Minimum)	clk	5.0	ns	Pulse width high
Write	t_{WCS}(Minimum)	we setup -> clk	3.2	ns	
Write	t_{WCH} (Minimum)	we hold -> clk	0.0	ns	
Write	t_{ACS} (Minimum)	wr addr setup -> clk	5.0	ns	
Write	t_{ACH} (Minimum)	wr addr hold -> clk	0.0	ns	
Write	t_{DCS} (Minimum)	wr data setup -> clk	3.9	ns	
Write	t_{DCH} (Minimum)	wr data hold -> clk	0.0	ns	
Write/Read	t_{CD} (Maximum)	clk -> dout	5.8	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	

Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer software.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Left Side (Top to Bottom)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
GND	GND	GND	GND	12	4	1	1	1	2	1	304	GND[1]
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	5	2	2	2	4	2	303	D23
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	6	3	3	3	5	3	302	C25
I/O3	I/O3	I/O3	I/O3				4	4	6	4	301	D24
I/O4	I/O4	I/O4	I/O4				5	5	7	5	300	E23
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	7	4	6	6	8	6	299	C26
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	8	5	7	7	9	7	298	E24
			GND									
			I/O7									
			I/O8									
			I/O9									D25
			I/O10									F23
		I/O7	I/O11								297	F24
		I/O8	I/O12								296	E25
		VCC	VCC									VCC[1]
		GND	GND									GND[1]
			I/O13									
			I/O14									
I/O7	I/O7	I/O9	I/O15					8	10	8	295	D26
I/O8	I/O8	I/O10	I/O16					9	11	9	294	G24
	I/O9	I/O11	I/O17						12	10	293	F25
	I/O10	I/O12	I/O18						13	11	292	F26
			GND									
			I/O19									
			I/O20									
	I/O11	I/O13	I/O21							12	291	H23
	I/O12	I/O14	I/O22							13	290	H24
		I/O15	I/O23								289	G25
		I/O16	I/O24								288	G26
GND	GND	GND	GND				8	10	14	14	287	GND[1]
I/O9, FCK1	I/O13, FCK1	I/O17, FCK1	I/O25, FCK1				9	11	15	15	286	J23
I/O10	I/O14	I/O18	I/O26				10	12	16	16	285	J24

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Left Side (Top to Bottom)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
I/O11 (A20)	I/O15 (A20)	I/O19 (A20)	I/O27 (A20)	17	9	6	11	13	17	17	284	H25
I/O12 (A21)	I/O16 (A21)	I/O20 (A21)	I/O28 (A21)	18	10	7	12	14	18	18	283	K23
	VCC	VCC	VCC							19	282	VCC[1]
	I/O17	I/O21	I/O29							20	280	K24
	I/O18	I/O22	I/O30							21	279	J25
			GND									
			I/O31									
			I/O32									
			I/O33									J26
			I/O34									L23
		I/O23	I/O35								278	L24
		I/O24	I/O36								277	K25
		GND	GND							22		GND[1]
			VCC									VCC[1]
			I/O37									
			I/O38									
		I/O25	I/O39								276	L25
		I/O26	I/O40								275	L26
	I/O19	I/O27	I/O41						19	23	274	M23
	I/O20	I/O28	I/O42						20	24	273	M24
			GND									
I/O13	I/O21	I/O29	I/O43				13	15	21	25	272	M25
I/O14	I/O22	I/O30	I/O44		11	8	14	16	22	26	271	M26
			I/O45									
			I/O46									
I/O15 (A22)	I/O23 (A22)	I/O31 (A22)	I/O47 (A22)	19	12	9	15	17	23	27	270	N24
I/O16 (A23)	I/O24 (A23)	I/O32 (A23)	I/O48 (A23)	20	13	10	16	18	24	28	269	N25
GND	GND	GND	GND	21	14	11	17	19	25	29	268	GND[1]
VCC	VCC	VCC	VCC	22	15	12	18	20	26	30	267	VCC[1]
I/O17	I/O25	I/O33	I/O49	23	16	13	19	21	27	31	266	N26
I/O18	I/O26	I/O34	I/O50	24	17	14	20	22	28	32	265	P25
			I/O51									
			I/O52									
I/O19	I/O27	I/O35	I/O53		18	15	21	23	29	33	264	P23

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Left Side (Top to Bottom)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
I/O20	I/O28	I/O36	I/O54				22	24	30	34	263	P24
			GND									
	I/O29	I/O37	I/O55						31	35	262	R26
	I/O30	I/O38	I/O56						32	36	261	R25
		I/O39	I/O57								260	R24
		I/O40	I/O58								259	R23
			I/O59									
			I/O60									
			VCC									VCC[1]
		GND	GND							37		GND[1]
		I/O41	I/O61								258	T26
		I/O42	I/O62								257	T25
			I/O63									
			I/O64									
			I/O65									T24
			I/O66									U25
			GND									
	I/O31	I/O43	I/O67							38	256	T23
	I/O32	I/O44	I/O68							39	255	V26
	VCC	VCC	VCC							40	253	VCC[1]
I/O21	I/O33	I/O45	I/O69	25	19	16	23	25	33	41	252	U24
I/O22	I/O34	I/O46	I/O70	26	20	17	24	26	34	42	251	V25
I/O23	I/O35	I/O47	I/O71				25	27	35	43	250	V24
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2				26	28	36	44	249	U23
GND	GND	GND	GND				27	29	37	45	248	GND[1]
		I/O49	I/O73								247	Y26
		I/O50	I/O74								246	W25
	I/O37	I/O51	I/O75							46	245	W24
	I/O38	I/O52	I/O76							47	244	V23
			I/O77									
			I/O78									
			GND									
			I/O79									
			I/O80									
	I/O39	I/O53	I/O81						38	48	243	AA26
	I/O40	I/O54	I/O82						39	49	242	Y25

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Left Side (Top to Bottom)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
I/O25	I/O41	I/O55	I/O83					30	40	50	241	Y24
I/O26	I/O42	I/O56	I/O84					31	41	51	240	AA25
		GND	GND									GND[1]
		VCC	VCC									VCC[1]
		I/O57	I/O85								239	AB25
		I/O58	I/O86								238	AA24
			I/O87									
			I/O88									
I/O27	I/O43	I/O59	I/O89	27	21	18	28	32	42	52	237	Y23
I/O28	I/O44	I/O60	I/O90		22	19	29	33	43	53	236	AC26
			GND									
			I/O91									AD26
			I/O92									AC25
I/O29	I/O45	I/O61	I/O93				30	34	44	54	235	AA23
I/O30	I/O46	I/O62	I/O94				31	35	45	55	234	AB24
I/O31 ($\overline{OTS}$)[3]	I/O47 ($\overline{OTS}$)[3]	I/O63 ($\overline{OTS}$)[3]	I/O95 ($\overline{OTS}$)[3]	28	23	20	32	36	46	56	233	AD25
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	24	21	33	37	47	57	232	AC24
M1	M1	M1	M1	30	25	22	34	38	48	58	231	AB23
GND	GND	GND	GND	31	26	23	35	39	49	59	230	GND[1]
M0	M0	M0	M0	32	27	24	36	40	50	60	229	AD24

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Bottom Side (Left to Right)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
VCC	VCC	VCC	VCC	33	28	25	37	41	55	61	228	VCC[1]
M2	M2	M2	M2	34	29	26	38	42	56	62	227	AC23
I/O33, GCK3	I/O49, GCK3	I/O65, GCK3	I/O97, GCK3	35	30	27	39	43	57	63	226	AE24
I/O34 (HDC)	I/O50 (HDC)	I/O66 (HDC)	I/O98 (HDC)	36	31	28	40	44	58	64	225	AD23
I/O35	I/O51	I/O67	I/O99				41	45	59	65	224	AC22
I/O36	I/O52	I/O68	I/O100				42	46	60	66	223	AF24
I/O37	I/O53	I/O69	I/O101		32	29	43	47	61	67	222	AD22

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Bottom Side (Left to Right)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
I/O38 (LDC)	I/O54 (LDC)	I/O70 (LDC)	I/O102 (LDC)	37	33	30	44	48	62	68	221	AE23
			GND									
			I/O103									
			I/O104									
			I/O105									AC21
			I/O106									AD21
		I/O71	I/O107								220	AE22
		I/O72	I/O108								219	AF23
		VCC	VCC									VCC[1]
		GND	GND									GND[1]
I/O39	I/O55	I/O73	I/O109					49	63	69	218	AD20
I/O40	I/O56	I/O74	I/O110					50	64	70	217	AE21
	I/O57	I/O75	I/O111						65	71	216	AF21
	I/O58	I/O76	I/O112						66	72	215	AC19
			I/O113									
			I/O114									
			GND									
		I/O77	I/O115									
		I/O78	I/O116									
	I/O59	I/O79	I/O117							73	214	AD19
	I/O60	I/O80	I/O118							74	213	AE20
			I/O119								212	AF20
			I/O120								211	AC18
GND	GND	GND	GND				45	51	67	75	210	GND[1]
I/O41	I/O61	I/O81	I/O121				46	52	68	76	209	AD18
I/O42	I/O62	I/O82	I/O122				47	53	69	77	208	AE19
I/O43	I/O63	I/O83	I/O123	38	34	31	48	54	70	78	207	AC17
I/O44	I/O64	I/O84	I/O124	39	35	32	49	55	71	79	206	AD17
	VCC	VCC	VCC							80	204	VCC[1]
	I/O65	I/O85	I/O125						72	81	203	AE18
	I/O66	I/O86	I/O126						73	82	202	AF18
			GND									
			I/O127									
			I/O128									
			I/O129									AC16
			I/O130									AD16

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Bottom Side (Left to Right)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
		I/O87	I/O131								201	AE17
		I/O88	I/O132								200	AE16
		GND	GND							83		GND[1]
			VCC									VCC[1]
		I/O89	I/O133								199	AF16
		I/O90	I/O134								198	AC15
	I/O67	I/O91	I/O135							84	197	AD15
	I/O68	I/O92	I/O136							85	196	AE15
I/O45	I/O69	I/O93	I/O137		36	33	50	56	74	86	195	AF15
I/O46	I/O70	I/O94	I/O138		37	34	51	57	75	87	194	AD14
			GND									
			I/O139									
			I/O140									
			I/O141									
			I/O142									
I/O47 (D15)	I/O71 (D15)	I/O95 (D15)	I/O143 (D15)	40	38	35	52	58	76	88	193	AE14
I/O48 (INIT)	I/O72 (INIT)	I/O96 (INIT)	I/O144 (INIT)	41	39	36	53	59	77	89	192	AF14
VCC	VCC	VCC	VCC	42	40	37	54	60	78	90	191	VCC[1]
GND	GND	GND	GND	43	41	38	55	61	79	91	190	GND[1]
I/O49 (D14)	I/O73 (D14)	I/O97 (D14)	I/O145 (D14)	44	42	39	56	62	80	92	189	AE13
I/O50 (D13)	I/O74 (D13)	I/O98 (D13)	I/O146 (D13)	45	43	40	57	63	81	93	188	AC13
			I/O147									
			I/O148									
			I/O149									
			I/O150									
			GND									
I/O51	I/O75	I/O99	I/O151		44	41	58	64	82	94	187	AD13
I/O52	I/O76	I/O100	I/O152		45	42	59	65	83	95	186	AF12
	I/O77	I/O101	I/O153						84	96	185	AE12
	I/O78	I/O102	I/O154						85	97	184	AD12
		I/O103	I/O155								183	AC12
		I/O104	I/O156								182	AF11
			VCC									VCC[1]
		GND	GND							98		GND[1]
		I/O105	I/O157								181	AE11

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Bottom Side (Left to Right)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
		I/O106	I/O158								180	AD11
			I/O159									AE10
			I/O160									AC11
			I/O161									
			I/O162									
			GND									
	I/O79	I/O107	I/O163							99	179	AF9
	I/O80	I/O108	I/O164							100	178	AD10
	VCC	VCC	VCC							101	177	VCC[1]
I/O53 (D12)	I/O81 (D12)	I/O109 (D12)	I/O165 (D12)	46	46	43	60	66	86	102	175	AE9
I/O54 (D11)	I/O82 (D11)	I/O110 (D11)	I/O166 (D11)	47	47	44	61	67	87	103	174	AD9
I/O55	I/O83	I/O111	I/O167				62	68	88	104	173	AC10
I/O56	I/O84	I/O112	I/O168				63	69	89	105	172	AF7
GND	GND	GND	GND				64	70	90	106	171	GND[1]
		I/O113	I/O169								170	AE8
		I/O114	I/O170								169	AD8
	I/O85	I/O115	I/O171							107	168	AC9
	I/O86	I/O116	I/O172							108	167	AF6
			I/O173									
			I/O174									
			GND									
			I/O175									
			I/O176									
	I/O87	I/O117	I/O177						91	109	166	AE7
	I/O88	I/O118	I/O178						92	110	165	AD7
I/O57	I/O89	I/O119	I/O179					71	93	111	164	AE6
I/O58	I/O90	I/O120	I/O180					72	94	112	163	AE5
		GND	GND									GND[1]
		VCC	VCC									VCC[1]
		I/O121	I/O181								162	AD6
		I/O122	I/O182								161	AC7
I/O59 (D10)	I/O91 (D10)	I/O123 (D10)	I/O183 (D10)	48	48	45	65	73	95	113	160	AF4
I/O60 (D9)	I/O92 (D9)	I/O124 (D9)	I/O184 (D9)	49	49	46	66	74	96	114	159	AF3
			I/O185									AE4
			I/O186									AC6

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Bottom Side (Left to Right)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
			GND									
			I/O187									
			I/O188									
I/O61	I/O93	I/O125	I/O189				67	75	97	115	158	AD5
I/O62	I/O94	I/O126	I/O190				68	76	98	116	157	AE3
I/O63 (D8)	I/O95 (D8)	I/O127 (D8)	I/O191 (D8)	50	50	47	69	77	99	117	156	AD4
I/O64, GCK4	I/O96, GCK4	I/O128, GCK4	I/O192, GCK4	51	51	48	70	78	100	118	155	AC5
GND	GND	GND	GND	52	52	49	71	79	101	119	154	GND[1]
$\overline{CON}$	$\overline{CON}$	$\overline{CON}$	$\overline{CON}$	53	53	50	72	80	103	120	153	AD3

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Right Side (Bottom to Top)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
VCC	VCC	VCC	VCC	54	54	51	73	81	106	121	152	VCC[1]
$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$	55	55	52	74	82	108	122	151	AC4
I/O65 (D7)	I/O97 (D7)	I/O129 (D7)	I/O193 (D7)	56	56	53	75	83	109	123	150	AD2
I/O66, GCK5	I/O98, GCK5	I/O130, GCK5	I/O194, GCK5	57	57	54	76	84	110	124	149	AC3
I/O67	I/O99	I/O131	I/O195				77	85	111	125	148	AB4
I/O68	I/O100	I/O132	I/O196				78	86	112	126	147	AD1
		I/O133	I/O197									AB3
		I/O134	I/O198									AC2
			GND									
	I/O101	I/O135	I/O199							127	146	AA4
	I/O102	I/O136	I/O200							128	145	AA3
			I/O201									
			I/O202									
			I/O203								144	AB2
			I/O204								143	AC1
		VCC	VCC									VCC[1]
		GND	GND									GND[1]
I/O69 (D6)	I/O103 (D6)	I/O137 (D6)	I/O205 (D6)	58	58	55	79	87	113	129	142	Y3

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Right Side (Bottom to Top)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
I/O70	I/O104	I/O138	I/O206		59	56	80	88	114	130	141	AA2
I/O71	I/O105	I/O139	I/O207					89	115	131	140	AA1
I/O72	I/O106	I/O140	I/O208					90	116	132	139	W4
			I/O209									
			I/O210									
			GND									
			I/O211									
			I/O212									
	I/O107	I/O141	I/O213						117	133	138	W3
	I/O108	I/O142	I/O214						118	134	137	Y2
		I/O143	I/O215								136	Y1
		I/O144	I/O216								135	V4
GND	GND	GND	GND				81	91	119	135	134	GND[1]
	I/O109	I/O145	I/O217							136	133	V3
	I/O110	I/O146	I/O218							137	132	W2
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3				82	92	120	138	131	U4
I/O74	I/O112	I/O148	I/O220				83	93	121	139	130	U3
	VCC	VCC	VCC							140	129	VCC[1]
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	60	57	84	94	122	141	127	V2
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	61	58	85	95	123	142	126	V1
			GND									
			I/O223									T4
			I/O224									T3
			I/O225									
			I/O226									
		I/O151	I/O227								125	U2
		I/O152	I/O228								124	T2
		GND	GND							143		GND[1]
			VCC									VCC[1]
			I/O229									
			I/O230									
		I/O153	I/O231								123	T1
		I/O154	I/O232								122	R4
	I/O115	I/O155	I/O233						124	144	121	R3
	I/O116	I/O156	I/O234						125	145	120	R2

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Right Side (Bottom to Top)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
			GND									
I/O77	I/O117	I/O157	I/O235		62	59	86	96	126	146	119	R1
I/O78	I/O118	I/O158	I/O236		63	60	87	97	127	147	118	P3
			I/O237									
			I/O238									
I/O79(D4)	I/O119(D4)	I/O159(D4)	I/O239(D4)	61	64	61	88	98	128	148	117	P2
I/O80	I/O120	I/O160	I/O240	62	65	62	89	99	129	149	116	P1
VCC	VCC	VCC	VCC	63	66	63	90	100	130	150	115	VCC[1]
GND	GND	GND	GND	64	67	64	91	101	131	151	114	GND[1]
I/O81 (D3)	I/O121 (D3)	I/O161 (D3)	I/O241 (D3)	65	68	65	92	102	132	152	113	N2
I/O82 ($\overline{\text{CHECK}}$)	I/O122 ($\overline{\text{CHECK}}$)	I/O162 ($\overline{\text{CHECK}}$)	I/O242 ($\overline{\text{CHECK}}$)	66	69	66	93	103	133	153	112	N4
			I/O243									
			I/O244									
I/O83	I/O123	I/O163	I/O245		70	67	94	104	134	154	111	N3
I/O84	I/O124	I/O164	I/O246				95	105	135	155	110	M1
			GND									
	I/O125	I/O165	I/O247						136	156	109	M2
	I/O126	I/O166	I/O248						137	157	108	M3
		I/O167	I/O249								107	M4
		I/O168	I/O250								106	L1
			I/O251									
			I/O252									
			VCC									VCC[1]
		GND	GND							158		GND[1]
		I/O169	I/O253								105	L2
		I/O170	I/O254								104	L3
			I/O255									K2
			I/O256									L4
			I/O257									
			I/O258									
			GND									
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	71	68	96	106	138	159	103	J1
I/O86	I/O128	I/O172	I/O260	68	72	69	97	107	139	160	102	K3
	VCC	VCC	VCC							161	101	VCC[1]
I/O87	I/O129	I/O173	I/O261				98	108	140	162	99	J2

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Right Side (Bottom to Top)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4				99	109	141	163	98	J3
	I/O131	I/O175	I/O263							164	97	K4
	I/O132	I/O176	I/O264							165	96	G1
GND	GND	GND	GND				100	110	142	166	95	GND[1]
		I/O177	I/O265								94	H2
		I/O178	I/O266								93	H3
	I/O133	I/O179	I/O267							167	92	J4
	I/O134	I/O180	I/O268							168	91	F1
			I/O269									
			I/O270									
			GND									
	I/O135	I/O181	I/O271						143	169	90	G2
	I/O136	I/O182	I/O272						144	170	89	G3
I/O89	I/O137	I/O183	I/O273					111	145	171	88	F2
I/O90	I/O138	I/O184	I/O274					112	146	172	87	E2
			I/O275									
			I/O276									
		GND	GND									GND[1]
		VCC	VCC									VCC[1]
I/O91 (D1)	I/O139 (D1)	I/O185 (D1)	I/O277 (D1)	69	73	70	101	113	147	173	86	F3
I/O92	I/O140	I/O186	I/O278	70	74	71	102	114	148	174	85	G4
			I/O279									D1
			I/O280									C1
			I/O281									
			I/O282									
			GND									
		I/O187	I/O283								84	D2
		I/O188	I/O284								83	F4
I/O93	I/O141	I/O189	I/O285				103	115	149	175	82	E3
I/O94	I/O142	I/O190	I/O286				104	116	150	176	81	C2
I/O95 (D0)	I/O143 (D0)	I/O191 (D0)	I/O287 (D0)	71	75	72	105	117	151	177	80	D3
I/O96, GCK6 ($\overline{\text{CSOUT}}$)	I/O144, GCK6 ($\overline{\text{CSOUT}}$)	I/O192, GCK6 ($\overline{\text{CSOUT}}$)	I/O288, GCK6 ($\overline{\text{CSOUT}}$)	72	76	73	106	118	152	178	79	E4

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Right Side (Bottom to Top)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
CCLK	CCLK	CCLK	CCLK	73	77	74	107	119	153	179	78	C3
VCC	VCC	VCC	VCC	74	78	75	108	120	154	180	77	VCC[1]
TSTCLK	TSTCLK	TSTCLK	TSTCLK	75	79	76	109	121	159	181	76	D4

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Top Side (Right to Left)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
GND	GND	GND	GND	76	80	77	110	122	160	182	75	GND[1]
I/O97 (A0)	I/O145 (A0)	I/O193 (A0)	I/O289 (A0)	77	81	78	111	123	161	183	74	B3
I/O98, GCK7 (A1)	I/O146, GCK7 (A1)	I/O194, GCK7 (A1)	I/O290, GCK7 (A1)	78	82	79	112	124	162	184	73	C4
I/O99	I/O147	I/O195	I/O291				113	125	163	185	72	D5
I/O100	I/O148	I/O196	I/O292				114	126	164	186	71	A3
			I/O293									
			I/O294									
			GND									
			I/O295									C5
			I/O296									B4
I/O101 ($\overline{CS1}$,A2)	I/O149 ($\overline{CS1}$,A2)	I/O197 ($\overline{CS1}$,A2)	I/O297 ($\overline{CS1}$,A2)	79	83	80	115	127	165	187	70	D6
I/O102 (A3)	I/O150 (A3)	I/O198 (A3)	I/O298 (A3)	80	84	81	116	128	166	188	69	C6
		I/O199	I/O299								68	B5
		I/O200	I/O300								67	A4
		VCC	VCC									VCC[1]
		GND	GND									GND[1]
	I/O151[3]	I/O201[3]	I/O301[3]	75[3] NC	79[3] NC	76[3] NC	109[3] NC	121[3] NC	159[3] NC	189[3] NC	66[3] NC	C7[3] NC
	I/O152	I/O202	I/O302							190	65	B6
I/O103	I/O153	I/O203	I/O303				117	129	167	191	64	A6
I/O104[3]	I/O154	I/O204	I/O304					130	168	192	63	D8
			I/O305									C8
			I/O306									
			GND									

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Top Side (Right to Left)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
			I/O307									
			I/O308									
	I/O155	I/O205	I/O309						169	193	62	B7
	I/O156	I/O206	I/O310						170	194	61	A7
		I/O207	I/O311							195	60	D9
		I/O208	I/O312								59	C9
GND	GND	GND	GND				118	131	171	196	58	GND[1]
I/O105	I/O157	I/O209	I/O313				119	132	172	197	57	B8
I/O106	I/O158	I/O210	I/O314				120	133	173	198	56	D10
	I/O159	I/O211	I/O315							199	55	C10
	I/O160	I/O212	I/O316							200	54	B9
	VCC	VCC	VCC							201	52	VCC[1]
		I/O213	I/O317								51	A9
		I/O214	I/O318								50	D11
			GND									
			I/O319									
			I/O320									
			I/O321									C11
			I/O322									B10
		I/O215	I/O323								49	B11
		I/O216	I/O324								48	A11
		GND	GND									GND[1]
			VCC									VCC[1]
I/O107 (A4)	I/O161 (A4)	I/O217 (A4)	I/O325 (A4)	81	85	82	121	134	174	202	47	D12
I/O108 (A5)	I/O162 (A5)	I/O218 (A5)	I/O326 (A5)	82	86	83	122	135	175	203	46	C12
	I/O163	I/O219	I/O327						176	205	45	B12
	I/O164	I/O220	I/O328					136	177	206	44	A12
I/O109	I/O165	I/O221	I/O329		87	84	123	137	178	207	43	C13
I/O110	I/O166	I/O222	I/O330		88	85	124	138	179	208	42	B13
			GND									
			I/O331									
			I/O332									
			I/O333									
			I/O334									
I/O111 (A6)	I/O167 (A6)	I/O223 (A6)	I/O335 (A6)	83	89	86	125	139	180	209	41	A13

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Top Side (Right to Left)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
I/O112 (A7)	I/O168 (A7)	I/O224 (A7)	I/O336 (A7)	84	90	87	126	140	181	210	40	B14
GND	GND	GND	GND	1	91	88	127	141	182	211	39	GND[1]
VCC	VCC	VCC	VCC	2	92	89	128	142	183	212	38	VCC[1]
I/O113 (A8)	I/O169 (A8)	I/O225 (A8)	I/O337 (A8)	3	93	90	129	143	184	213	37	D14
I/O114 (A9)	I/O170 (A9)	I/O226 (A9)	I/O338 (A9)	4	94	91	130	144	185	214	36	C14
			I/O339									
			I/O340									
			I/O341									
			I/O342									
			GND									
I/O115	I/O171	I/O227	I/O343		95	92	131	145	186	215	35	A15
I/O116	I/O172	I/O228	I/O344		96	93	132	146	187	216	34	B15
	I/O173	I/O229	I/O345						188	217	33	C15
	I/O174	I/O230	I/O346						189	218	32	D15
I/O117 (A10)	I/O175 (A10)	I/O231 (A10)	I/O347 (A10)	5	97	94	133	147	190	220	31	A16
I/O118 (A11)	I/O176 (A11)	I/O232 (A11)	I/O348 (A11)	6	98	95	134	148	191	221	30	B16
			VCC									VCC[1]
		GND	GND									GND[1]
		I/O233	I/O349								29	C16
		I/O234	I/O350								28	B17
			I/O351									D16
			I/O352									A18
			I/O353									
			I/O354									
			GND									
		I/O235	I/O355								27	C17
		I/O236	I/O356								26	B18
	VCC	VCC	VCC							222	25	VCC[1]
	I/O177	I/O237	I/O357							223	23	C18
	I/O178	I/O238	I/O358							224	22	D17
I/O119	I/O179	I/O239	I/O359				135	149	192	225	21	A20
I/O120	I/O180	I/O240	I/O360				136	150	193	226	20	B19
GND	GND	GND	GND				137	151	194	227	19	GND[1]
		I/O241	I/O361								18	C19

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K05 AT40K05LV	AT40K10 AT40K10LV	AT40K20 AT40K20LV	AT40K40 AT40K40LV	Top Side (Right to Left)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
		I/O242	I/O362								17	D18
	I/O181	I/O243	I/O363						195	228	16	A21
	I/O182	I/O244	I/O364						196	229	15	B20
			I/O365									
			I/O366									
			GND									
			I/O367									
			I/O368									
I/O121	I/O183	I/O245	I/O369					152	197	230	14	C20
I/O122	I/O184	I/O246	I/O370					153	198	231	13	B21
I/O123 (A12)	I/O185 (A12)	I/O247 (A12)	I/O371 (A12)	7	99	96	138	154	199	232	12	B22
I/O124 (A13)	I/O186 (A13)	I/O248 (A13)	I/O372 (A13)	8	100	97	139	155	200	233	10	C21
		GND	GND									GND[1]
		VCC	VCC									VCC[1]
		I/O249	I/O373								9	D20
		I/O250	I/O374								8	A23
			I/O375									A24
			I/O376									B23
			I/O377									
			I/O378									
			GND									
	I/O187	I/O251	I/O379							234	7	D21
	I/O188	I/O252	I/O380							235	6	C22
I/O125	I/O189	I/O253	I/O381				140	156	201	236	5	B24
I/O126	I/O190	I/O254	I/O382				141	157	202	237	4	C23
I/O127 (A14)	I/O191 (A14)	I/O255 (A14)	I/O383 (A14)	9	1	98	142	158	203	238	3	D22
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O256, GCK8 (A15)	I/O384, GCK8 (A15)	10	2	99	143	159	204	239	2	C24
VCC	VCC	VCC	VCC	11	3	100	144	160	205	240	1	VCC[1]

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

Power and Ground Pinouts for 352 SBGA[1]

VCC Pins						
A10	A17	B2	B25	D7	D13	D19
G23	H4	K1	K26	N23	P4	U1
U26	W23	Y4	AC8	AC14	AC20	AE2
AE25	AF10	AF17				
GND Pins						
A1	A2	A5	A8	A14	A19	A22
A25	A26	B1	B26	E1	E26	H1
H26	N1	P26	W1	W26	AB1	AB26
AE1	AE26	AF1	AF2	AF5	AF8	AF13
AF19	AF22	AF25	AF26			

Note: 1. In SBGA packages, Power and Ground pins do not connect directly to die. They connect to Power and Ground planes inside the package.

Part/Package Availability and User I/O Counts (including Dual-function Pins)

Package[1]	AT40K05/AT40K05LV	AT40K10/AT40K10LV	AT40K20/AT40K20LV	AT40K40/AT40K40LV
84 PLCC	62	62	62	–
100 PQFP	78	78	77	–
100 TQFP	78	78	78	–
144 LQFP	114	114	114	114
160 PQFP	128	130	130	–
208 PQFP	128	161	161	161
240 PQFP	–	–	193	193
304 PQFP	–	–	–	256
352 SBGA	–	–	–	289

Note: 1. Devices in same package are pin-to-pin compatible.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100Q4	100-lead, Plastic Quad Flat Package (PQFP)
100T1	100-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
144L1	144-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)
160Q1	160-lead, Plastic Quad Flat Package (PQFP)
208Q1	208-lead, Plastic Quad Flat Package (PQFP)
240Q1	240-lead, Plastic Quad Flat Package (PQFP)
304Q1	304-lead, Plastic Quad Flat Package (PQFP)
352C1	252-ball, Enhanced, Low-profile Square Ball Grid Array Package (SBGA)

AT40K05/AT40K05LV Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
5,000 - 10,000	5.0V	2	AT40K05-2AJC	84J	Commercial
			AT40K05-2AQC	100T1	(0°C to 70°C)
			AT40K05-2RQC	100Q4	
			AT40K05-2BQC	144L1	
			AT40K05-2CQC	160Q1	
			AT40K05-2DQC	208Q1	
5,000 - 10,000	5.0V	2	AT40K05-2AJI	84J	Industrial
			AT40K05-2AQI	100T1	(-40°C to 85°C)
			AT40K05-2RQI	100Q4	
			AT40K05-2BQI	144L1	
			AT40K05-2CQI	160Q1	
			AT40K05-2DQI	208Q1	
5,000 - 10,000	3.3V	3	AT40K05LV-3AJC	84J	Commercial
			AT40K05LV-3AQC	100T1	(0°C to 70°C)
			AT40K05LV-3RQC	100Q4	
			AT40K05LV-3BQC	144L1	
			AT40K05LV-3CQC	160Q1	
			AT40K05LV-3DQC	208Q1	
5,000 - 10,000	3.3V	3	AT40K05LV-3AJI	84J	Industrial
			AT40K05LV-3AQI	100T1	(-40°C to 85°C)
			AT40K05LV-3RQI	100Q4	
			AT40K05LV-3BQI	144L1	
			AT40K05LV-3CQI	160Q1	
			AT40K05LV-3DQI	208Q1	

Note: 1. For military parts, contact Atmel at fpga@atmel.com.

AT40K10/AT40K10LV Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
10,000 - 20,000	5.0V	2	AT40K10-2AJC	84J	Commercial
			AT40K10-2AQC	100T1	(0°C to 70°C)
			AT40K10-2RQC	100Q4	
			AT40K10-2BQC	144L1	
			AT40K10-2CQC	160Q1	
			AT40K10-2DQC	208Q1	
10,000 - 20,000	5.0V	2	AT40K10-2AJI	84J	Industrial
			AT40K10-2AQI	100T1	(-40°C to 85°C)
			AT40K10-2RQI	100Q4	
			AT40K10-2BQI	144L1	
			AT40K10-2CQI	160Q1	
			AT40K10-2DQI	208Q1	
10,000 - 20,000	3.3V	3	AT40K10LV-3AJC	84J	Commercial
			AT40K10LV-3AQC	100T1	(0°C to 70°C)
			AT40K10LV-3RQC	100Q4	
			AT40K10LV-3BQC	144L1	
			AT40K10LV-3CQC	160Q1	
			AT40K10LV-3DQC	208Q1	
10,000 - 20,000	3.3V	3	AT40K10LV-3AJI	84J	Industrial
			AT40K10LV-3AQI	100T1	(-40°C to 85°C)
			AT40K10LV-3RQI	100Q4	
			AT40K10LV-3BQI	144L1	
			AT40K10LV-3CQI	160Q1	
			AT40K10LV-3DQI	208Q1	

Note: 1. For military parts, contact Atmel at fpga@atmel.com.

AT40K20/AT40K20LV Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
20,000 - 30,000	5.0V	2	AT40K20-2AJC	84J	Commercial
			AT40K20-2AQC	100T1	(0°C to 70°C)
			AT40K20-2RQC	100Q4	
			AT40K20-2BQC	144L1	
			AT40K20-2CQC	160Q1	
			AT40K20-2DQC	208Q1	
			AT40K20-2EQC	240Q1	
20,000 - 30,000	5.0V	2	AT40K20-2AJI	84J	Industrial
			AT40K20-2AQI	100T1	(-40°C to 85°C)
			AT40K20-2RQI	100Q4	
			AT40K20-2BQI	144L1	
			AT40K20-2CQI	160Q1	
			AT40K20-2DQI	208Q1	
			AT40K20-2EQI	240Q1	
20,000 - 30,000	3.3V	3	AT40K20LV-3AJC	84J	Commercial
			AT40K20LV-3AQC	100T1	(0°C to 70°C)
			AT40K20LV-3RQC	100Q4	
			AT40K20LV-3BQC	144L1	
			AT40K20LV-3CQC	160Q1	
			AT40K20LV-3DQC	208Q1	
			AT40K20LV-2EQC	240Q1	
20,000 - 30,000	3.3V	3	AT40K20LV-3AJI	84J	Industrial
			AT40K20LV-3AQI	100T1	(-40°C to 85°C)
			AT40K20LV-3RQI	100Q4	
			AT40K20LV-3BQI	144L1	
			AT40K20LV-3CQI	160Q1	
			AT40K20LV-3DQI	208Q1	
			AT40K20LV-2EQI	240Q1	

Note: 1. For military parts, contact Atmel at fpga@atmel.com

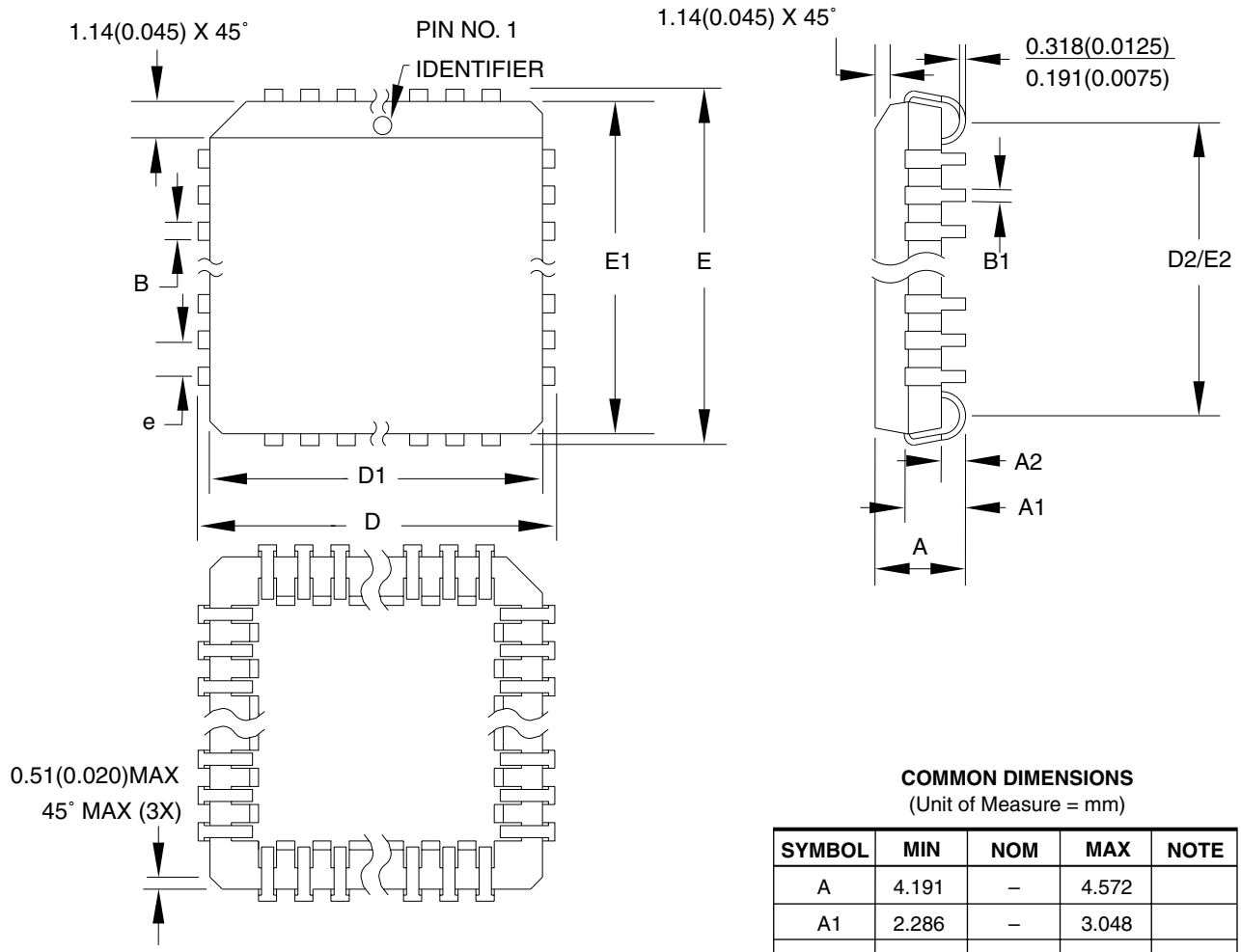
AT40K40/AT40K40LV Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
40,000 - 50,000	5.0V	2	AT40K40-2BQC AT40K40-2DQC AT40K40-2EQC AT40K40-2FQC AT40K40-2BGC	144Q1 208Q1 240Q1 304Q1 352C1	Commercial (0°C to 70°C)
40,000 - 50,000	5.0V	2	AT40K40-2BQI AT40K40-2DQI AT40K40-2EQI AT40K40-2FQI AT40K40-2BGI	144Q1 208Q1 240Q1 304Q1 352C1	Industrial (-40°C to 85°C)
40,000 - 50,000	3.3V	3	AT40K40LV-2BQC AT40K40LV-2DQC AT40K40LV-2EQC AT40K40LV-2FQC AT40K40LV-2BGC	144Q1 208Q1 240Q1 304Q1 352C1	Commercial (0°C to 70°C)
40,000 - 50,000	3.3V	3	AT40K40LV-2BQI AT40K40LV-2DQI AT40K40LV-2EQI AT40K40LV-2FQI AT40K40LV-2BGI	144Q1 208Q1 240Q1 304Q1 352C1	Industrial (-40°C to 85°C)

Note: 1. For military parts, contact Atmel at fpga@atmel.com.

Packaging Information

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

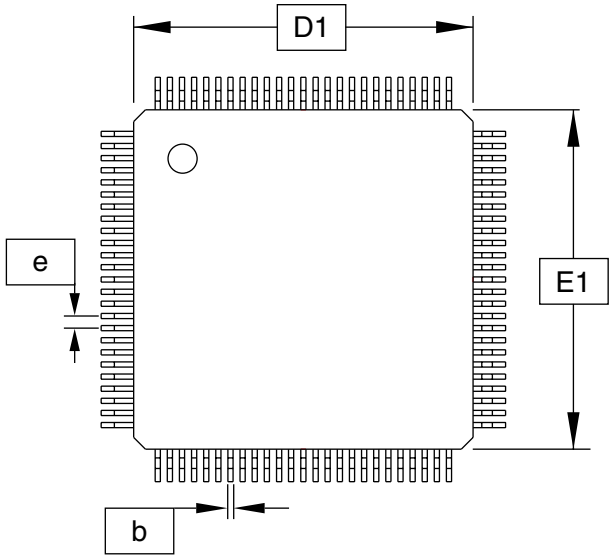
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

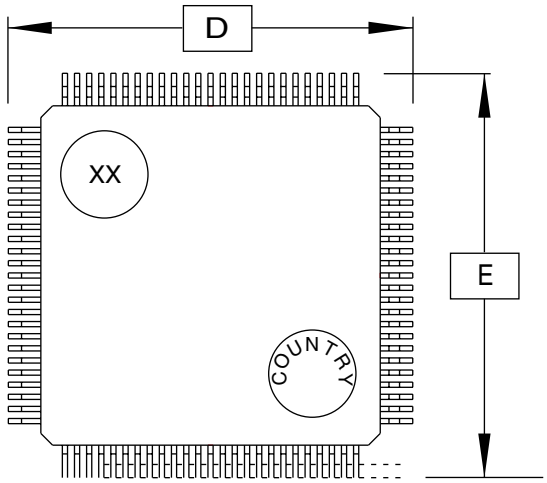
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

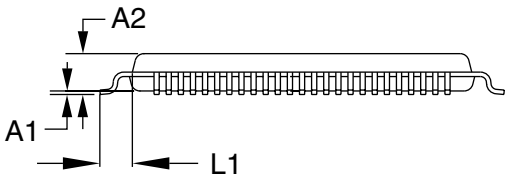
100T1 – TQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

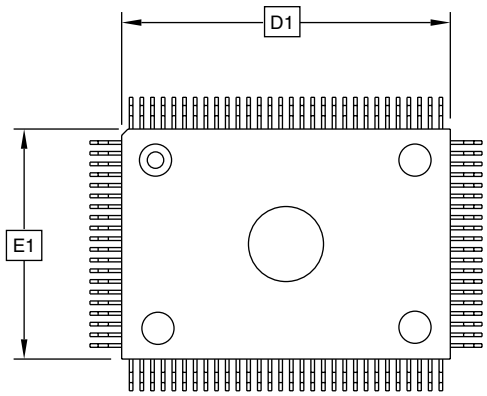
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	0.95	1.00	1.05	
D		16.00 BSC		
D1		14.00 BSC		2, 3
E		16.00 BSC		
E1		14.00 BSC		2, 3
e		0.50 BSC		
b	0.17	0.22	0.27	4, 5
L1		1.00 REF		

Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions, including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

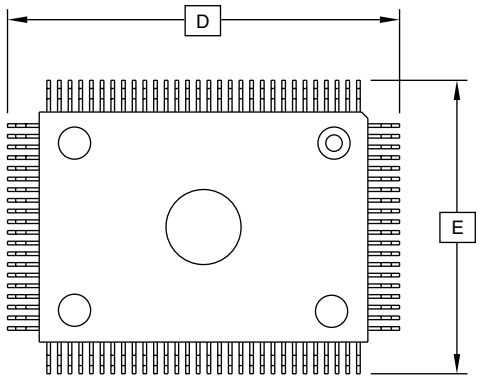
11/30/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100T1**, 100-lead (14 x 14 x 1.0 mm Body), Thin Plastic Quad Flat Pack (TQFP)	100T1	A

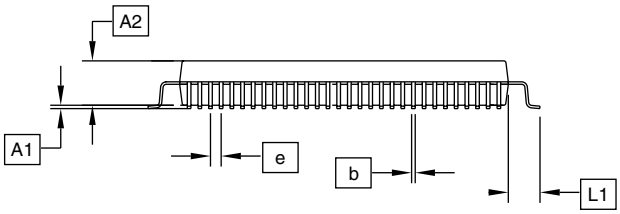
100Q4 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

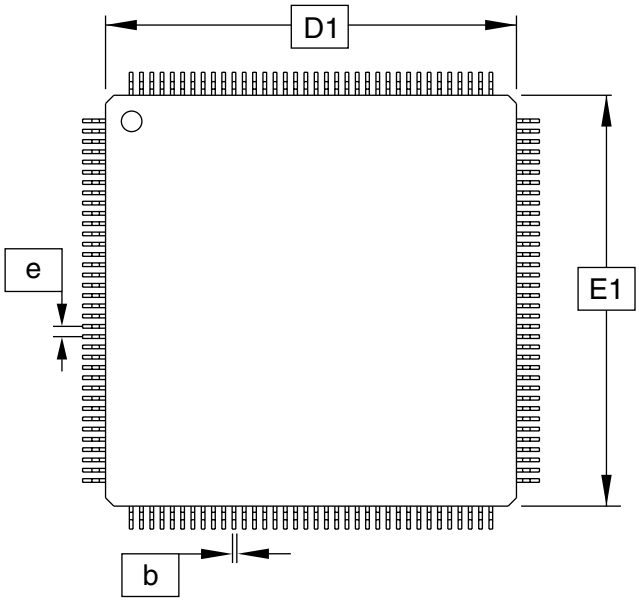
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	5
A2	2.50	2.70	2.90	
D	23.20 BSC			2
D1	20.00 BSC			3
E	17.20 BSC			2
E1	14.00 BSC			3
e	0.65 BSC			
b	0.22		0.40	4
L1	1.60 REF			

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-022, Variation GC-1, for additional information.
2. To be determined at seating plane.
3. Regardless of the relative size of the upper and lower body sections, dimensions D1 and E1 are determined at the largest feature of the body exclusive of mold Flash and gate burrs, but including any mismatch between the upper and lower sections of the molded body.
4. Dimension b does not include Dambar protrusion. The Dambar protrusion(s) shall not cause the lead width to exceed b maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
5. A1 is defined as the distance from the seating plane to the lowest point of the package body.

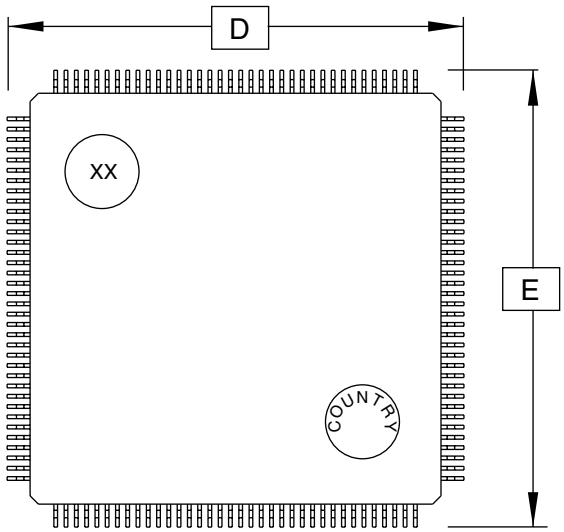
3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100Q4,** 100-lead, 14 x 20 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP)	100Q4	A

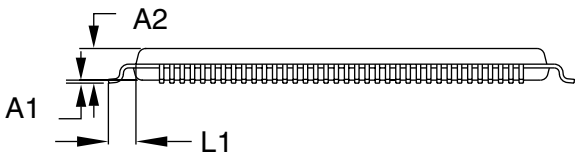
144L1 – LQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

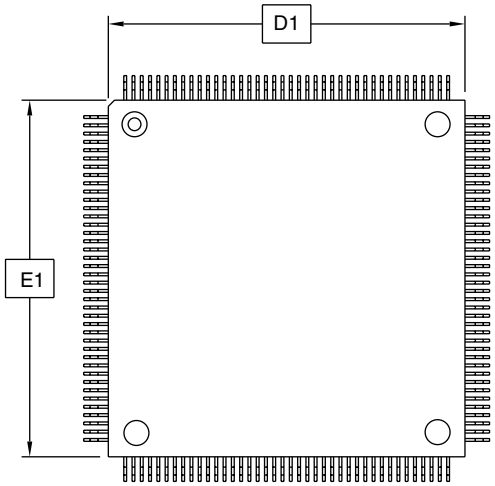
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	1.35	1.40	1.45	
D	22.00 BSC			
D1	20.00 BSC			2, 3
E	22.00 BSC			
E1	20.00 BSC			2, 3
e	0.50 BSC			
b	0.17	0.22	0.27	4, 5
L1	1.00 REF			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-026 for additional information.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

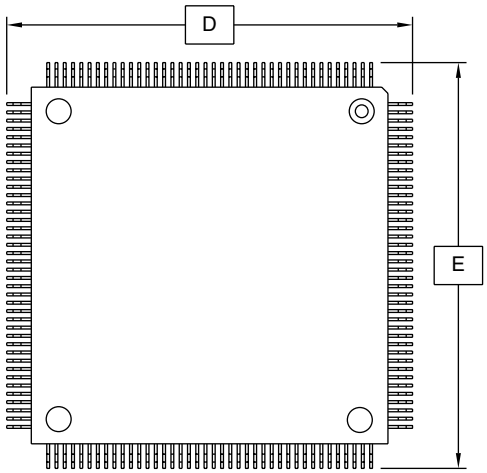
11/30/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**144L1**, 144-lead (20 x 20 x 1.4 mm Body), Low Profile Plastic Quad Flat Pack (LQFP)	144L1	A

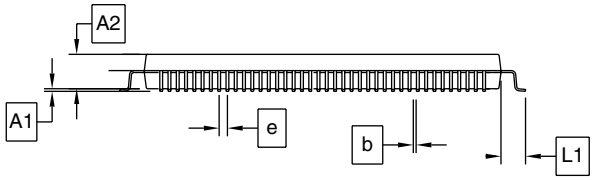
160Q1 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

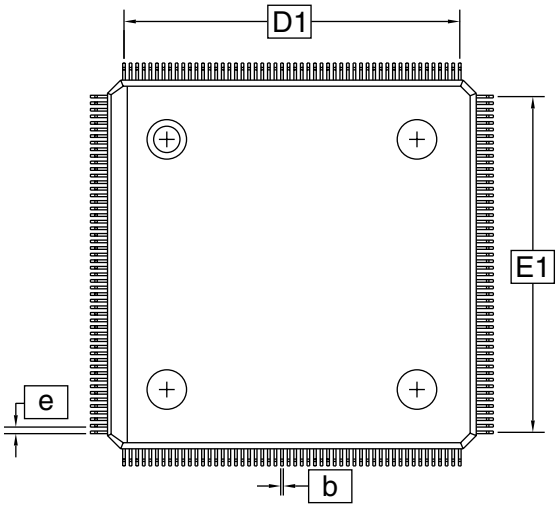
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	5
A2	3.20	3.40	3.60	
D	31.20 BSC			2
D1	28.00 BSC			3
E	31.20 BSC			2
E1	28.00 BSC			3
e	0.65 BSC			
b	0.22	–	0.40	4
L1	1.60 REF			

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-022, Variation DD-1, for additional information.
2. To be determined at seating plane.
3. Regardless of the relative size of the upper and lower body sections, dimensions D1 and E1 are determined at the largest feature of the body exclusive of mold Flash and gate burrs, but including any mismatch between the upper and lower sections of the molded body.
4. Dimension b does not include Dambar protrusion. The Dambar protrusion(s) shall not cause the lead width to exceed b maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
5. A1 is defined as the distance from the seating plane to the lowest point of the package body.

3/28/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**160Q1,** 160-lead, 28 x 28 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP)	160Q1	A

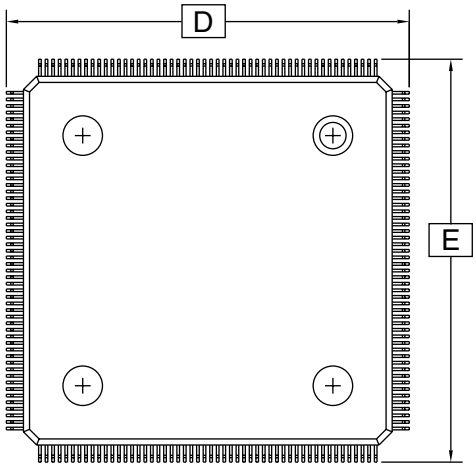
208Q1 – TQFP



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

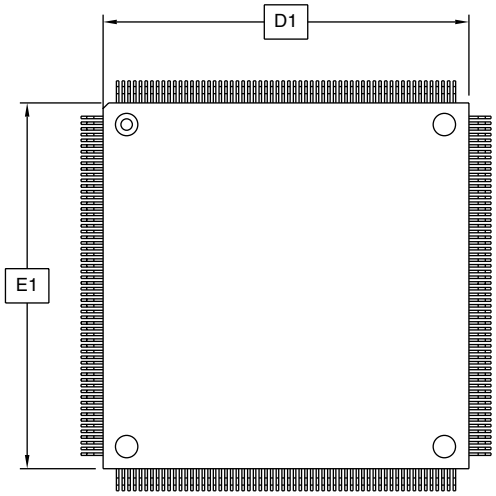
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25		0.50	
A2	3.20	3.40	3.60	
D	30.60 BSC			
D1	28.00 BSC			2, 3
E	30.60 BSC			
E1	28.00 BSC			2, 3
e	0.50 BSC			
b	0.17		0.27	4
L1	1.30 REF			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

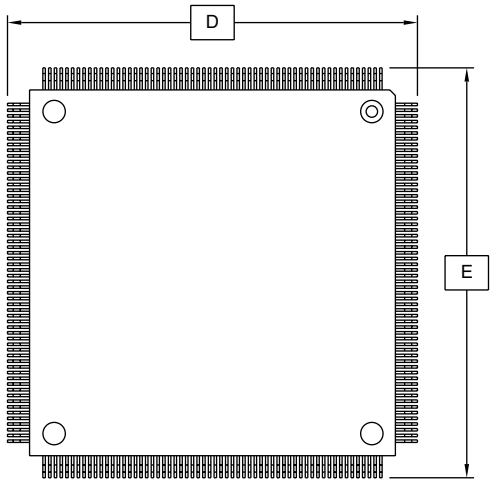
11/30/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**208Q1**, 208-lead (28 x 28 mm Body, 2.6 Form Opt.), Plastic Quad Flat Pack (PQFP)	208Q1	A

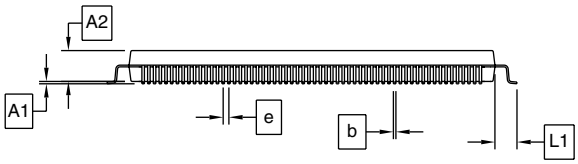
240Q1 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

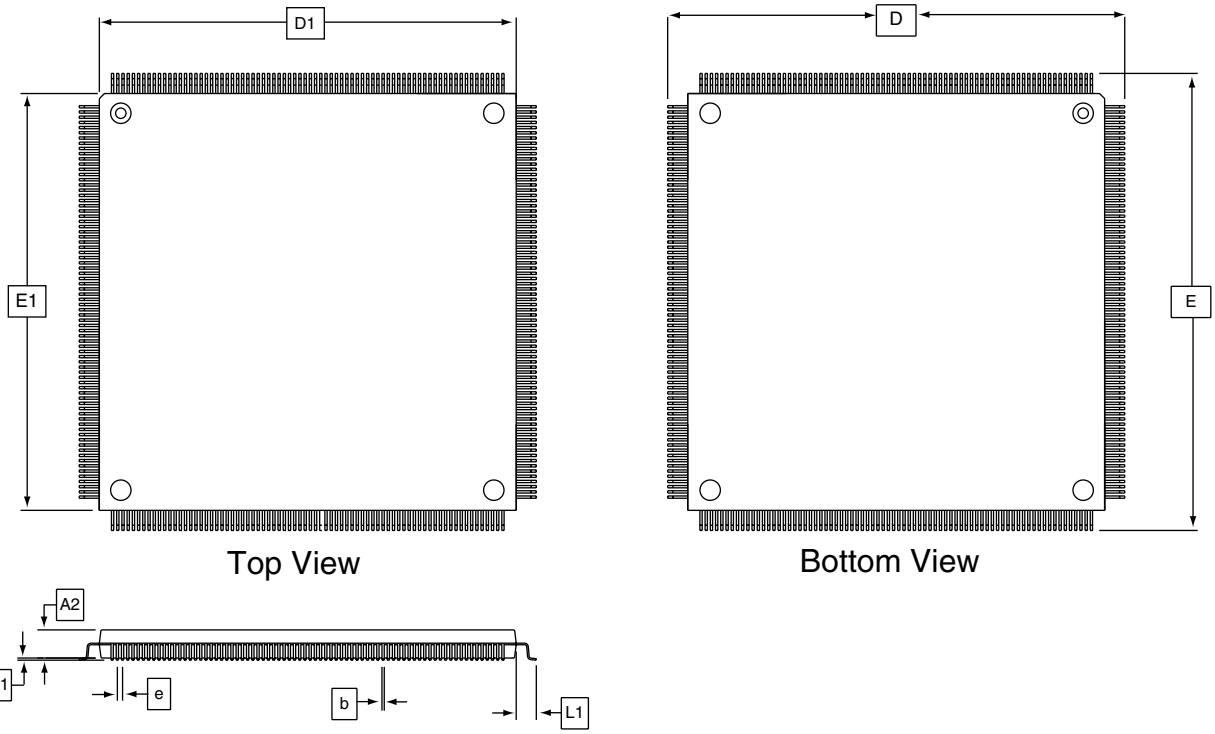
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		34.60 BSC		3
D1		32.00 BSC		2, 4
E		34.60 BSC		3
E1		32.00 BSC		2, 4
e		0.50 BSC		
b	0.17	–	0.27	5
L1		1.30 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-029, Variation GA, for additional information.
2. All dimensioning and tolerancing conforms to ASME Y14.5M-1994.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 shall be determined at datum plane.
5. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**240Q1,** 240-lead, 32 x 32 mm Body, 2.6 Form Opt., Plastic Quad Flat Pack (PQFP)	240Q1	A

304Q1 – PQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

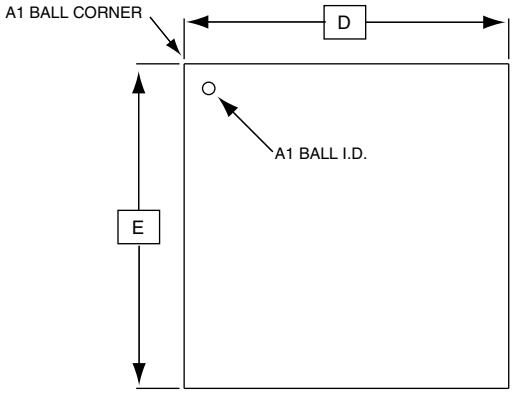
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.55	3.80	4.05	
D		42.60 BSC		3
D1		40.00 BSC		2, 4
E		42.60 BSC		3
E1		40.00 BSC		2, 4
e		0.50 BSC		
b	0.17	–	0.27	5
L1		1.30 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-029, Variation JA, for additional information.
2. All dimensioning and tolerancing conforms to ASME Y14.5M-1994.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 shall be determined at Datum plane.
5. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

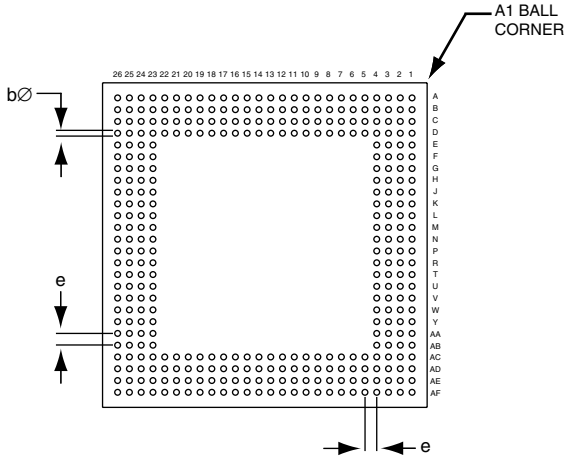
3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**304Q1,** 304-lead, 40 x 40 mm Body, 2.6 Form Opt., Plastic Quad Flat Pack (PQFP)	304Q1	A

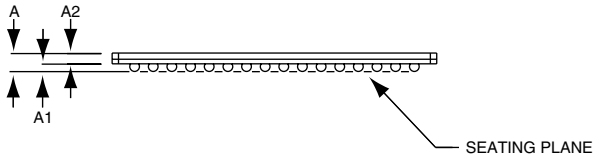
352C1 – SBGA



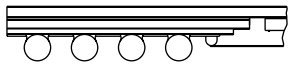
Top View



Bottom View
Die Side



Side View



Section View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		35.0 BSC		
E		35.0 BSC		
Matrix Size		26 x 26		
A	–	–	1.70	
A1	0.35	–	–	
A2	0.25	–	1.10	
bØ	0.60	0.75	0.90	
e		1.27 BSC		

Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-192, Variation BAR-2, for additional information.
2. JEDEC variations are based on fully populated ball arrays. Arrays can be depopulated as desired by removing balls from the fully populated array.

3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**352C1,** 352-ball, 35 x 35, Enhanced, Low-profile Square Ball Grid Array Package (SBGA)	352C1	A

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