CMOS ASYNCHRONOUS FIFO
256 x 9, 512 x 9 and 1,024 x 9

IDT7200L
IDT7201LA
IDT7202LA

FEATURES:

- **First-In/First-Out dual-port memory**
- **256 x 9 organization (IDT7200)**
- **512 x 9 organization (IDT7201)**
- **1,024 x 9 organization (IDT7202)**
- **Low power consumption**
  — Active: 440mW (max.)
  —Power-down: 28mW (max.)
- **Ultra high speed—12ns access time**
- **Asynchronous and simultaneous read and write**
- **Fully expandable by both word depth and/or bit width**
- **Pin and functionally compatible with 720X family**
- **Status Flags: Empty, Half-Full, Full**
- **Auto-retransmit capability**
- **High-performance CEMOS™ technology**
- **Military product compliant to MIL-STD-883, Class B**
- **Standard Military Drawing #5962-87531, 5962-89666, 5962-89863 and 5962-89536 are listed on this function**
- **Dual versions available in the TSSOP package. For more information, see IDT7280/7281/7282 data sheet**
  IDT7280 = 2 x IDT7200
  IDT7281 = 2 x IDT7201
  IDT7282 = 2 x IDT7202
- **Industrial temperature range (–40°C to +85°C) is available (plastic packages only)**

DESCRIPTION:

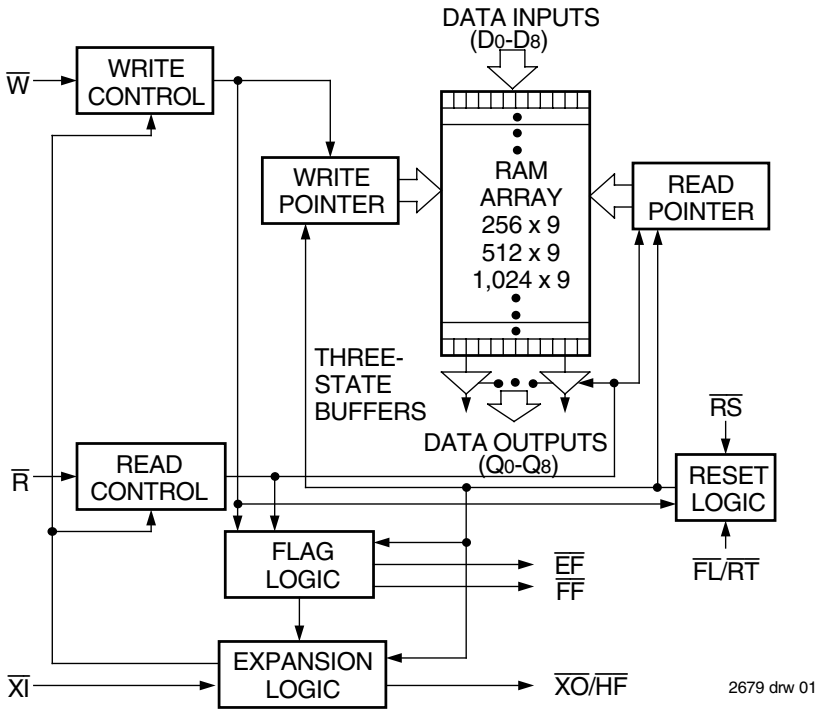
The IDT7200/7201/7202 are dual-port memories that load and empty data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed LOW to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

These FIFOs are fabricated using IDT's high-speed CMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

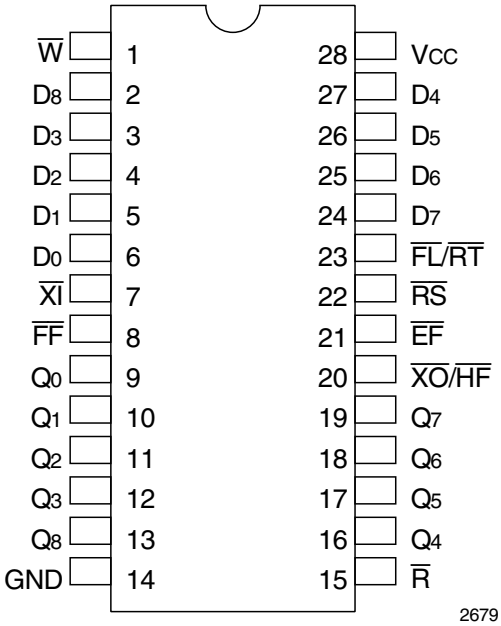
FUNCTIONAL BLOCK DIAGRAM



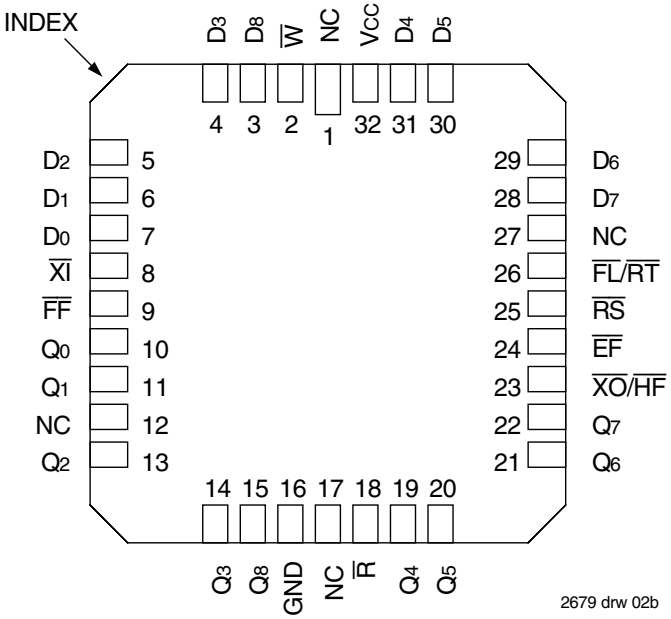
IDT and the IDT logo are registered trademarks of Integrated Device Technology, Inc.

© 2002 Integrated Device Technology, Inc. All rights reserved. Product specifications subject to change without notice.

PIN CONFIGURATIONS



2679 drw 02a



2679 drw 02b

Package Type	Reference Identifier	Order Code
PLASTIC DIP[1]	P28-1	P
PLASTIC THIN DIP	P28-2	TP
CERDIP[1]	D28-1	D
THIN CERDIP	D28-3	TD
SOIC	SO28-3	SO

TOP VIEW

Package Type	Reference Identifier	Order Code
LCC[1]	L32-1	L
PLCC	J32-1	J

TOP VIEW

NOTE:
1. The 600-mil-wide DIP (P28-1 and D28-1) and LCC are not available for the IDT7200.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	–50 to +50	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Commercial/Industrial/Military	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}[1]	Input High Voltage Com'l/Ind'l	2.0	—	—	V
V_{IH}[1]	Input High Voltage Military	2.2	—	—	V
V_{IL}[2]	Input Low Voltage Commercial/Industrial/Military	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C
T_A	Operating Temperature Industrial	–40	—	85	°C
T_A	Operating Temperature Military	–55	—	125	°C

NOTES:
1. For $\overline{RT}/\overline{RS}/\overline{XI}$ input, V_{IH} = 2.6V (commercial).
   For $\overline{RT}/\overline{RS}/\overline{XI}$ input, V_{IH} = 2.8V (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0ºC to +70ºC; Industrial: V_{CC} = 5V ± 10%, T_A = –40ºC to +85ºC; Military: V_{CC} = 5V ± 10%, T_A = –55ºC to +125ºC)

Symbol	Parameter	IDT7200L IDT7201LA IDT7202LA Com'l & Ind'l[1] t_A = 12, 15, 20, 25, 35, 50 ns		IDT7200L IDT7201LA IDT7202LA Military[2] t_A = 20, 30, 50, 80 ns		Unit
		Min.	Max.	Min.	Max.	
I_{LI}[3]	Input Leakage Current (Any Input)	–1	1	–10	10	µA
I_{LO}[4]	Output Leakage Current	–10	10	–10	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	0.4	—	0.4	V
I_{CC1}[5,6,7]	Active Power Supply Current	—	80	—	100	mA
I_{CC2}[5,8]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	5	—	15	mA

NOTES:
1. Industrial temperature range product for the 15ns and 25 ns speed grades are available as a standard device.
2. Military speed grades of 50ns and 80ns are only available for the IDT7201LA.
3. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
4. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
5. Tested with outputs open (I_{OUT} = 0).
6. Tested at f = 20 MHz.
7. Typical I_{CC1} = 15 + 2*fs + 0.02*C_L*fs (in mA) with V_{CC} = 5V, T_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
8. All Inputs = V_{CC} - 0.2V or GND + 0.2V.

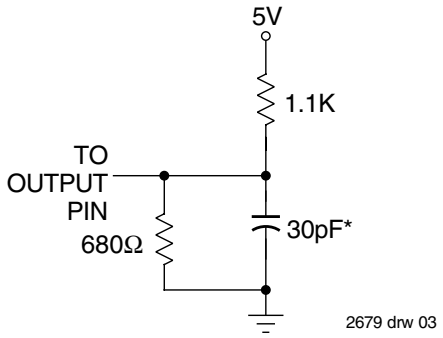
CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. Characterized values, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



or equivalent circuit

Figure 1. Output Load

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Industrial: V_{CC} = 5V ± 10%, T_A = –40°C to +85°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commercial		Com'l & Ind'l[2]		Com'l & Mil.		Com'l & Ind'l[2]		
		IDT7200L12 IDT7201LA12 IDT7202LA12		IDT7200L15 IDT7201LA15 IDT7202LA15		IDT7200L20 IDT7201LA20 IDT7202LA20		IDT7200L25 IDT7201LA25 IDT7202LA25		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	50	—	40	—	33.3	—	28.5	MHz
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	ns
t_A	Access Time	—	12	—	15	—	20	—	25	ns
t_{RR}	Read Recovery Time	8	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[3]	12	—	15	—	20	—	25	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[4]	3	—	3	—	3	—	3	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[4,5]	5	—	5	—	5	—	5	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[4]	—	12	—	15	—	15	—	18	ns
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	ns
t_{WPW}	Write Pulse Width[3]	12	—	15	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	8	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	9	—	11	—	12	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	20	—	25	—	30	—	35	—	ns
t_{RS}	Reset Pulse Width[3]	12	—	15	—	20	—	25	—	ns
t_{RSS}	Reset Set-up Time[4]	12	—	15	—	20	—	25	—	ns
t_{RSR}	Reset Recovery Time	8	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	20	—	25	—	30	—	35	—	ns
t_{RT}	Retransmit Pulse Width[3]	12	—	15	—	20	—	25	—	ns
t_{RTS}	Retransmit Set-up Time[4]	12	—	15	—	20	—	25	—	ns
t_{RTR}	Retransmit Recovery Time	8	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	12	—	25	—	30	—	35	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	17	—	25	—	30	—	35	ns
t_{RTF}	Retransmit Low to Flags Valid	—	20	—	25	—	30	—	35	ns
t_{REF}	Read Low to Empty Flag Low	—	12	—	15	—	20	—	25	ns
t_{RFF}	Read High to Full Flag High	—	14	—	15	—	20	—	25	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	12	—	15	—	20	—	25	—	ns
t_{WEF}	Write High to Empty Flag High	—	12	—	15	—	20	—	25	ns
t_{WFF}	Write Low to Full Flag Low	—	14	—	15	—	20	—	25	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	17	—	25	—	30	—	35	ns
t_{RHF}	Read High to Half-Full Flag High	—	17	—	25	—	30	—	35	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	12	—	15	—	20	—	25	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	12	—	15	—	20	—	25	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	12	—	15	—	20	—	25	ns
t_{XI}	$\overline{XI}$ Pulse Width[3]	12	—	15	—	20	—	25	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	8	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	8	—	10	—	10	—	10	—	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Industrial temperature range product for 15ns and 25ns speed grades are available as a standard device.
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode

AC ELECTRICAL CHARACTERISTICS[1] (Continued)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Industrial: V_{CC} = 5V ± 10%, T_A = –40°C to +85°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Military		Commercial		Com'l & Mil.[2]		Military[2]		
		IDT7200L30 IDT7201LA30 IDT7202LA30		IDT7200L35 IDT7201LA35 IDT7202LA35		IDT7200L50 IDT7201LA50 IDT7202LA50		IDT7201LA80		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	25	—	22.2	—	15	—	10	MHz
t_{RC}	Read Cycle Time	40	—	45	—	65	—	100	—	ns
t_A	Access Time	—	30	—	35	—	50	—	80	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	20	—	ns
t_{RPW}	Read Pulse Width[3]	30	—	35	—	50	—	80	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[4]	3	—	3	—	3	—	3	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[4,5]	5	—	5	—	5	—	5	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[4]	—	20	—	20	—	30	—	30	ns
t_{WC}	Write Cycle Time	40	—	45	—	65	—	100	—	ns
t_{WPW}	Write Pulse Width[3]	30	—	35	—	50	—	80	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	15	—	20	—	ns
t_{DS}	Data Set-up Time	18	—	18	—	30	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	10	—	ns
t_{RSC}	Reset Cycle Time	40	—	45	—	65	—	100	—	ns
t_{RS}	Reset Pulse Width[3]	30	—	35	—	50	—	80	—	ns
t_{RSS}	Reset Set-up Time[4]	30	—	35	—	50	—	80	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	40	—	45	—	65	—	100	—	ns
t_{RT}	Retransmit Pulse Width[3]	30	—	35	—	50	—	80	—	ns
t_{RTS}	Retransmit Set-up Time[4]	30	—	35	—	50	—	80	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	40	—	45	—	65	—	100	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	40	—	45	—	65	—	100	ns
t_{RTF}	Retransmit Low to Flags Valid	—	40	—	45	—	65	—	100	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	30	—	45	—	60	ns
t_{RFF}	Read High to Full Flag High	—	30	—	30	—	45	—	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	30	—	35	—	50	—	80	—	ns
t_{WEF}	Write High to Empty Flag High	—	30	—	30	—	45	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	30	—	30	—	45	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	40	—	45	—	65	—	100	ns
t_{RHF}	Read High to Half-Full Flag High	—	40	—	45	—	65	—	100	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	30	—	35	—	50	—	80	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	30	—	35	—	50	—	80	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	30	—	35	—	50	—	80	ns
t_{XI}	$\overline{XI}$ Pulse Width[3]	30	—	35	—	50	—	80	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	10	—	15	—	15	—	ns

NOTES:
1. Timings referenced as in AC Test Conditions
2. Military speed grades of 50ns and 80ns are only available for IDT7201LA.
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D_0 – D_8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to HIGH after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (Q_0–Q_8) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7200/7201A/7202A can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than 256/512/1,024 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go LOW after 256 writes for IDT7200, 512 writes for the IDT7201A and 1,024 writes for the IDT7202A.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

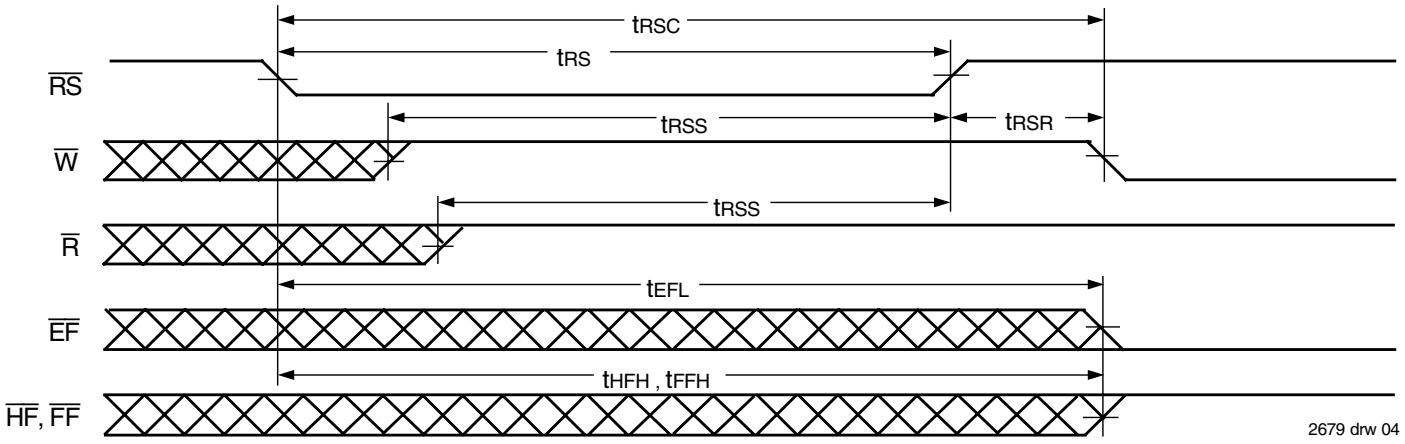
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0 – Q_8)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a HIGH state.



NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

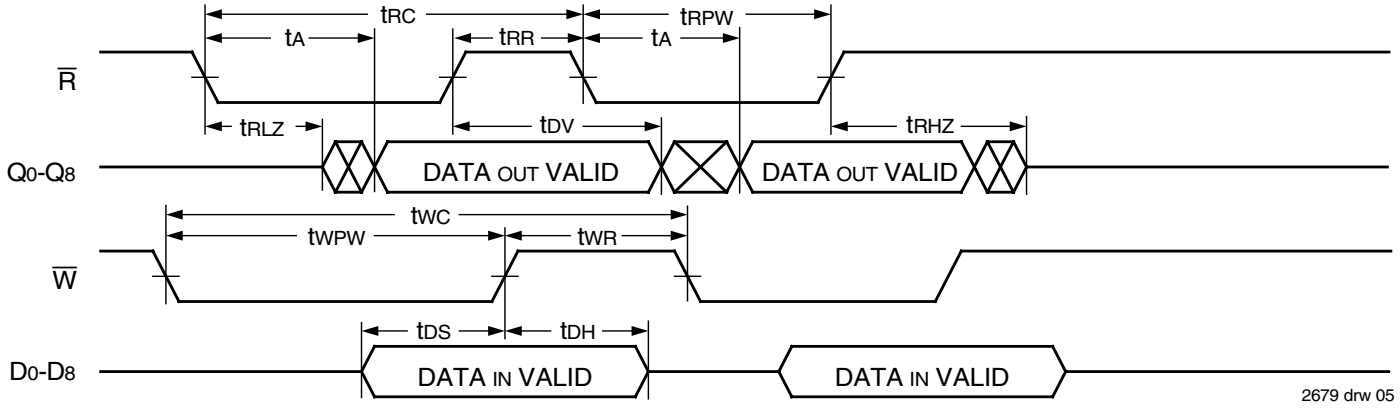


Figure 3. Asynchronous Write and Read Operation

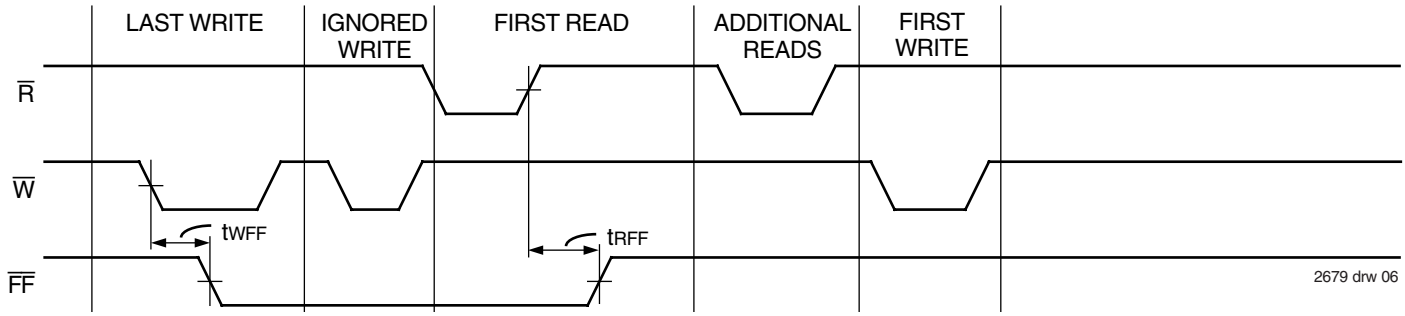


Figure 4. Full Flag From Last Write to First Read

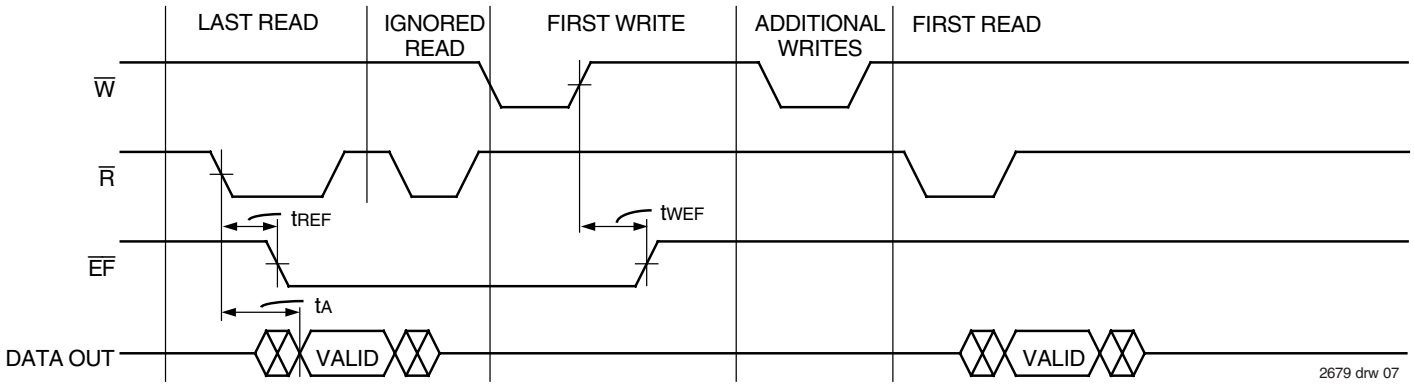


Figure 5. Empty Flag From Last Read to First Write

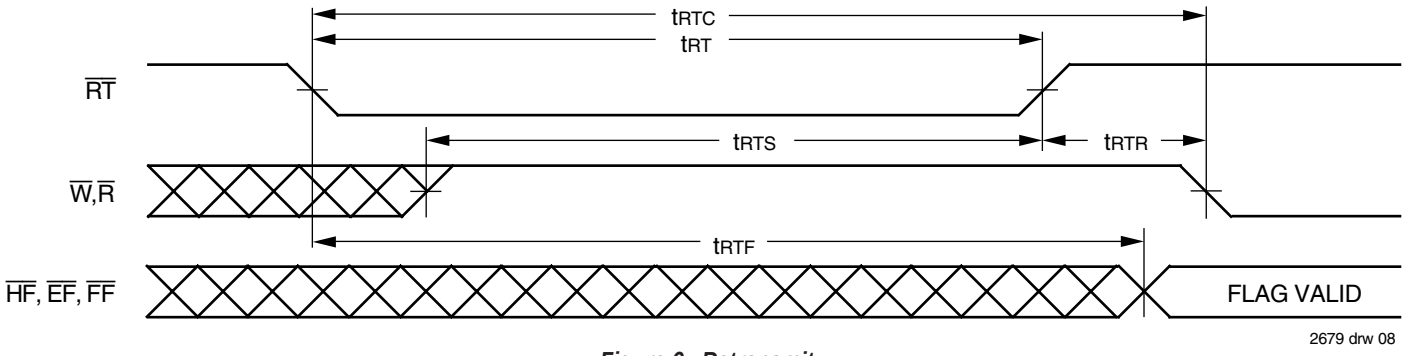


Figure 6. Retransmit

Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse

Figure 8. Minimum Timing for a Full Flag Coincident Write Pulse

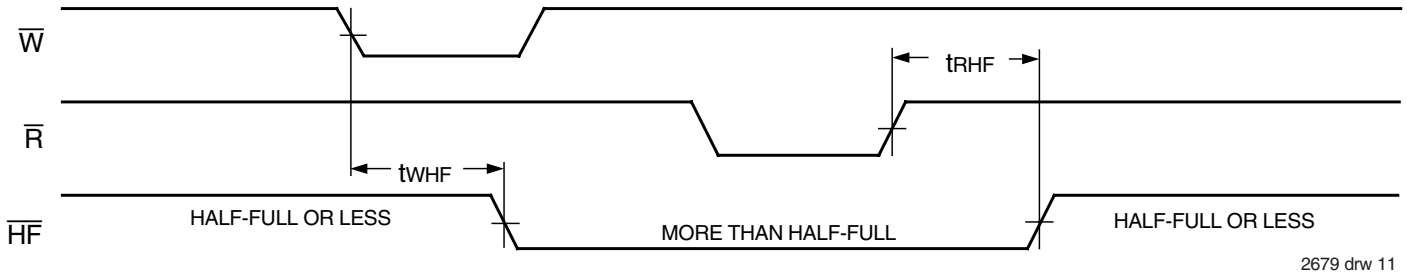


Figure 9. Half-Full Flag Timing

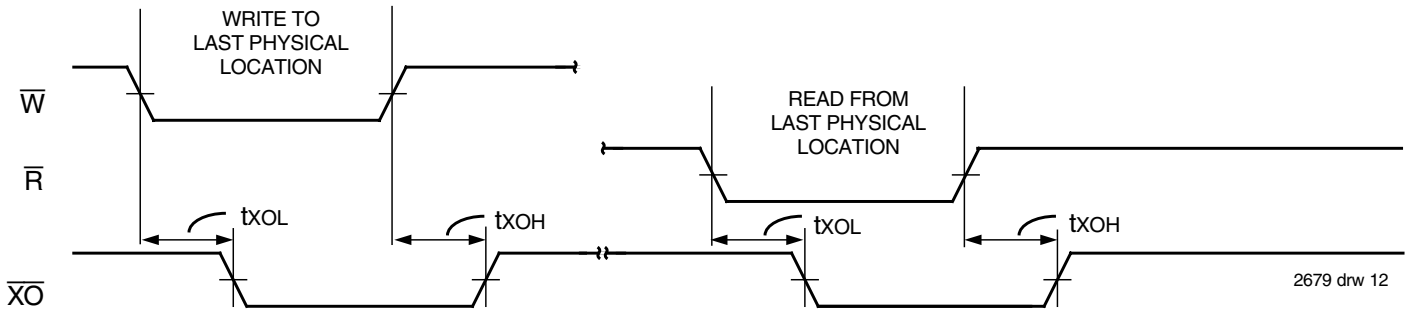


Figure 10. Expansion Out

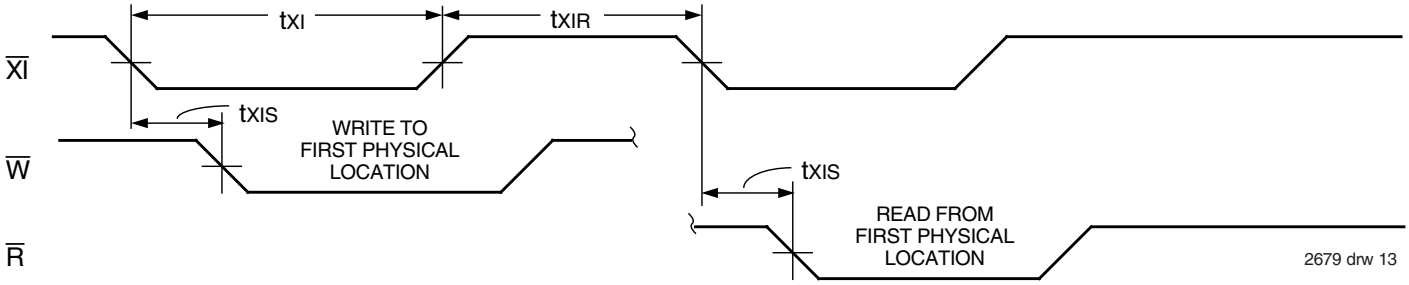


Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

SINGLE DEVICE MODE

A single IDT7200/7201A/7202A may be used when the application requirements are for 256/512/1,024 words or less. These devices are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

DEPTH EXPANSION

The IDT7200/7201A/7202A can easily be adapted to applications when the requirements are for greater than 256/512/1,024 words. Figure 14 demonstrates Depth Expansion using three IDT7200/7201A/7202As. Any depth can be attained by adding additional IDT7200/7201A/7202As. These FIFOs operate in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7200/7201A/7202As. Any word width can be attained by adding additional IDT7200/7201A/7202As (Figure 13).

BIDIRECTIONAL OPERATION

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7200/7201A/7202As as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

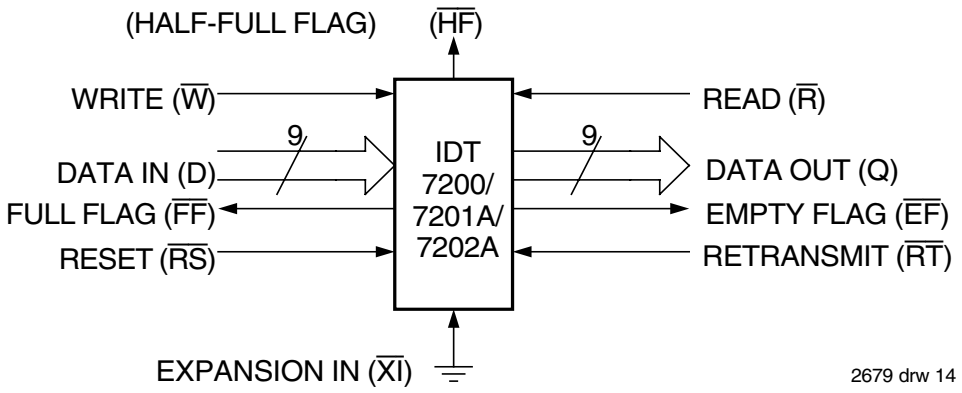


Figure 12. Block Diagram of Single 256 x 9, 512 x 9, 1,024 x 9 FIFO

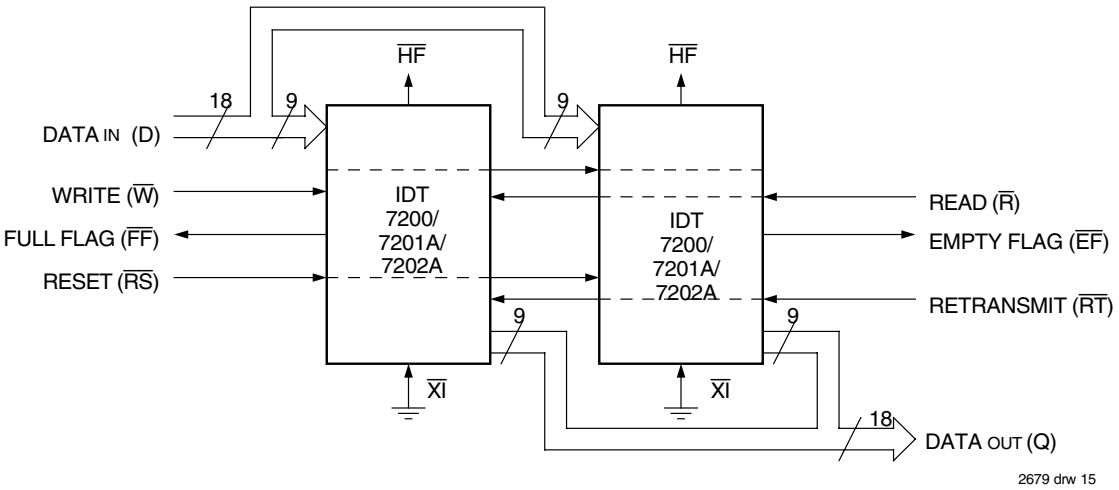


Figure 13. Block Diagram of 256 x 18, 512 x 18, 1,024 x 18 FIFO Memory Used in Width Expansion Mode

TABLE 1 — RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if flag is HIGH.

TABLE 2 — RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

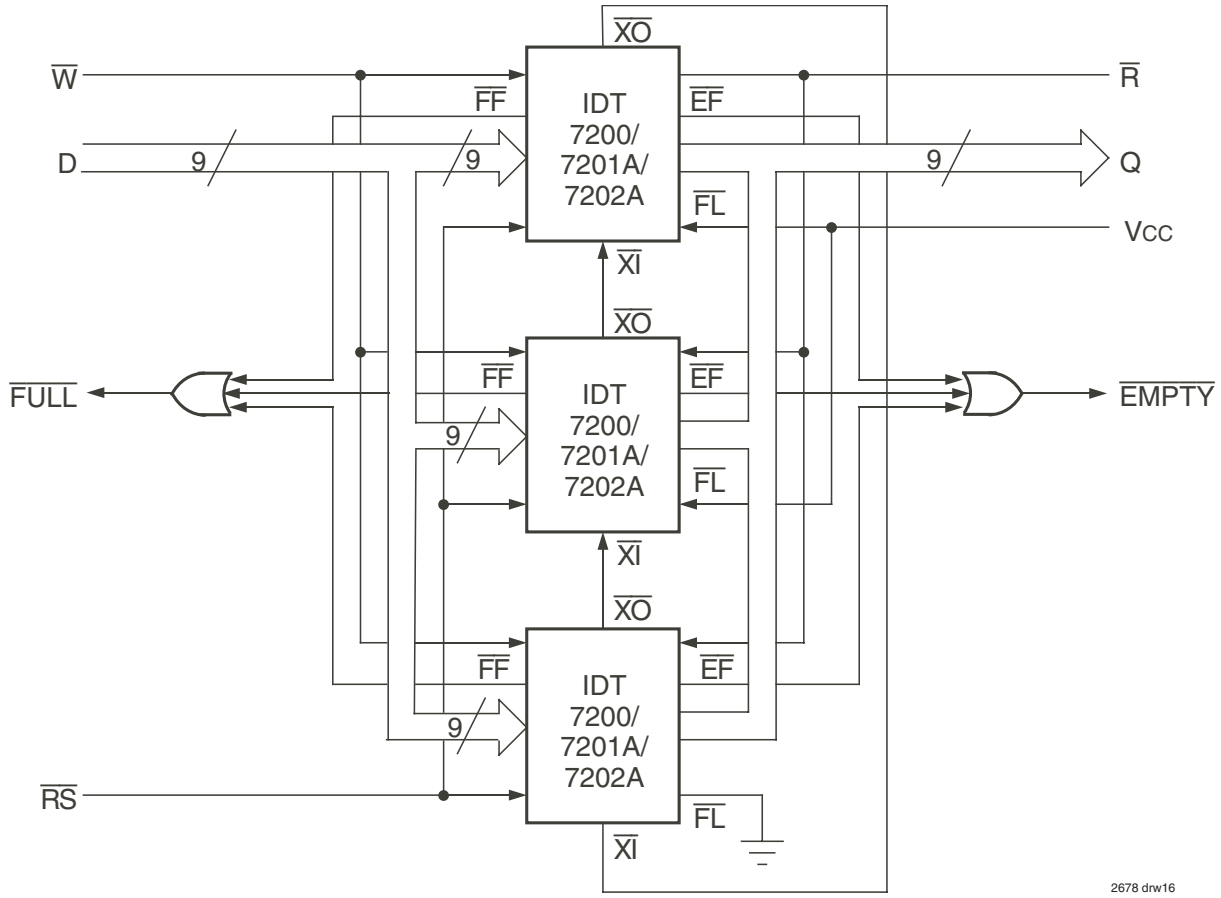
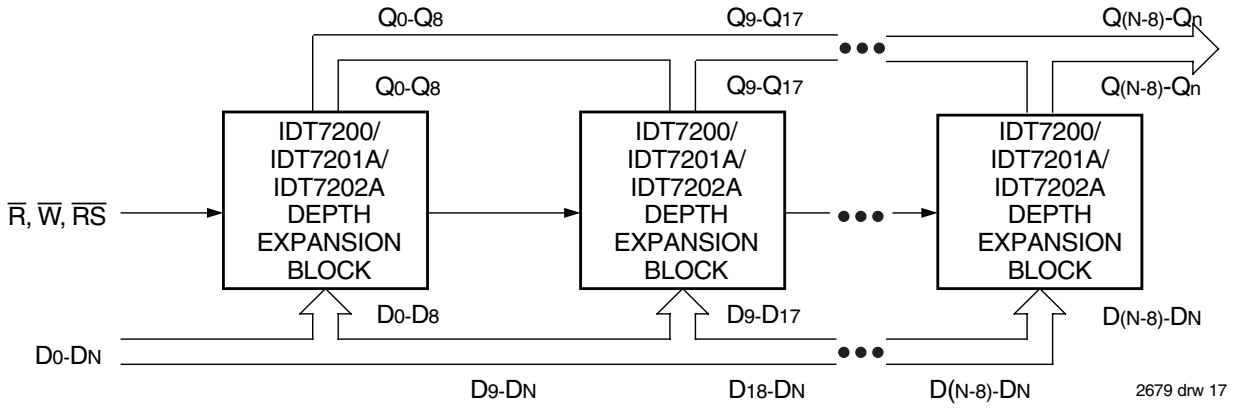


Figure 14. Block Diagram of 768 x 9, 1,536 x 9, 3,072 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

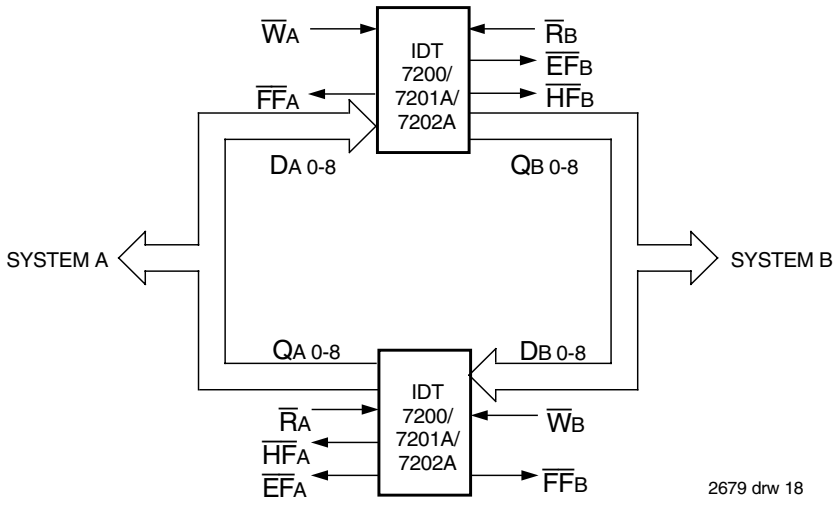


Figure 16. Bidirectional FIFO Mode

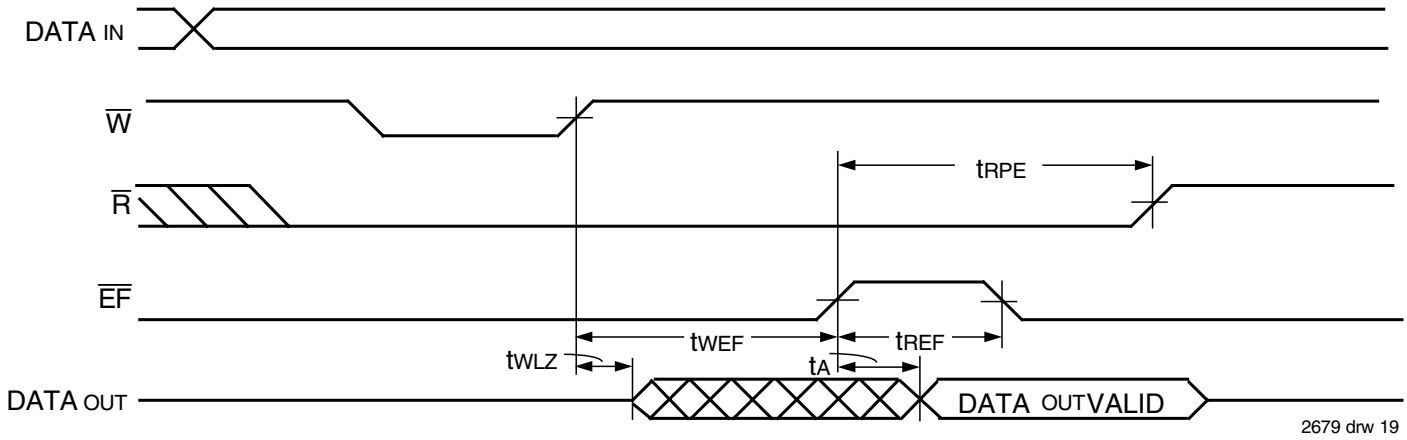


Figure 17. Read Data Flow-Through Mode

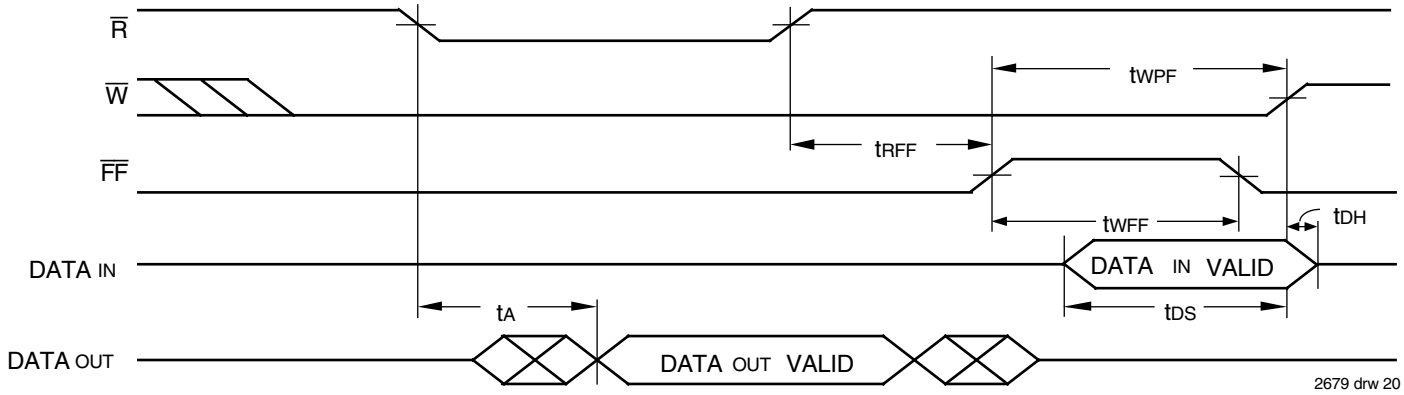


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT XXXX X XXX X X

Device Type | Power | Speed | Package | Process/ Temperature Range

Process/ Temperature Range

Blank	Commercial (0°C to +70°C)
I[1]	Industrial (-40°C to +85°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

P	Plastic DIP		P28-1	(7201 & 7202 Only)
TP	Plastic Thin DIP		P28-2	
D	CERDIP		D28-1	(7201 & 7202 Only)
TD	Thin CERDIP		D28-3	
J	Plastic Leaded Chip Carrier	PLCC	J32-1	
SO	SOIC		SO28-3	
L	Leadless Chip Carrier	LCC	L32-1	(7201 & 7202 Only)

Speed (Access Time (t_A) Speed in Nanoseconds)

12	Commercial Only
15	Commercial and Industrial
20	Commercial and Military
25	Commercial and Industrial
30	Military Only
35	Commercial Only
50	Commercial and (Military only for 7201)
80	Military only for 7201

Power

LA[2]	Low Power

Device Type

7200	256 x 9-Bit FIFO
7201	512 x 9-Bit FIFO
7202	1,024 x 9-Bit FIFO
7280	256 x 9-Bit DUAL FIFO
7281	512 x 9-Bit DUAL FIFO
7282	1,024 x 9-Bit DUAL FIFO

See 7280/7281/7282 data sheet for details

2679 drw 21

NOTES:
1. Industrial temperature range product is available for the 15ns and 25ns as a standard product.
2. "A" to be included for IDT7201 and IDT7202 ordering part number.

DATASHEET DOCUMENT HISTORY

05/02/2001 pgs. 1, 2, 3, 4, 5 and 14.

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for TECH SUPPORT:
408-330-1753
e-mail: FIFOhelp@idt.com

НИОКР СИСТЕМС

ООО «НИОКРсистемс» - это оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов. Реализуемая нашей компанией продукция насчитывает более полумиллиона наименований.

Благодаря этому наша компания предлагает к поставке практически не ограниченный ассортимент компонентов как оптовыми, мелкооптовыми партиями, так и в розницу.

Благодаря развитой сети поставщиков, помогаем в поиске и приобретении экзотичных или снятых с производства компонентов.

Наша компания это:

- Гарантия качества поставляемой продукции
- Широкий ассортимент
- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование
- Работаем по 275 ФЗ

ООО «НИОКР СИТЕМС»
Москва, 125362, Россия, ул. Вишневая, д. 9, к. 1, Блок 104 а и 104 в

Телефон: 8 (495) 268-14-82
Email: n@nsistems.ru

ИНН: 7735154786
ОГРН: 1167746717709