FAIRCHILD SEMICONDUCTOR®

May 2007

74VCX163245
Low Voltage 16-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

Features

- Bidirectional interface between busses ranging from 1.65V to 3.6V
- Supports Live Insertion and Withdrawal(1)
- Static Drive (I_{OH}/I_{OL})
  - ±24mA @ 3.0V V_{CC}
  - ±18mA @ 2.3V V_{CC}
  - ±6mA @ 1.65V V_{CC}
- Uses proprietary Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 16245
- Latchup performance exceeds 300mA
- ESD performance:
  - Human Body Model >2000V
  - Machine model >200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note:

1. To ensure the high impedance state during power up or power down, OE_n should be tied to V_{CCB} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

General Description

The VCX163245 is a dual supply, 16-bit translating transceiver that is designed for 2 way asynchronous communication between busses at different supply voltages by providing true signal translation. The supply rails consist of V_{CCA}, which is a higher potential rail operating at 2.3V to 3.6V and V_{CCB}, which is the lower potential rail operating at 1.65V to 2.7V. (V_{CCB} must be less than or equal to V_{CCA} for proper device operation). This dual supply design allows for translation from 1.8V to 2.5V busses to busses at a higher potential, up to 3.3V.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable ($\overline{OE}$) input, when HIGH, disables both A and B Ports by placing them in a High-Z condition. The A Port interfaces with the higher voltage bus (2.7V to 3.3V); The B Port interfaces with the lower voltage bus (1.8V to 2.5V). Also the VCX163245 is designed so that the control pins ($T/\overline{R}_n$, $\overline{OE}_n$) are supplied by V_{CCB}.

The 74VCX163245 is suitable for mixed voltage applications such as notebook computers using a 1.8V CPU and 3.3V peripheral components. It is fabricated with an Advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Ordering Information

Order Number	Package Number	Package Description
74VCX163245G(2)(3)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74VCX163245MTD(3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Notes:

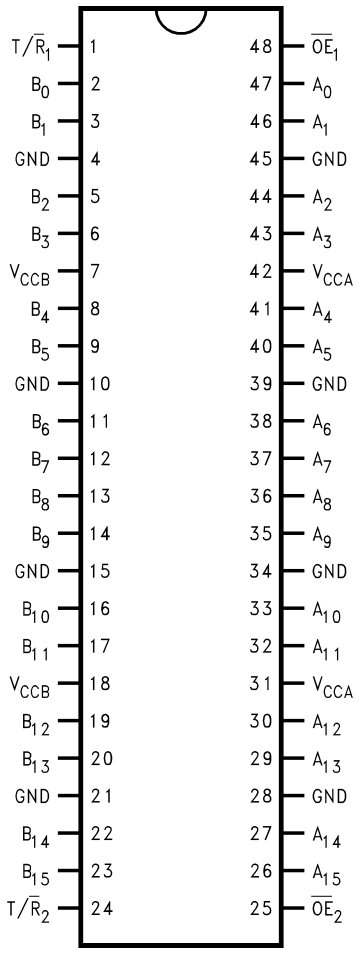
2. Ordering code “G” indicates Trays.
3. Device also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

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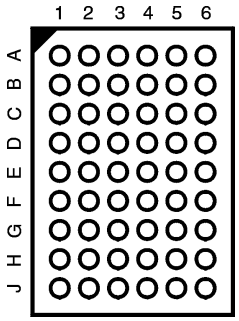
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Connection Diagram

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

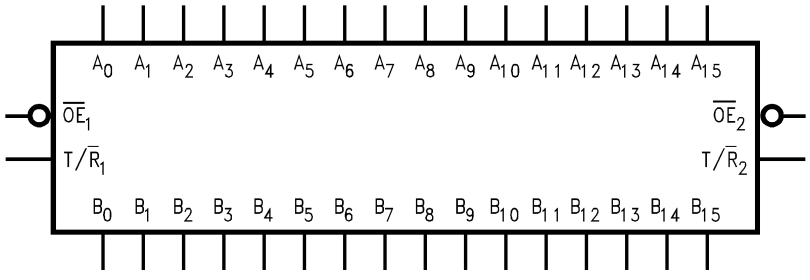
FBGA Pin Assignments

	1	2	3	4	5	6
A	B_0	NC	$T/\overline{R}_1$	$\overline{OE}_1$	NC	A_0
B	B_2	B_1	NC	NC	A_1	A_2
C	B_4	B_3	V_{CCB}	V_{CCA}	A_3	A_4
D	B_6	B_5	GND	GND	A_5	A_6
E	B_8	B_7	GND	GND	A_7	A_8
F	B_{10}	B_9	GND	GND	A_9	A_{10}
G	B_{12}	B_{11}	V_{CCB}	V_{CCA}	A_{11}	A_{12}
H	B_{14}	B_{13}	NC	NC	A_{13}	A_{14}
J	B_{15}	NC	$T/\overline{R}_2$	$\overline{OE}_2$	NC	A_{15}

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or 3-STATE Outputs
B_0–B_{15}	Side B Inputs or 3-STATE Outputs
NC	No Connect

Logic Diagram



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Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial (HIGH or LOW, inputs may not float)

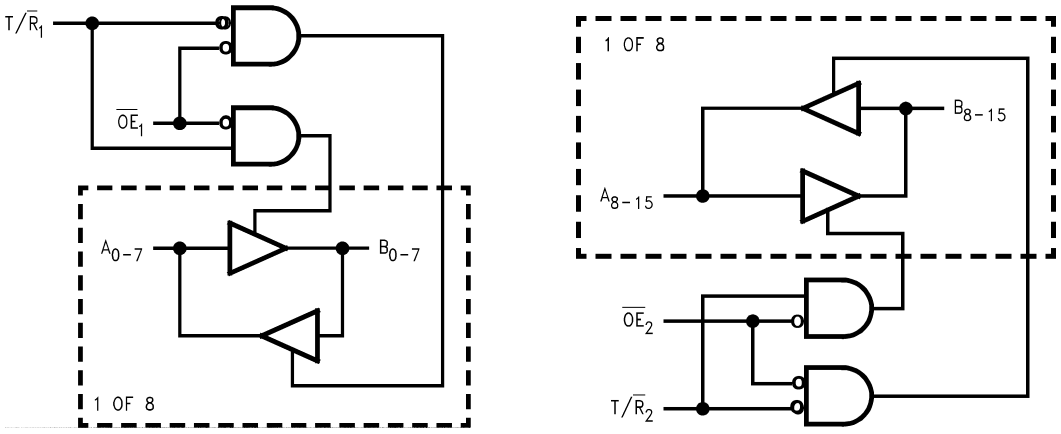
Z = High Impedance

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

VCX163245 Translator Power Up Sequence Recommendations

To guard against power up problems, some simple guidelines need to be adhered to. The VCX163245 is designed so that the control pins ($T/\overline{R}_n$, $\overline{OE}_n$) are supplied by V_{CCB}. Therefore the first recommendation is to begin by powering up the control side of the device, V_{CCB}. The $\overline{OE}_n$ control pins should be ramped with or ahead of V_{CCB}, this will guard against bus contentions and oscillations as all A Port and B Port outputs will be disabled. To ensure the high impedance state during power up or power down, $\overline{OE}_n$ should be tied to V_{CCB} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver. Second, the $T/\overline{R}_n$ control pins should be placed at logic LOW (0V) level, this will ensure that the B-side bus pins are configured as inputs to help guard against bus contention and oscillations. B-side Data Inputs should be driven to a valid logic level (0V or V_{CCB}), this will prevent excessive current draw and oscillations. V_{CCA} can then be powered up after V_{CCB}, however V_{CCA} must be greater than or equal to V_{CCB} to ensure proper device operation. Upon completion of these steps the device can then be configured for the users desired operation. Following these steps will help to prevent possible damage to the translator device as well as other system components.

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CCA}	Supply Voltage	–0.5V to +4.6V
V_{CCB}		–0.5V to V_{CCA}
V_I	DC Input Voltage	–0.5V to +4.6V
$V_{I/O}$	DC Output Voltage	
	Outputs 3-STATE	–0.5V to +4.6V
	A_n Output Active(4)	–0.5V to V_{CCA} + 0.5V
	B_n Output Active(4)	–0.5V to V_{CCB} + 0.5V
I_{IK}	DC Input Diode Current, $V_I < 0V$	–50mA
I_{OK}	DC Output Diode Current	
	$V_O < 0V$	–50mA
	$V_O > V_{CC}$	+50mA
I_{OH}/I_{OL}	DC Output Source/Sink Current	±50mA
	DC V_{CC} or Ground Current	±100mA
I_{CC} or Ground	Supply Pin	
T_{STG}	Storage Temperature	–65°C to +150°C

Recommended Operating Conditions(5)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CCA}	Power Supply(6)	2.3V to 3.6V
V_{CCB}		1.65V to 2.7V
V_I	Input Voltage () @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCB}
$V_{I/O}$	Input/Output Voltage ()	
	A_n	0V to V_{CCA}
	B_n	0V to V_{CCB}
I_{OH}/I_{OL}	Output Current in I_{OH}/I_{OL}	
	V_{CCA} = 3.0V to 3.6V	±24mA
	V_{CCA} = 2.3V to 2.7V	±18mA
	V_{CCB} = 2.3V to 2.7V	±18mA
	V_{CCB} = 1.65V to 1.95V	±6mA
T_A	Free Air Operating Temperature	–40°C to +85°C
$\Delta t / \Delta V$	Minimum Input Edge Rate, V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10ns/V

Notes:

4. I_O Absolute Maximum Rating must be observed.
5. Unused inputs or I/O pins must be held HIGH or LOW. They may not float.
6. Operation requires: $V_{CCB} \leq V_{CCA}$

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DC Electrical Characteristics ($1.65V < V_{CCB} \le 1.95V$, $2.3V < V_{CCA} \le 2.7V$)

Symbol	Parameter		V_{CCB} (V)	V_{CCA} (V)	Conditions	Min.	Max.	Units
V_{IHA}	HIGH Level Input Voltage	A_n	1.65–1.95	2.3–2.7		1.6		V
V_{IHB}		B_n, T/$\overline{R}$, $\overline{OE}$	1.65–1.95	2.3–2.7		0.65 x V_{CCB}		V
V_{ILA}	LOW Level Input Voltage	A_n	1.65–1.95	2.3–2.7			0.7	V
V_{ILB}		B_n, T/$\overline{R}$, $\overline{OE}$	1.65–1.95	2.3–2.7			0.35 x V_{CCB}	V
V_{OHA}	HIGH Level Output Voltage		1.65–1.95	2.3–2.7	$I_{OH} = -100\mu A$	$V_{CCA} - 0.2$		V
			1.65	2.3–2.7	$I_{OH} = -18mA$	1.7		
V_{OHB}	HIGH Level Output Voltage		1.65–1.95	2.3–2.7	$I_{OH} = -100\mu A$	$V_{CCB} - 0.2$		V
			1.65–1.95	2.3	$I_{OH} = -6mA$	1.25		
V_{OLA}	Low Level Output Voltage		1.65–1.95	2.3–2.7	$I_{OL} = 100\mu A$		0.2	V
			1.65	2.3–2.7	$I_{OL} = 18mA$		0.6	
V_{OLB}	Low Level Output Voltage		1.65–1.95	2.3–2.7	$I_{OL} = 100\mu A$		0.2	V
			1.65–1.95	2.3	$I_{OL} = 6mA$		0.3	
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		1.65–1.95	2.3–2.7	$0V \le V_I \le 3.6V$		±5.0	µA
I_{OZ}	3-STATE Output Leakage		1.65–1.95	2.3–2.7	$0V \le V_O \le 3.6V$, $\overline{OE} = V_{CCB}$', $V_I = V_{IH}$ or V_{IL}		±10	µA
I_{OFF}	Power Off Leakage Current		0	0	$0 \le (V_I, V_O) \le 3.6V$		10	µA
I_{CCA}/I_{CCB}	Quiescent Supply Current, per supply, V_{CCA} / V_{CCB}		1.65–1.95	2.3–2.7	$A_n = V_{CCA}$ or GND, B_n, $\overline{OE}$, & T/$\overline{R}$ = V_{CCB} or GND		20	µA
			1.65–1.95	2.3–2.7	$V_{CCA} \le An \le 3.6V$, $V_{CCB} \le B_n$, $\overline{OE}$, T/$\overline{R} \le 3.6V$		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input, B_n, T/$\overline{R}$, $\overline{OE}$		1.65–1.95	2.3–2.7	$V_I = V_{CCB} - 0.6V$		750	µA
	Increase in I_{CC} per Input, A_n		1.65–1.95	2.3–2.7	$V_I = V_{CCA} - 0.6V$		750	µA

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DC Electrical Characteristics ($1.65V < V_{CCB} \le 1.95V$, $3.0V < V_{CCA} \le 3.6V$)

Symbol	Parameter		V_{CCB} (V)	V_{CCA} (V)	Conditions	Min.	Max.	Units
V_{IHA}	HIGH Level Input Voltage	A_n	1.65–1.95	3.0–3.6		2.0		V
V_{IHB}		B_n, T/$\overline{R}$, $\overline{OE}$	1.65–1.95	3.0–3.6		0.65 x V_{CCB}		V
V_{ILA}	LOW Level Input Voltage	A_n	1.65–1.95	3.0–3.6			0.8	V
V_{ILB}		B_n, T/$\overline{R}$, $\overline{OE}$	1.65–1.95	3.0–3.6			0.35 x V_{CCB}	V
V_{OHA}	HIGH Level Output Voltage		1.65–1.95	3.0–3.6	$I_{OH} = -100\mu A$	$V_{CCA} - 0.2$		V
			1.65	3.0–3.6	$I_{OH} = -24mA$	2.2		
V_{OHB}	HIGH Level Output Voltage		1.65–1.95	3.0–3.6	$I_{OH} = -100\mu A$	$V_{CCA} - 0.2$		V
			1.65–1.95	3.0	$I_{OH} = -6mA$	1.25		
V_{OLA}	LOW Level Output Voltage		1.65–1.95	3.0–3.6	$I_{OL} = 100\mu A$		0.2	V
			1.65	3.0–3.6	$I_{OL} = 24mA$		0.55	
V_{OLB}	LOW Level Output Voltage		1.65–1.95	3.0–3.6	$I_{OL} = 100\mu A$		0.2	V
			1.65–1.95	3.0	$I_{OL} = 6mA$		0.3	
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		1.65–1.95	3.0–3.6	$0V \le V_I \le 3.6V$		±5.0	µA
I_{OZ}	3-STATE Output Leakage		1.65–1.95	3.0–3.6	$0V \le V_O \le 3.6V$, $\overline{OE} = V_{CCB}$, $V_I = V_{IH}$ or V_{IL}		±10	µA
I_{OFF}	Power OFF Leakage Current		0	0	$0 \le (V_I, V_O) \le 3.6V$		10	µA
I_{CCA}/I_{CCB}	Quiescent Supply Current, per supply, V_{CCA}/V_{CCB}		1.65–1.95	3.0–3.6	$A_n = V_{CCA}$ or GND, B_n, $\overline{OE}$, & T/$\overline{R}$ = V_{CCB} or GND		20	µA
			1.65–1.95	3.0–3.6	$V_{CCA} \le A_n \le 3.6V$, $V_{CCB} \le B_n$, $\overline{OE}$, T/$\overline{R} \le 3.6V$		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input, B_n, T/$\overline{R}$, $\overline{OE}$,		1.65–1.95	3.0–3.6	$V_I = V_{CCB} - 0.6V$		750	µA
	Increase in I_{CC} per Input, A_n		1.65–1.95	3.0–3.6	$V_I = V_{CCA} - 0.6V$		750	µA

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DC Electrical Characteristics ($2.3V < V_{CCB} \le 2.7V$, $3.0V \le V_{CCA} \le 3.6V$)

Symbol	Parameter		V_{CCB} (V)	V_{CCA} (V)	Conditions	Min.	Max.	Units
V_{IHA}	HIGH Level Input Voltage	A_n	2.3–2.7	3.0–3.6		2.0		V
V_{IHB}		B_n, T/$\overline{R}$, $\overline{OE}$	2.3–2.7	3.0–3.6		1.6		V
V_{ILA}	LOW Level Input Voltage	A_n	2.3–2.7	3.0–3.6			0.8	V
V_{ILB}		B_n, T/$\overline{R}$, $\overline{OE}$	2.3–2.7	3.0–3.6			0.7	V
V_{OHA}	HIGH Level Output Voltage		2.3–2.7	3.0–3.6	$I_{OH} = -100\mu A$	$V_{CCA} - 0.2$		V
			2.3	3.0–3.6	$I_{OH} = -24mA$	2.2		
V_{OHB}	HIGH Level Output Voltage		2.3–2.7	3.0–3.6	$I_{OH} = -100\mu A$	$V_{CCB} - 0.2$		V
			2.3–2.7	3.0	$I_{OH} = -18mA$	1.7		
V_{OLA}	LOW Level Output Voltage		2.3–2.7	3.0–3.6	$I_{OL} = 100\mu A$		0.2	V
			2.3	3.0–3.6	$I_{OL} = 24mA$		0.55	
V_{OLB}	LOW Level Output Voltage		2.3–2.7	3.0–3.6	$I_{OL} = 100\mu A$		0.2	V
			2.3–2.7	3.0	$I_{OL} = 18mA$		0.6	
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		2.3–2.7	3.0–3.6	$0V \le V_I \le 3.6V$		±5.0	µA
I_{OZ}	3-STATE Output Leakage @ A_n		2.3–2.7	3.0–3.6	$0V \le V_O \le 3.6V$, $\overline{OE} = V_{CCA}$, $V_I = V_{IH}$ or V_{IL}		±10	µA
I_{OFF}	Power OFF Leakage Current		0	0	$0 \le (V_I, V_O) \le 3.6V$		10	µA
I_{CCA}/I_{CCB}	Quiescent Supply Current, per supply, V_{CCA}/V_{CCB}		2.3–2.7	3.0–3.6	$A_n = V_{CCA}$ or GND, B_n, $\overline{OE}$, & T/$\overline{R}$ = V_{CCB} or GND		20	µA
			2.3–2.7	3.0–3.6	$V_{CCA} \le A_n \le 3.6V$, $V_{CCB} \le B_n$, $\overline{OE}$, T/$\overline{R} \le 3.6V$		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input, B_n, T/$\overline{R}$, $\overline{OE}$		2.3–2.7	3.0–3.6	$V_I = V_{CCB} - 0.6V$		750	µA
	Increase in I_{CC} per Input, A_n		2.3–2.7	3.0–3.6	$V_I = V_{CCA} - 0.6V$		750	µA

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AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 30$ pF, $R_L = 500\Omega$						Units
		V_{CCB} = 1.65V to 1.95V, V_{CCA} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V, V_{CCA} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V, V_{CCA} = 3.0V to 3.6V		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay, A to B	1.5	5.8	1.5	6.2	0.8	4.4	ns
t_{PHL}, t_{PLH}	Propagation Delay, B to A	0.8	5.5	0.6	5.1	0.6	4.0	ns
t_{PZL}, t_{PZH}	Output Enable Time, OE to B	1.5	8.3	1.5	8.2	0.8	4.6	ns
t_{PZL}, t_{PZH}	Output Enable Time, OE to A	0.8	5.3	0.6	5.1	0.6	4.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to B	0.8	4.6	0.8	4.5	0.8	4.4	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to A	0.8	5.2	0.6	5.6	0.6	4.8	ns
t_{osHL}, t_{osLH}	Output to Output Skew(7)		0.05		0.5		0.75	ns

Note:

7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{osHL}) or LOW-to-HIGH (t_{osLH}).

Dynamic Switching Characteristics

Symbol	Parameter	V_{CCB} (V)	V_{CCA} (V)	Conditions	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}, A to B	1.8	2.5	C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0V	0.25	V
		1.8	3.3		0.25	
		2.5	3.3		0.6	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}, B to A	1.8	2.5	C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0V	0.6	V
		1.8	3.3		0.8	
		2.5	3.3		0.8	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}, A to B	1.8	2.5	C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0V	–0.25	V
		1.8	3.3		–0.25	
		2.5	3.3		–0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}, B to A	1.8	2.5	C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0V	–0.6	V
		1.8	3.3		–0.8	
		2.5	3.3		–0.8	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}, A to B	1.8	2.5	C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0V	1.3	V
		1.8	3.3		1.3	
		2.5	3.3		1.7	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}, B to A	1.8	2.5	C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0V	1.7	V
		1.8	3.3		2.0	
		2.5	3.3		2.0	

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Capacitance

Symbol	Parameter	Conditions	T_A = +25°C	Units
C_{IN}	Input Capacitance	V_{CCB} = 2.5V, V_{CCA} = 3.3V, V_I = 0V or $V_{CCA/B}$	5	pF
$C_{I/O}$	Input/Output Capacitance	V_{CCB} = 2.5V, V_{CCA} = 3.3V, V_I = 0V or $V_{CCA/B}$	6	pF
C_{PD}	Power Dissipation Capacitance	V_{CCB} = 2.5V, V_{CCA} = 3.3V, V_I = 0V or $V_{CCA/B}$, f = 10MHz	20	pF

AC Loading and Waveforms

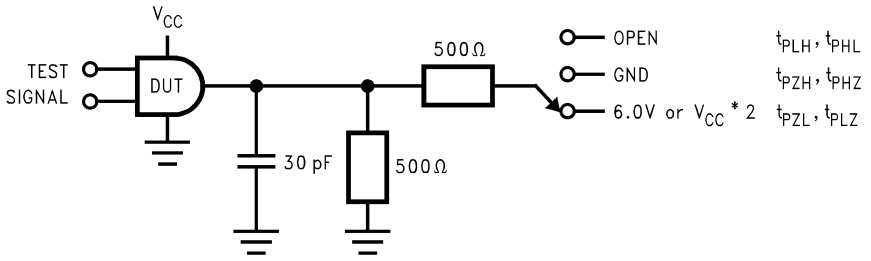


Figure 1. AC Test Circuit

Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ±0.3V; V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

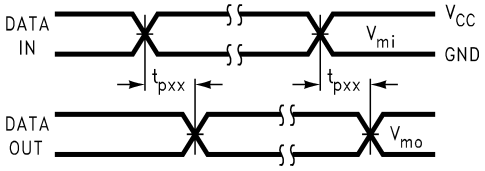


Figure 2. Waveform for Inverting and Non-inverting Functions
t_R = t_F ≤ 2.0 ns, 10% to 90%

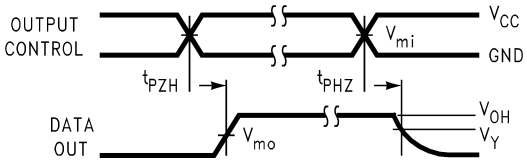


Figure 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic
t_R = t_F ≤ 2.0 ns, 10% to 90%

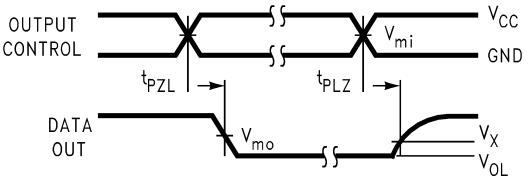


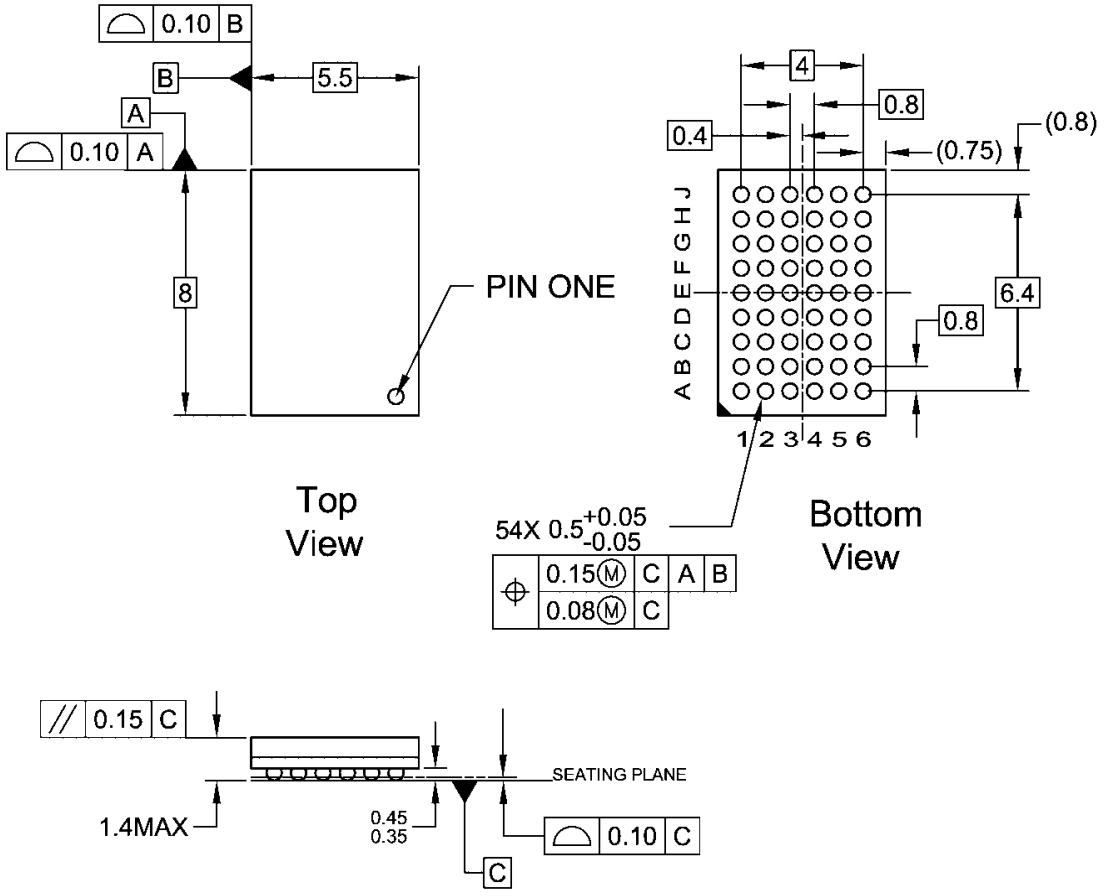
Figure 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic
t_R = t_F ≤ 2.0 ns, 10% to 90%

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	V_{CC} / 2	V_{CC} / 2
V_{mo}	1.5V	V_{CC} / 2	V_{CC} / 2
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} – 0.3V	V_{OH} – 0.15V	V_{OH} – 0.15V

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Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205

B. ALL DIMENSIONS IN MILLIMETERS

C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS

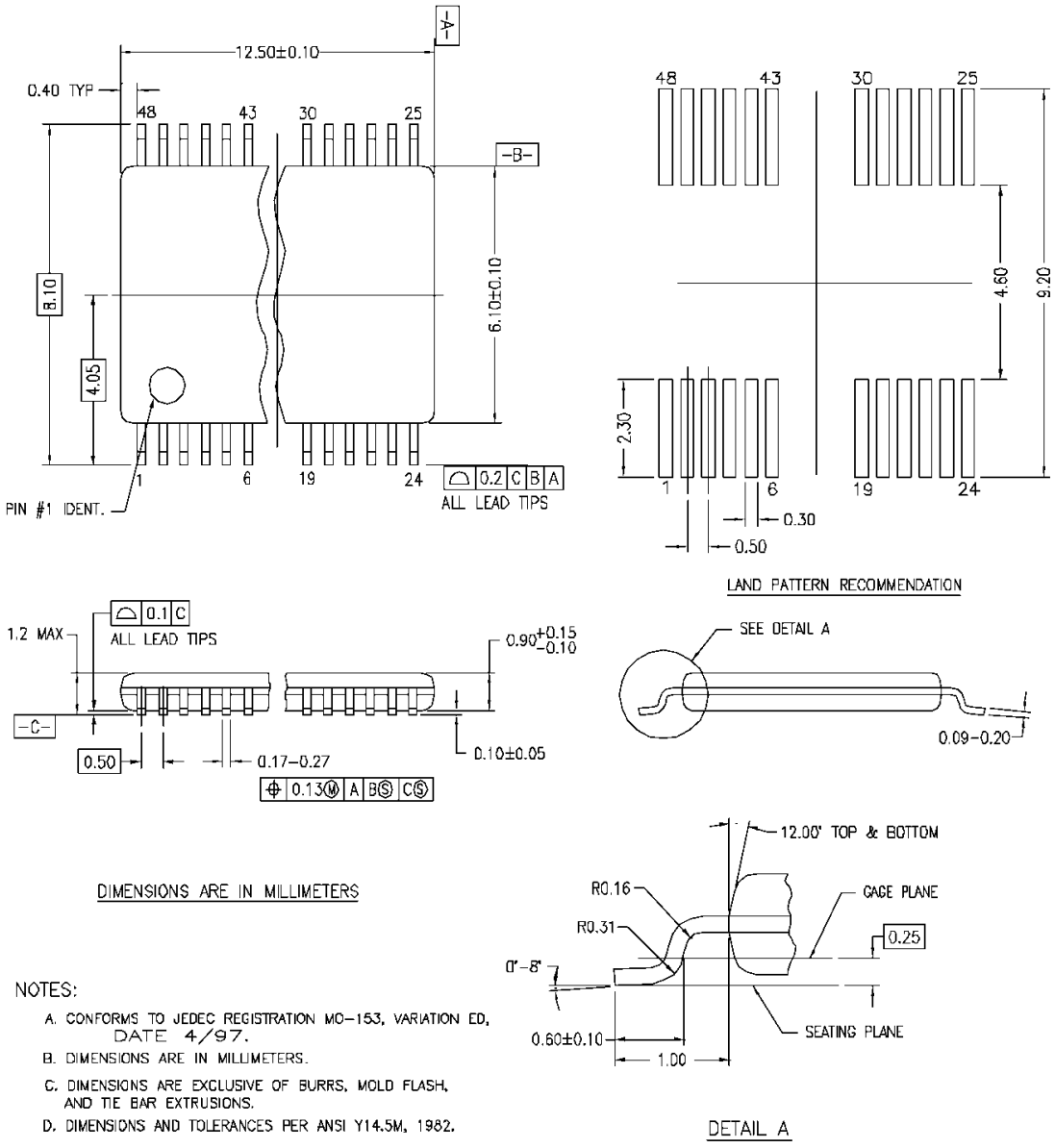
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

Figure 5. 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–153, VARIATION ED, DATE 4/97.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

Figure 6. 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I26

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