Desktop/Notebook Frequency Generator

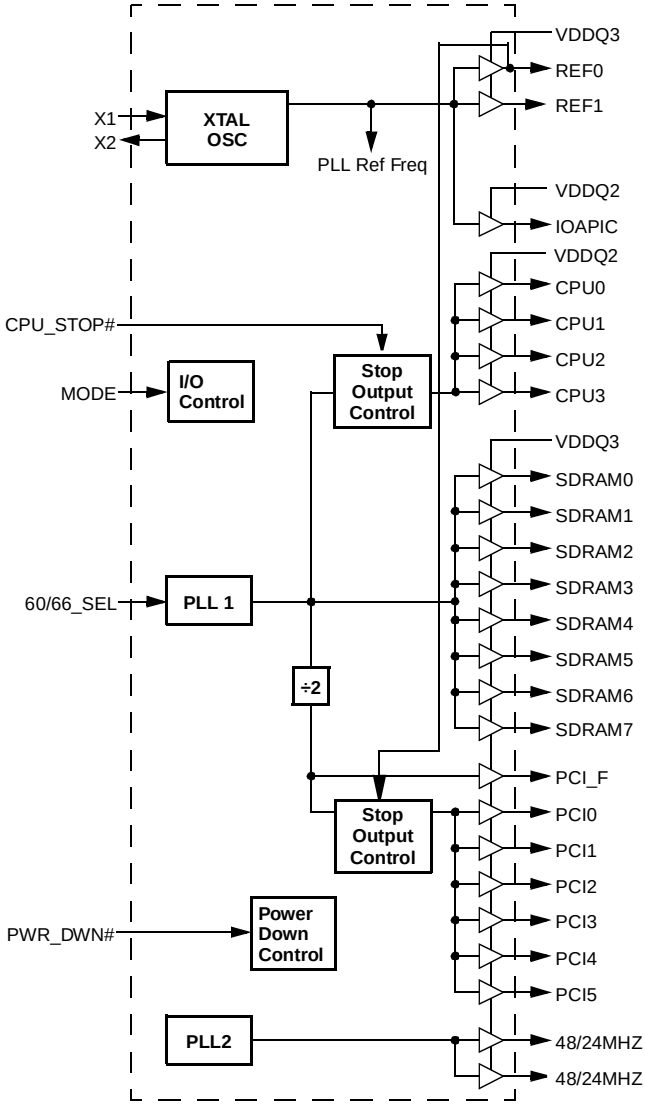
Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **±0.5% Spread Spectrum clocking**
- **Equivalent to the W48S67-72 with Spread Spectrum for Tilamook, MMO, and Deschutes processors**
- **Generates system clocks for CPU, IOAPIC, SDRAM, PCI, USB plus 14.318-MHz (REF0:1)**
- **Serial data interface (SDATA, SCLOCK inputs) provides additional CPU/PCI clock frequency selections, individual output clock disabling and other functions**
- **MODE input pin selects optional power management input control pins (reconfigures pins 26 and 27)**
- **Two fixed outputs separately selectable as 24-MHz or 48-MHz (default = 48-MHz)**
- **V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5%**
- **Uses external 14.318-MHz crystal**
- **Available in 48-pin SSOP (300 mils)**
- **10Ω CPU output impedance**

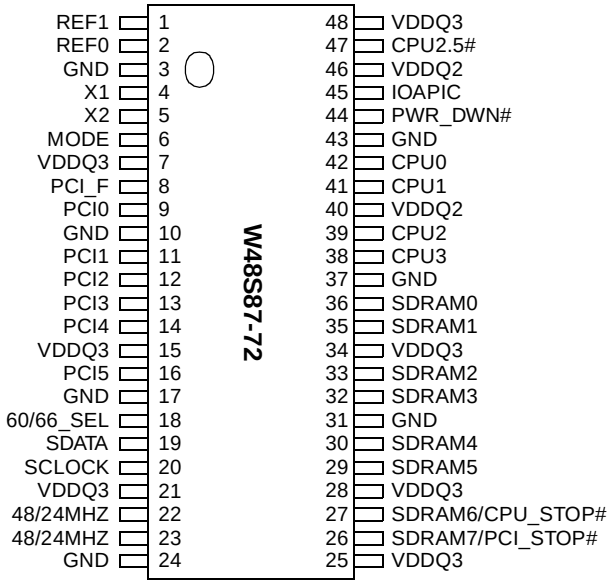
Table 1. Pin Selectable Frequency[1]

60/66_SEL	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)
0	60	30
1	66.8	33.4

Block Diagram



Pin Configuration



Note:

1. Additional frequency selections provided by serial data interface; refer to *Table 5* on page 8.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	42, 41, 39, 38	O	***CPU Outputs 0 through 3:*** These four CPU outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI0:5	9, 11, 12, 13, 14, 16	O	***PCI Bus Outputs 0 through 5:*** These six PCI outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI_F	8	O	***Free Running PCI Output:*** Unlike PCI0:5 outputs, this output is not controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
SDRAM0:5	36, 35, 33, 32, 30, 29	O	***SDRAM Clock Outputs 0 through 5:*** These six SDRAM clock outputs run synchronous to the CPU clock outputs. Output voltage swing is controlled by voltage applied to VDDQ3.
SDRAM6/ CPU_STOP#	27	I/O	***SDRAM Clock Output 6 or CPU Clock Output Stop Control:*** This pin has dual functions, selectable by the MODE input pin. When MODE = 0, this pin becomes the CPU_STOP# input. When MODE = 1, this pin becomes SDRAM clock output 6. Regarding use as a CPU_STOP# input: When brought LOW, clock outputs CPU0:3 are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, clock outputs CPU0:3 are started beginning with a full clock cycle (2–3 CPU clock latency). Regarding use as a SDRAM clock: Output voltage swing is controlled by voltage applied to VDDQ3.
SDRAM7/ PCI_STOP#	26	I/O	***SDRAM Clock Output 7 or PCI Clock Output Stop Control:*** This pin has dual functions, selectable by the MODE input pin. When MODE = 0, this pin becomes the PCI_STOP# input. When MODE = 1, this pin becomes SDRAM clock output 7. PCI_STOP# input: When brought LOW, clock outputs PCI0:5 are stopped LOW after completing a full clock cycle. When brought HIGH, clock outputs PCI0:5 are started beginning with a full clock cycle. Clock latency provides one PCI_F rising edge of PCI clock following PCI_STOP# state change. Regarding use as a SDRAM clock: Output voltage swing is controlled by voltage applied to VDDQ3.
IOAPIC	45	O	***I/O APIC Clock Output:*** Provides 14.318-MHz fixed frequency. The output voltage swing is controlled by VDDQ2.
48/24MHz	22, 23	O	***48-MHz / 24-MHz Output:*** Fixed clock outputs that default to 48 MHz following device power-up. Either or both can be changed to 24 MHz through use of the serial data interface (Byte 0, bits 2 and 3). Output voltage swing is controlled by voltage applied to VDDQ3
REF0:1	2, 1	O	***Fixed 14.318-MHz Outputs 0 through 1:*** Used for various system applications. Output voltage swing is controlled by voltage applied to VDDQ3. REF0 is stronger than REF1 and should be used for driving ISA slots.
CPU_2.5#	47	I	Set to logic 0 for V_{DDQ2} = 2.5V (0 to 2.5V CPU output swing).
60/66_SEL	18	I	***60- or 66-MHz Input Selection:*** Selects power-up default CPU clock frequency as shown in *Table 1* on page 1 (also determines SDRAM and PCI clock frequency selections). Can be used to change CPU clock frequency while device is in operation if serial data port bits 0–2 of Byte 7 are logic 1 (default power-up condition).
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.

Pin Definitions (continued)

Pin Name	Pin No.	Pin Type	Pin Description
PWR_DWN#	44	I	***Power-Down Control:*** When this input is LOW, the device goes into a low-power standby condition. All outputs are actively held LOW while in power-down. CPU, SDRAM, and PCI clock outputs are stopped LOW after completing a full clock cycle (2–4 CPU clock cycle latency). When brought HIGH, CPU, SDRAM, and PCI outputs start with a full clock cycle at full operating frequency (3 ms maximum latency).
MODE	6	I	***Mode Control:*** This input selects the function of device pin 26 (SDRAM7/PCI_STOP#) and pin 27 (SDRAM6/CPU_STOP#). Refer to description for those pins.
SDATA	19	I/O	***Serial Data Input:*** Data input for Serial Data Interface. Refer to Serial Data Interface section that follows.
SCLOCK	20	I	***Serial Clock Input:*** Clock input for Serial Data Interface. Refer to Serial Data Interface section that follows.
VDDQ3	7, 15, 21, 25 28, 34, 48	P	***Power Connection:*** Power supply for PCI0:5, REF0:1, and 48/24MHz output buffers. Connected to 3.3V supply.
VDDQ2	46, 40	P	***Power Connection:*** Power supply for IOAPIC0, CPU0:3 output buffer. Connected to 2.5V supply.
GND	3, 10, 17, 24, 31, 37, 43	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Spread Spectrum Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As depicted in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is ±0.5% of the center frequency. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1–0 in data byte 0 of the I^2C data stream. Refer to *Table 4* for more details.

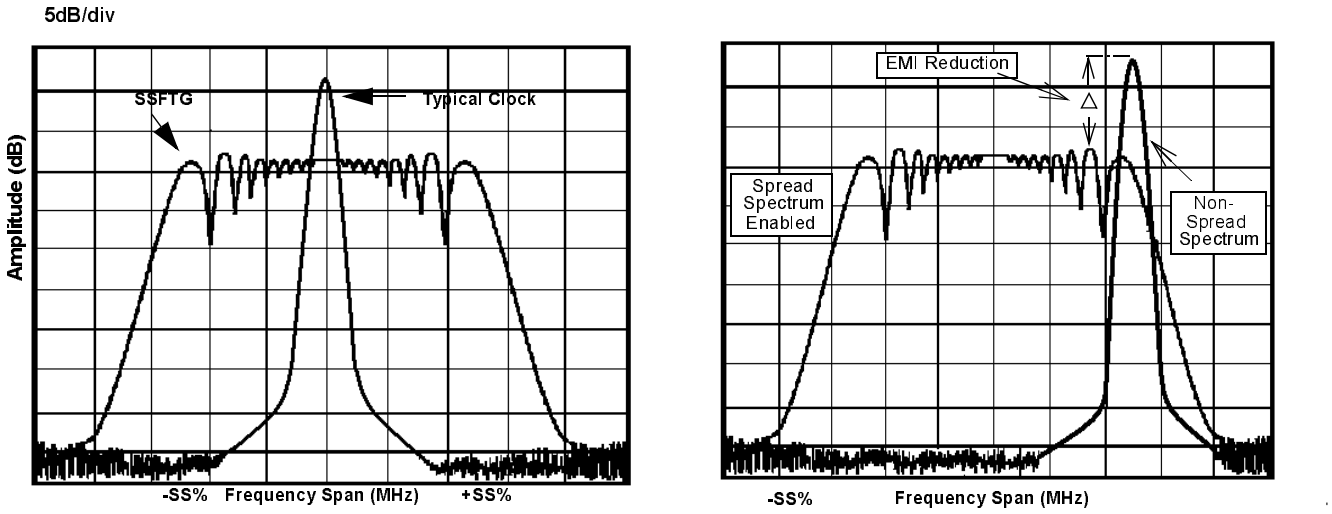


Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

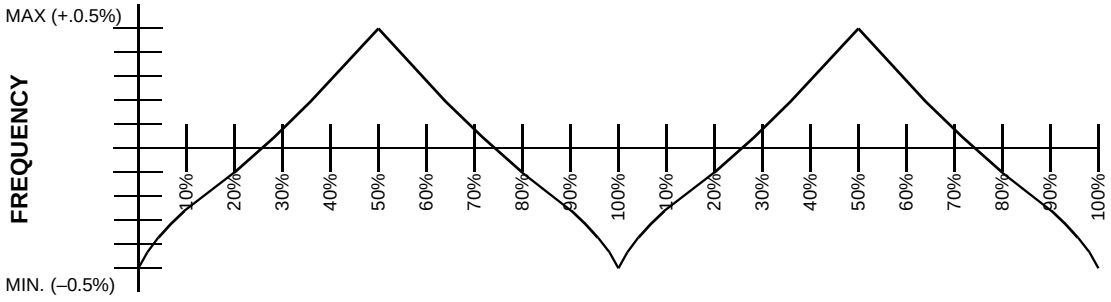


Figure 2. Typical Modulation Profile

Serial Data Interface

The W48S87-72 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W48S87-72 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 2* summarizes the control functions of the serial data interface.

Operation

Data is written to the W48S87-72 in ten bytes of eight bits each. Bytes are written in the order shown in *Table 3*.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused SDRAM DIMM socket or PCI slot.
48-/24-MHz Clock Output Frequency Selection	48-/24-MHz clock outputs can be set to 48 MHz or 24 MHz.	Provides flexibility in Super I/O and USB device selection.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 60- and 66.6-MHz selections that are provided by the SEL60/66 input pin. Frequency is changed in a smooth and controlled fashion.	For alternate CPU devices, and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Three-state	Puts all clock outputs into a high-impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation with X1 input, internal PLL is bypassed. Refer to *Table 4*.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W48S87-72 to accept the bits in Data Bytes 0–7 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W48S87-72 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W48S87-72, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W48S87-72, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to *Table 4*	The data bits in Data Bytes 0–7 set internal W48S87-72 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 4*, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		
11	Data Byte 7		

Writing Data Bytes

Each bit in the data bytes control a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 4* gives the bit formats for registers located in Data Bytes 0–7.

Table 5 details additional frequency selections that are available through the serial data interface.

Table 6 details the select functions for Byte 0, bits 1 and 0.

Table 4. Data Bytes 0–7 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	Refer to *Table 5*		0
5	--	--	SEL_4	Refer to *Table 5*		0
4	--	--	SEL_3	Refer to *Table 5*		0
3	23	48/24MHZ	48-/24-MHz Clock Output Frequency Selection	24 MHz	48 MHz	0
2	22	48/24MHZ	48-/24-MHz Clock Output Frequency Selection	24 MHz	48 MHz	0
1–0	--	--	Bit 1 Bit 0 Function (See *Table 6* for function details) 0 0 Normal Operation 0 1 Test Mode 1 0 Spread Spectrum On 1 1 All Outputs Three-stated			00
Data Byte 1						
7	23	48/24MHZ	Clock Output Disable	Low	Active	1
6	22	48/24MHZ	Clock Output Disable	Low	Active	1
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	38	CPU3	Clock Output Disable	Low	Active	1
2	39	CPU2	Clock Output Disable	Low	Active	1
1	41	CPU1	Clock Output Disable	Low	Active	1
0	42	CPU0	Clock Output Disable	Low	Active	1
Data Byte 2						
7	--	--	(Reserved)	--	--	0
6	8	PCI_F	Clock Output Disable	Low	Active	1
5	16	PCI5	Clock Output Disable	Low	Active	1
4	14	PCI4	Clock Output Disable	Low	Active	1
3	13	PCI3	Clock Output Disable	Low	Active	1
2	12	PCI2	Clock Output Disable	Low	Active	1
1	11	PCI1	Clock Output Disable	Low	Active	1
0	9	PCI0	Clock Output Disable	Low	Active	1
Data Byte 3						
7	26	SDRAM7	Clock Output Disable	Low	Active	1
6	27	SDRAM6	Clock Output Disable	Low	Active	1
5	29	SDRAM5	Clock Output Disable	Low	Active	1
4	30	SDRAM4	Clock Output Disable	Low	Active	1
3	32	SDRAM3	Clock Output Disable	Low	Active	1
2	33	SDRAM2	Clock Output Disable	Low	Active	1
1	35	SDRAM1	Clock Output Disable	Low	Active	1
0	36	SDRAM0	Clock Output Disable	Low	Active	1

Table 4. Data Bytes 0–7 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0
Data Byte 5						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	45	IOAPIC	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	1	REF1	Clock Output Disable	Low	Active	1
0	2	REF0	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0
Data Byte 7						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	SEL_2	Refer to *Table 5*		1
1	--	--	SEL_1	Refer to *Table 5*		1
0	--	--	SEL_0	Refer to *Table 5*		1

Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes

Date Byte 0			Date Byte 7					
Bit 5 SEL_4	Bit 4 SEL_3	60/66_SEL (Pin 18)	Bit 2 SEL_2	BIT 1 SEL_1	BIT 0 SEL_0	CPU0:3 SDRAM0:7	PCI_F PCI0:5	Spread Spectrum%
0	0	X	0	0	0	75.0	CPU/2	±0.5
0	0	X	0	0	1	75.0	32	±0.5
0	0	X	0	1	0	83.31	32	±0.5
0	0	X	0	1	1	33.41	CPU/2	±0.5
0	0	X	1	0	0	50.11	CPU/2	±0.5
0	0	X	1	0	1	68.52	CPU/2	±0.5
0	0	X	1	1	0	60.0	CPU/2	±0.5
0	0	0	1	1	1	60.0	CPU/2	±0.5
0	0	1	1	1	1	66.82	CPU/2	±0.5
0	1	0	X	X	X	60.0	CPU/2	±0.5
0	1	1	X	X	X	66.6	CPU/2	–0.5
1	0	0	X	X	X	60.0	CPU/2	±0.5
1	0	1	X	X	X	66.6	CPU/2	–0.5
1	1	0	X	X	X	60.0	CPU/2	±0.5
1	1	1	X	X	X	66.6	CPU/2	–0.5

Table 6. Select Function for Data Byte 0, Bits 0:1

	Input Conditions		Output Conditions			
	Data Byte 0					
Function	Bit 1	Bit 0	CPU0:3, SRAM0:7	PCI_F, PCI0:5	REF0:2, IOAPIC	48/24MHZ
Normal Operation	0	0	Note 2	Note 2	14.318 MHz	48 or 24 MHz
Test Mode	0	1	X1/2	X1/4	X1	Note 3
Spread Spectrum On	1	0	Note 2	Note 2	14.318 MHz	48 or 24 MHz
Three-state	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes:

2. CPU, SDRAM, and PCI frequency selections are listed in *Table 1* and *Table 5*.
3. In Test Mode, the 48-/24-MHz clock outputs are:
   - X1/2 if 48-MHz is selected.
   - X1/4 if 24-MHz is selected.

How To Use the Serial Data Interface

Electrical Requirements

Figure 3 illustrates electrical characteristics for the serial interface bus used with the W48S87-72. Devices send data over the bus with an open drain logic output that can (a) pull the bus line LOW, or (b) let the bus default to logic 1. The pull-up resistors on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W48S87-72 is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

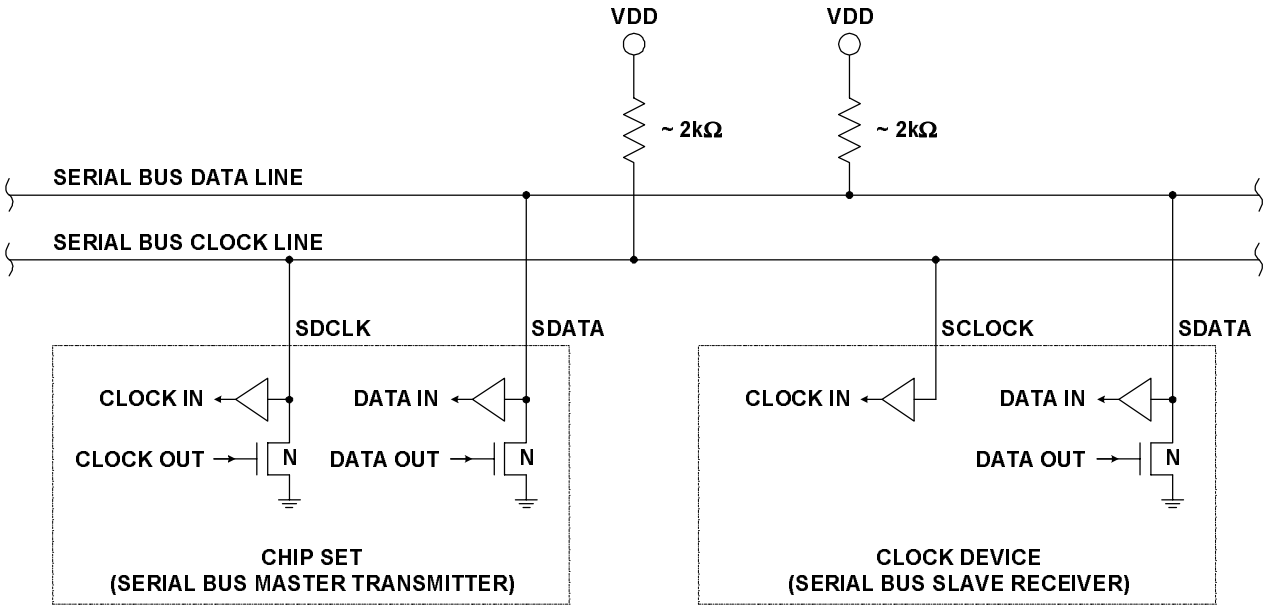


Figure 3. Serial Interface Bus Electrical Characteristics

Signaling Requirements

As shown in *Figure 4*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock HIGH pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “start bit” as shown in *Figure 5*. A “stop bit” signifies that a transmission has ended.

As stated previously, the W48S87-72 sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 6*.

Sending Data to the W48S87-72

The device accepts data once it has detected a valid start bit and address byte sequence. Device functionality is changed upon the receipt of each data bit (registers are not double buffered). Partial transmission is allowed meaning that a transmission can be truncated as soon as the desired data bits are transmitted (remaining registers will be unmodified). Transmission is truncated with either a stop bit or new start bit (restart condition).

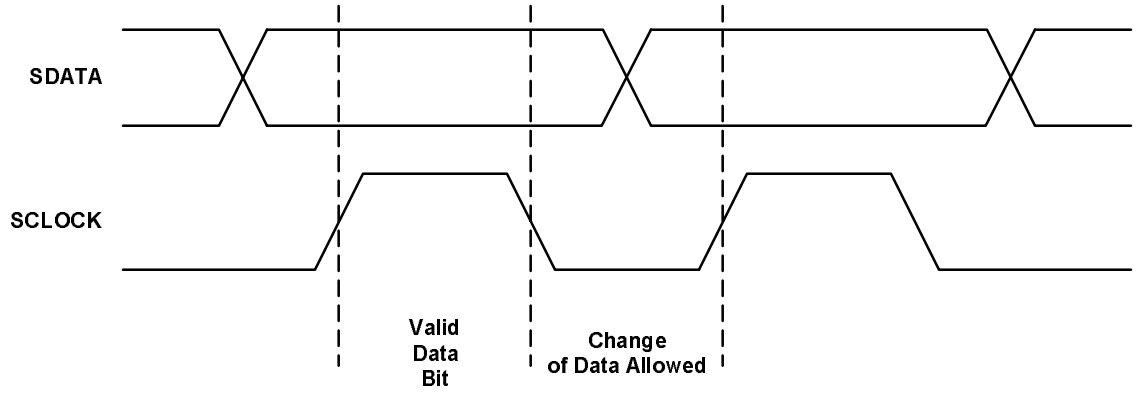


Figure 4. Serial Data Bus Valid Data Bit

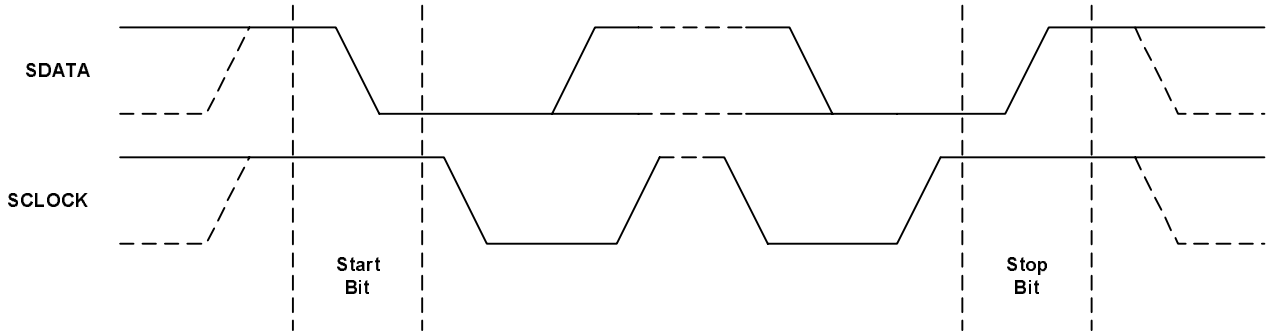


Figure 5. Serial Data Bus Start and Stop Bit

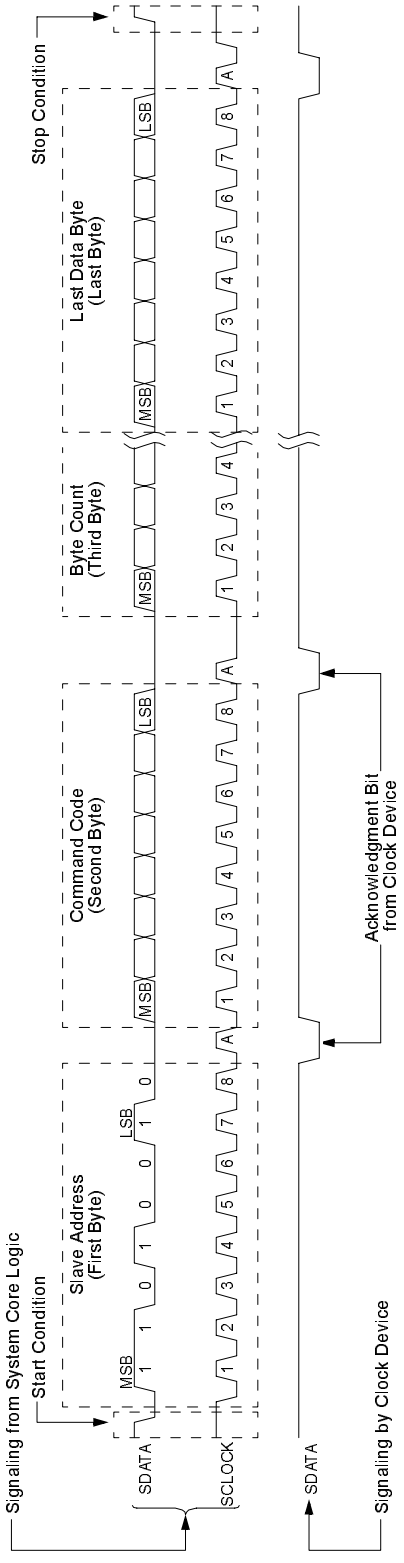


Figure 6. Serial Data Bus Write Sequence

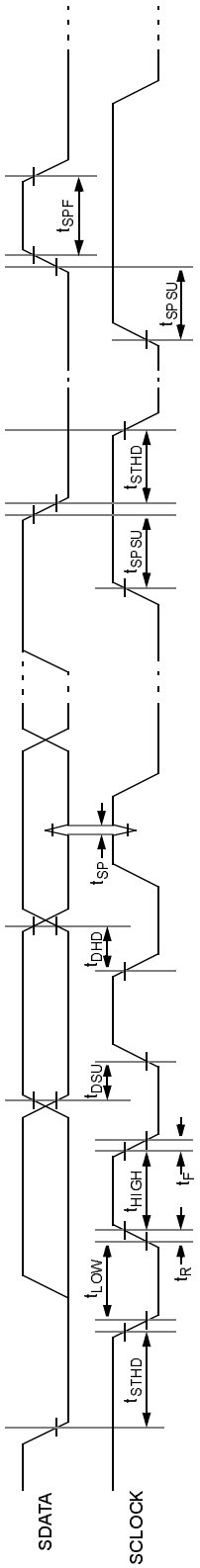


Figure 7. Serial Data Bus Timing Diagram

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics:

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5% (3.135–3.465V) f_{XTL} = 14.31818 MHz, V_{DDQ2} = 2.5±5%

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DDQ3}	Supply Current (3.3V)		CPUCLK =66.8 MHz Outputs Loaded[4]	120	150	200	mA
I_{DDQ2}	Supply Current (2.5V)		CPUCLK =66.8 MHz Outputs Loaded[4]			50	mA
Logic Inputs							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current[5]					10	µA
I_{IH}	Input High Current[5]					10	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
V_{OH}	Output High Voltage (CPU, IOAPIC)		I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current	CPU0:3	V_{OL} = 1.25V		155		mA
		SDRAM0:7	V_{OL} = 1.5V		100		mA
		PCI_F, PCI0:5	V_{OL} = 1.5V		95		mA
		IOAPIC	V_{OL} = 1.25V		85		mA
		REF0	V_{OL} = 1.5V		75		mA
		REF1	V_{OL} = 1.5V		60		mA
		48/24MHZ	V_{OL} = 1.5V		60		mA
I_{OH}	Output High Current	CPU0:3	V_{OL} = 1.25V		125		mA
		SDRAM0:7	V_{OL} = 1.5V		95		mA
		PCI_F, PCI0:5	V_{OL} = 1.5V		100		mA
		IOAPIC	V_{OL} = 1.25V		80		mA
		REF0	V_{OL} = 1.5V		80		mA
		REF1	V_{OL} = 1.5V		65		mA
		48/24MHZ	V_{OL} = 1.5V		60		mA

Notes:

4. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
5. W48S87-72 logic inputs have internal pull-up devices. (Not CMOS level.)

DC Electrical Characteristics: (continued)

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5% (3.135–3.465V) f_{XTL} = 14.31818 MHz, V_{DDQ2} = 2.5±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[6]	V_{DD} = 3.3V		1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[7]			14		pF
$C_{IN,X1}$	X1 Input Capacitance[8]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH
Serial Input Port						
V_{IL}	Input Low Voltage	V_{DD} = 3.3V		0.4	$0.3V_{DD}$	V
V_{IH}	Input High Voltage	V_{DD} = 3.3V	$0.7V_{DD}$	2.4		V
I_{IL}	Input Low Current	No internal pull-up/down on SCLOCK		10	10	µA
I_{IH}	Input High Current	No internal pull-up/down on SCLOCK		10	10	µA
I_{OL}	Sink Current into SDATA or SCLOCK, Open Drain N-Channel Device On	$I_{OL} = 0.3V_{DD}$	5	10	15	mA
C_{IN}	Input Capacitance of SDATA and SCLOCK			5	10	pF
C_{SDATA}	Total Capacitance of SDATA Bus				400	pF
C_{SCLOCK}	Total Capacitance of SCLOCK Bus				400	pF

Notes:

6. X1 input threshold voltage (typical) is $V_{DDQ3}/2$.
7. The W48S87-72 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
8. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = V_{DDQ3} = 3.3V±5% (3.135–3.465V) f_{XTL} = 14.31818 MHz, V_{DDQ2} = 2.5±5%

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8 MHz			CPU = 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	15			16.7			ns
f	Frequency, Actual	Determined by PLL divider ratio		66.8			59.876		MHz
t_H	High Time	Duration of clock cycle above 2.4V	5.2			6			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5			5.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45	52	55	45	52	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			250			250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		10			10		Ω

SDRAM Clock Outputs, SDRAM0:7 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8 MHz			CPU = 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	15			16.7			ns
f	Frequency, Actual	Determined by PLL divider ratio		66.8			59.876		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	45	50	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V		100			100		ps
t_{SK}	CPU to SDRAM Clock Skew	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.			500			500	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		16			16		Ω

PCI Clock Outputs, PCI0:5 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8 MHz			CPU = 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	30			33.3			ns
f	Frequency, Actual	Determined by PLL divider ratio		33.4			29.938		MHz
t_H	High Time	Duration of clock cycle above 2.4V	12			13.3			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			13.3			ns
t_R	Output Rise Edge Rate		1		4	1		4	V/ns
t_F	Output Fall Edge Rate		1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	51	55	45	51	55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250			250	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1		4	1		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30			30		Ω

I/O APIC Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 60/66.8 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate		1		4	V/ns
t_F	Output Fall Edge Rate		1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45	52.5	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

REF0 Clock Output (Lump Capacitance Test Load = 45 pF)

Parameter	Description	Test Condition/Comments	CPU = 60/66.8 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		16		Ω

REF1 Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 60/66.8 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.31818		MHz
t_R	Output Rise Edge Rate		0.5		2	V/ns
t_F	Output Fall Edge Rate		0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

48/24MHZ Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 60/66.8 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see n/m below)		48.008/24.004		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17		
t_R	Output Rise Edge Rate		0.5		2	V/ns
t_F	Output Fall Edge Rate		0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	50	55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

Serial Input Port

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{SCLOCK}	SCLOCK Frequency	Normal Mode	0		100	kHz
t_{STHD}	Start Hold Time		4.0			µs
t_{LOW}	SCLOCK Low Time		4.7			µs
t_{HIGH}	SCLOCK High Time		4.0			µs
t_{DSU}	Data Set-up Time		250			ns
t_{DHD}	Data Hold Time	(Transmitter should provide a 300-ns hold time to ensure proper timing at the receiver.)	0			ns
t_R	Rise Time, SDATA and SCLOCK	From $0.3V_{DD}$ to $0.7V_{DD}$			1000	ns
t_F	Fall Time, SDATA and SCLOCK	From $0.7V_{DD}$ to $0.3V_{DD}$			300	ns
t_{STSU}	Stop Set-up Time		4.0			µs
t_{SPF}	Bus Free Time between Stop and Start Condition		4.7			µs
t_{SP}	Allowable Noise Spike Pulse Width				50	ns

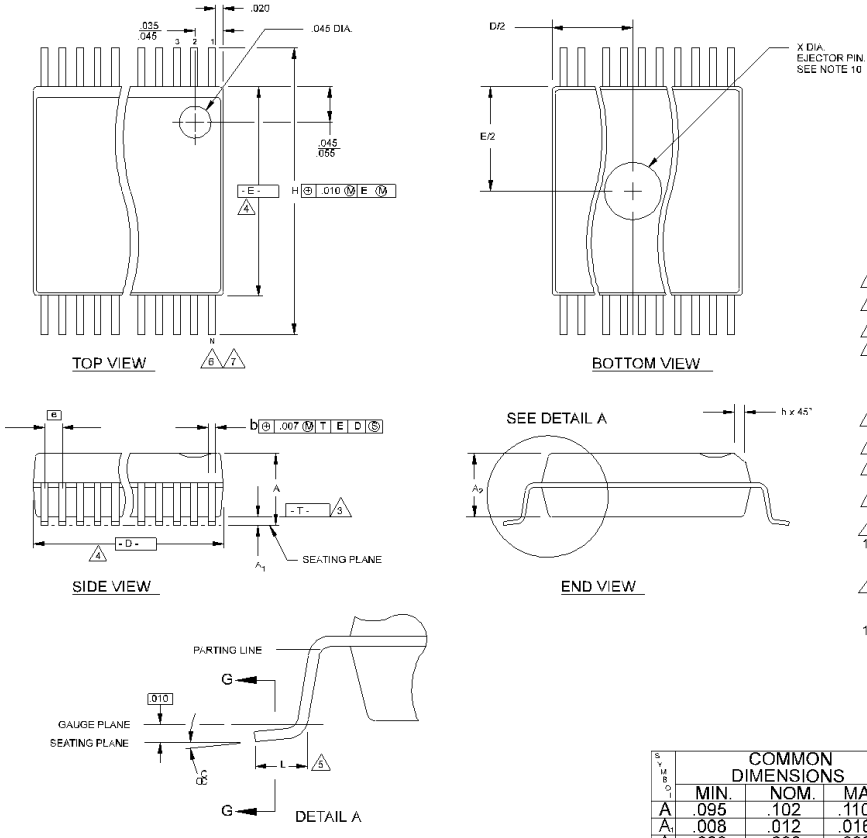
Ordering Information

Ordering Code	Freq. Mask Code	Package Name	Package Type
W48S87	72	H X	48-pin SSOP (300 mils) 48-pin TSSOP

Document #: 38-00855-*A

Package Diagrams

48-Pin Small Shrink Outline Package (SSOP, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
α	0°	5°	8°						

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

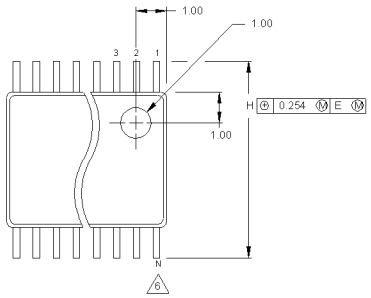
Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
α	0°	5°	8°						

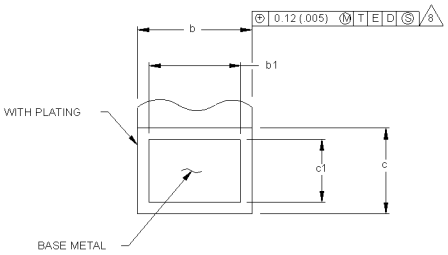
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Package Diagrams (continued)

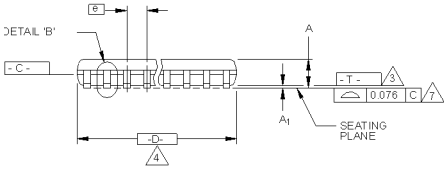
48-Pin Thin Shrink Small Outline Package (TSSOP)



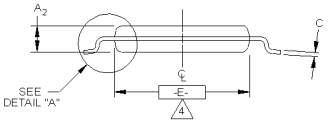
TOP VIEW



DETAIL "C"
SCALE: 120/1
(SEE NOTE 9)



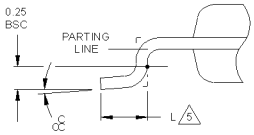
SIDE VIEW



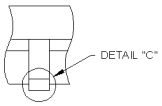
END VIEW

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (.0110±.0005 INCH
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
8. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm SEE DETAILS 'B' AND 'C'.
9. DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS.
11. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-15 VARIATIONS AA, AB, AC, AD AND AE.



DETAIL 'A'
(SCALE: 30/1)



DETAIL "B"
(SCALE: 30/1)
DAMBAR PROTRUSION

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	NOTE 4 VARIATIONS	D MIN.	D NOM.	D MAX.	S MIN.	S NOM.	S MAX.	6 N
A	——	——	1.10		AA	12.40	12.50	12.60	0.37	0.50	——	48
A_1	0.05	0.10	0.15		AB	13.90	14.00	14.10	0.12	0.25	——	56
A_2	0.85	0.90	0.95									
b	0.17	——	0.27	8								
b1	0.17	0.20	0.23									
C	0.090	——	0.200	8								
C1	0.090	0.127	0.160									
D	SEE VARIATIONS			4								
E	6.00	6.10	6.20	4								
e	0.50 BSC											
H	7.95	8.10	8.25									
L	0.50	0.60	0.75	5								
N	SEE VARIATIONS			6								
øC	0°	4°	8°									

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	NOTE 4 VARIATIONS	D MIN.	D NOM.	D MAX.	S MIN.	S NOM.	S MAX.	6 N
A	——	——	.0433		AA	.488	.492	.496	.0146	.0197	——	48
A_1	.002	.004	.006		AB	.547	.551	.555	.0047	.0098	——	56
A_2	.0335	.0354	.0374									
b	.0067	——	.011	8								
b1	.0067	.0078	.0090									
C	.0035	——	.0078	8								
C1	.0035	.0050	.0063									
D	SEE VARIATIONS			4								
E	.236	.240	.244	4								
e	.0197 BSC											
H	.313	.319	.325									
L	.020	.024	.030	5								
N	SEE VARIATIONS			6								
øC	0°	4°	8°									

PACKAGE OUTLINE, 6.10mm (.240") BODY, TSSOP, 0.50mm LEAD PITCH

SIZE	DWG. NO.	REV
A5	34389	02

SCALE 8/1 SHEET 2 OF 2

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