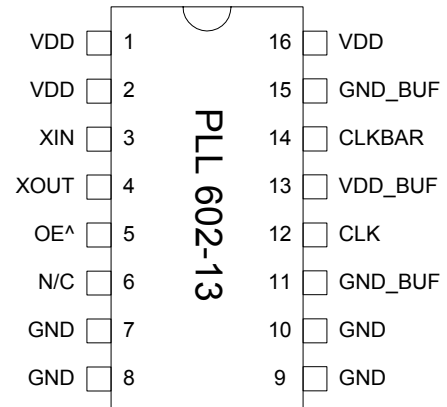


**192MHz – 400MHz Low Phase Noise PECL XO (12 – 25MHz Crystal)**

**FEATURES**

- Low phase noise output for the 192MHz to 400MHz range (-134 dBc at 10kHz offset).
- PECL output.
- 12 to 25MHz crystal input.
- Integrated crystal load capacitor: no external load capacitor required.
- Output Enable selector.
- 3.3V operation.
- Available in 16 Pin TSSOP.

**PIN CONFIGURATION**



Note: ^ denotes internal pull up

$$F_{OUT} = F_{XIN} \times 16$$

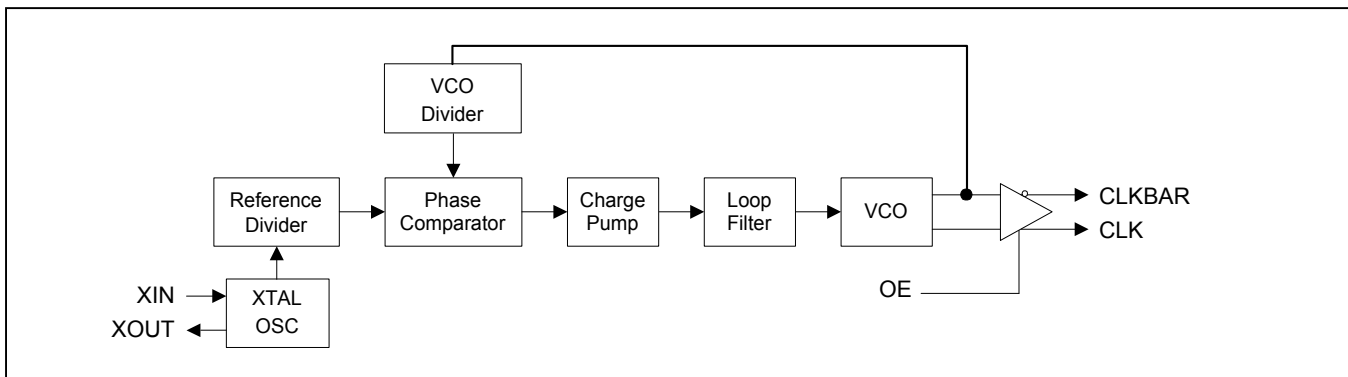
**DESCRIPTION**

The PLL602-13 is a monolithic low jitter and low phase noise (-134dBc/Hz @ 10kHz offset) XO IC with PECL output, for 192MHz to 400MHz output range. It provides a low phase noise reference frequency using a low cost crystal.

The chip delivers an output frequency of  $F_{XIN} \times 16$ . This makes the PLL602-13 ideal for a wide range of applications.

OE (Pin 5)	Output State
0	Tri-state
1 (Default)	Output enabled

**BLOCK DIAGRAM**



## 192MHz – 400MHz Low Phase Noise PECL XO (12 – 25MHz Crystal)

### PIN DESCRIPTIONS

Name	Number	Type	Description
VDD	1,2,16	P	Power supply.
XIN	3	I	Crystal input. See Crystal Specifications on page 2.
XOUT	4	I	Crystal output. See Crystal Specifications on page 2.
OE	5	I	Output enable input. Disables (tri-state) output when low. Internal pull-up enables output by default if pin is not connected to low.
N/C	6	-	Not connected.
GND	7,8,9,10	P	Ground.
GND_BUF	11,15	P	Ground for output buffers.
CLK	12	O	True clock output.
VDD_BUF	13	P	Power supply for output buffers.
CLKB	14	O	Complementary clock output.

### ELECTRICAL SPECIFICATIONS

#### 1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

#### 2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	$C_L$ (xtal)			20		pF
Recommended ESR	$R_E$	AT cut			30	$\Omega$

## 192MHz – 400MHz Low Phase Noise PECL XO (12 – 25MHz Crystal)

### 3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	I <sub>DD</sub>	PECL			80	mA
Operating Voltage	V <sub>DD</sub>		2.97		3.63	V
Output Clock Duty Cycle		@ V <sub>DD</sub> – 1.3V (PECL)	45	50	55	%
Short Circuit Current				±50		mA

### 4. Jitter and Phase Noise Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND.		5		ps
Accumulated jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles.		11		ps
Phase Noise relative to carrier	311MHz @100Hz offset		-90		dBc/Hz
Phase Noise relative to carrier	311MHz @1kHz offset		-115		dBc/Hz
Phase Noise relative to carrier	311MHz @10kHz offset		-125		dBc/Hz
Phase Noise relative to carrier	311MHz @100kHz offset		-119		dBc/Hz

**192MHz – 400MHz Low Phase Noise PECL XO (12 – 25MHz Crystal)**

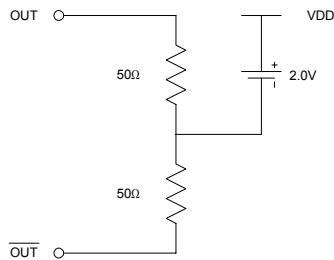
**5. PECL Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	$V_{OL}$			$V_{DD} - 1.620$	V

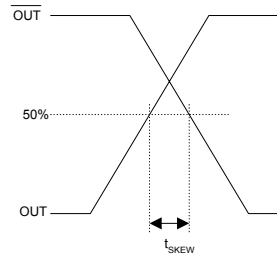
**6. PECL Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	$t_r$	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	$t_f$	@80/20% - PECL		0.5	1.5	ns

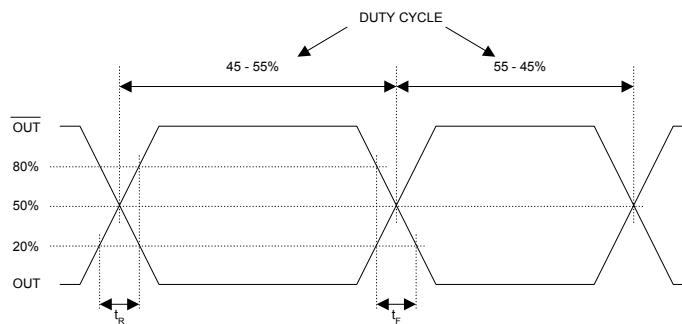
PECL Levels Test Circuit



PECL Output Skew



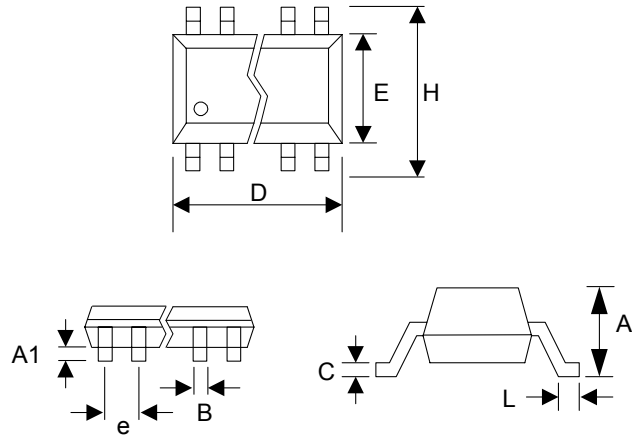
PECL Transition Time Waveform



**192MHz – 400MHz Low Phase Noise PECL XO (12 – 25MHz Crystal)**

**PACKAGE INFORMATION**

16 PIN TSSOP ( mm )		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



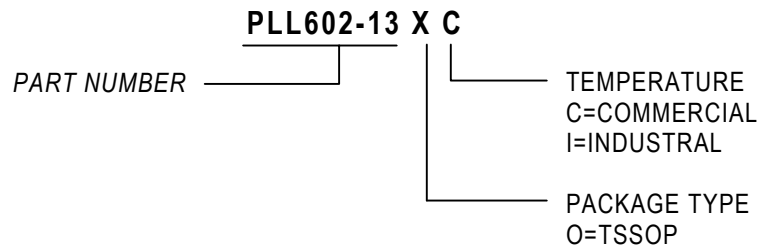
**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA  
Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range



<u>Order Number</u>	<u>Marking</u>	<u>Package Option</u>
PLL602-13OC	P602-13OC	TSSOP – Tube
PLL602-13OC-R	P602-13OC	TSSOP - Tape and Reel

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