AT91SAM9261-EK Evaluation Board

User Guide



Table of Contents

Section 1

Overview 1-1

1.1 Scope 1-1
1.2 Deliverables 1-1
1.3 The AT91SAM9261-EK Evaluation Board 1-1

Section 2

Setting Up the AT91SAM9261-EK Evaluation Board 2-1

2.1 Electrostatic Warning 2-1
2.2 Requirements 2-1
2.3 Layout 2-2
2.4 Powering Up the Board 2-4
2.5 Backup Power Supply 2-4
2.6 Getting Started 2-4
2.7 AT91SAM9261-EK Block Diagram 2-5

Section 3

Board Description 3-1

3.1 AT91SAM9261 Microcontroller 3-1
3.2 AT91SAM9261 Block Diagram 3-4
3.3 Memory 3-5
3.4 Clock Circuitry 3-5
3.5 Reset Circuitry 3-5
3.6 Shutdown Controller 3-5
3.7 Power Supply Circuitry 3-5
3.8 Remote Communication 3-5
3.9 Audio Stereo Interface 3-5
3.10 User Interface 3-5
3.11 Debug Interface 3-6
3.12 Expansion Slot 3-6
3.13 PIO Usage 3-7

Section 4

Configuration Straps 4-1

4.1 Configuration Straps 4-1

Section 5

Schematics 5-1

5.1 Schematics 5-1

Section 6

Errata 6-1

6.1 JTAGSEL S5 Footprint Selector 6-1

Section 7

Revision History 7-1

7.1 Revision History 7-1

Section 1

Overview

1.1 Scope

The AT91SAM9261-EK evaluation kit is an effective platform for evaluating chip performance and developing code for applications based on the AT91SAM9261.

This guide is a description of the hardware included in the AT91SAM9261-EK evaluation kit. Software files are available on the DVD-ROM included in the kit and described in "Deliverables" below.

1.2 Deliverables

The AT91SAM9261-EK package contains the following items:

- an AT91SAM9261-EK board
- one A/B-type USB cable
- one serial RS232 cable
- one RJ45 crossed Ethernet cable
- universal input AC/DC power supply with US and EU plug adapter
- one DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 The AT91SAM9261-EK Evaluation Board

The board is equipped with an AT91SAM9261 (217-ball LFBGA package) together with the following:

- 64 Mbytes of SDRAM memory
- 256 Mbytes of NAND Flash memory
- one Atmel® serial DataFlash®
- one USB device port interface
- two USB host port interfaces
- one DBGU serial communication port
- JTAG/ICE debug interface

- one Ethernet 100-base TX with three status LEDs
- one Atmel AT73C213 Audio DAC
- one 3.5" 1/4 VGA TFT LCD Module with TouchScreen and backlight
- one Power LED and two general-purpose LEDs
- four user input pushbuttons
- one wakeup input pushbutton
- one reset pushbutton
- one DataFlash SD/MMC card slot
- two expansion footprint connectors (solder side)
- one Lithium Coin Cell Battery Retainer for 12 mm cell size
- dual pitch prototyping area

Section 2

Setting Up the AT91SAM9261-EK Evaluation Board

2.1 Electrostatic Warning

The AT91SAM9261-EK evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM9261-EK evaluation board, the following items are required:

- the AT91SAM9261-EK evaluation board itself
- AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm

2.3 Layout

Figure 2-1. AT91SAM9261-EK Layout - Top View

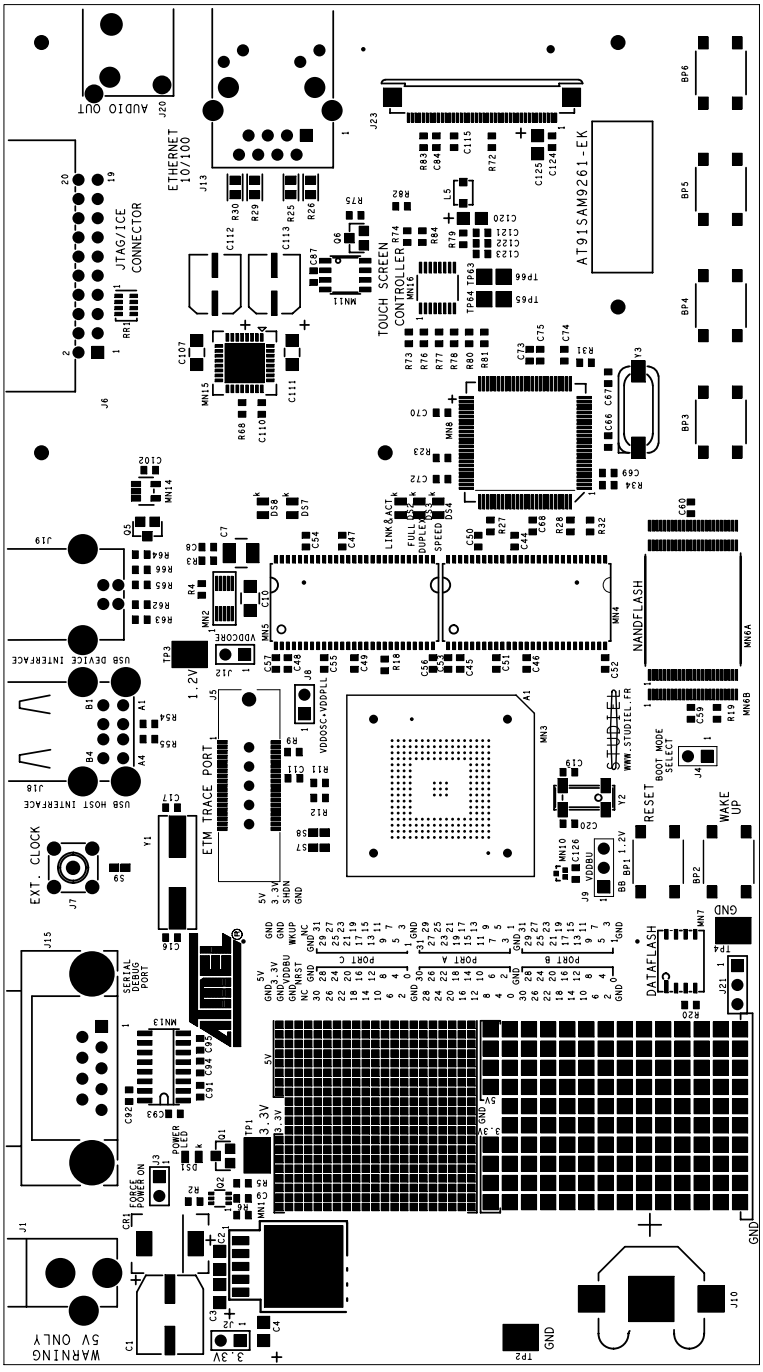
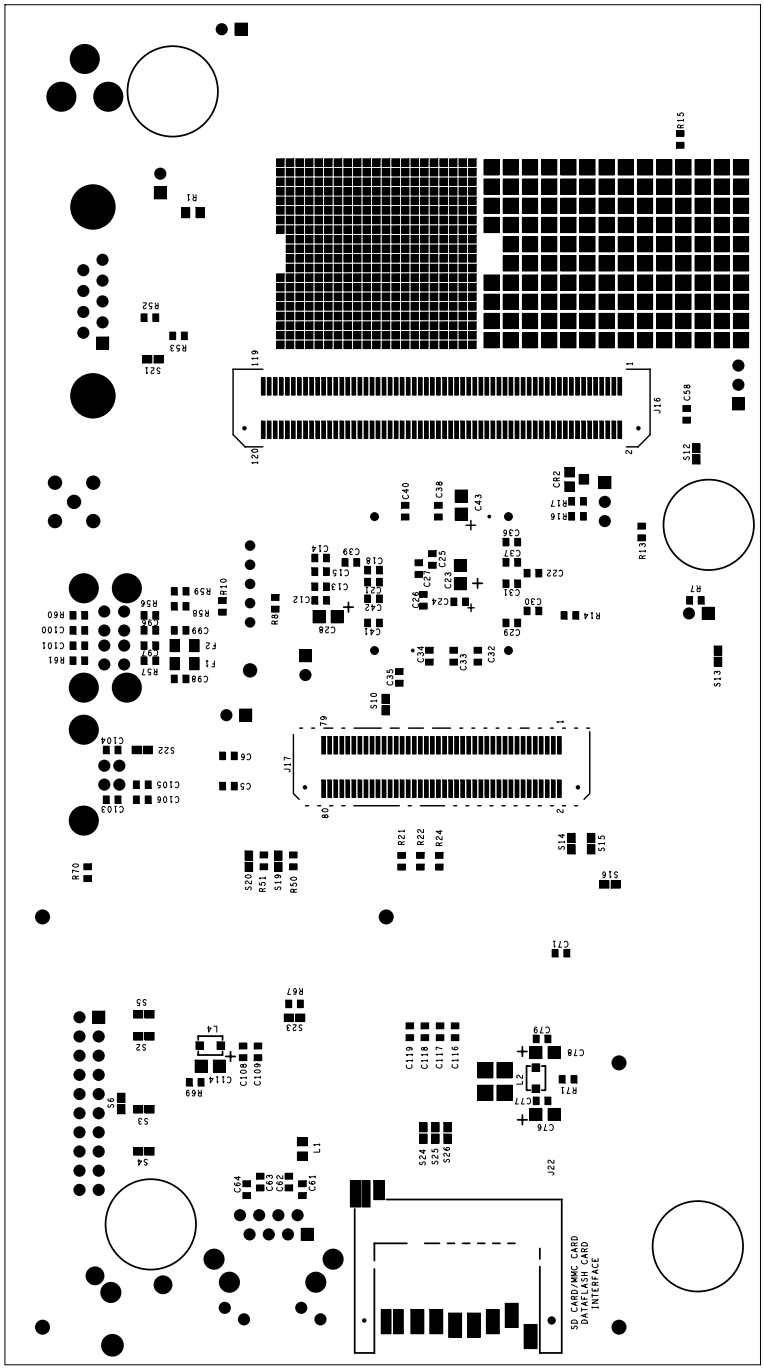


Figure 2-2. AT91SAM9261-EK Layout - Bottom View



2.4 Powering Up the Board

AT91SAM9261-EK requires 5V DC (±5%). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket (J1). The coaxial power plug center pin is positive polarity .

2.5 Backup Power Supply

The user has the possibility to add a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device. In this case, J9 configuration must to be set in position 1, 2.

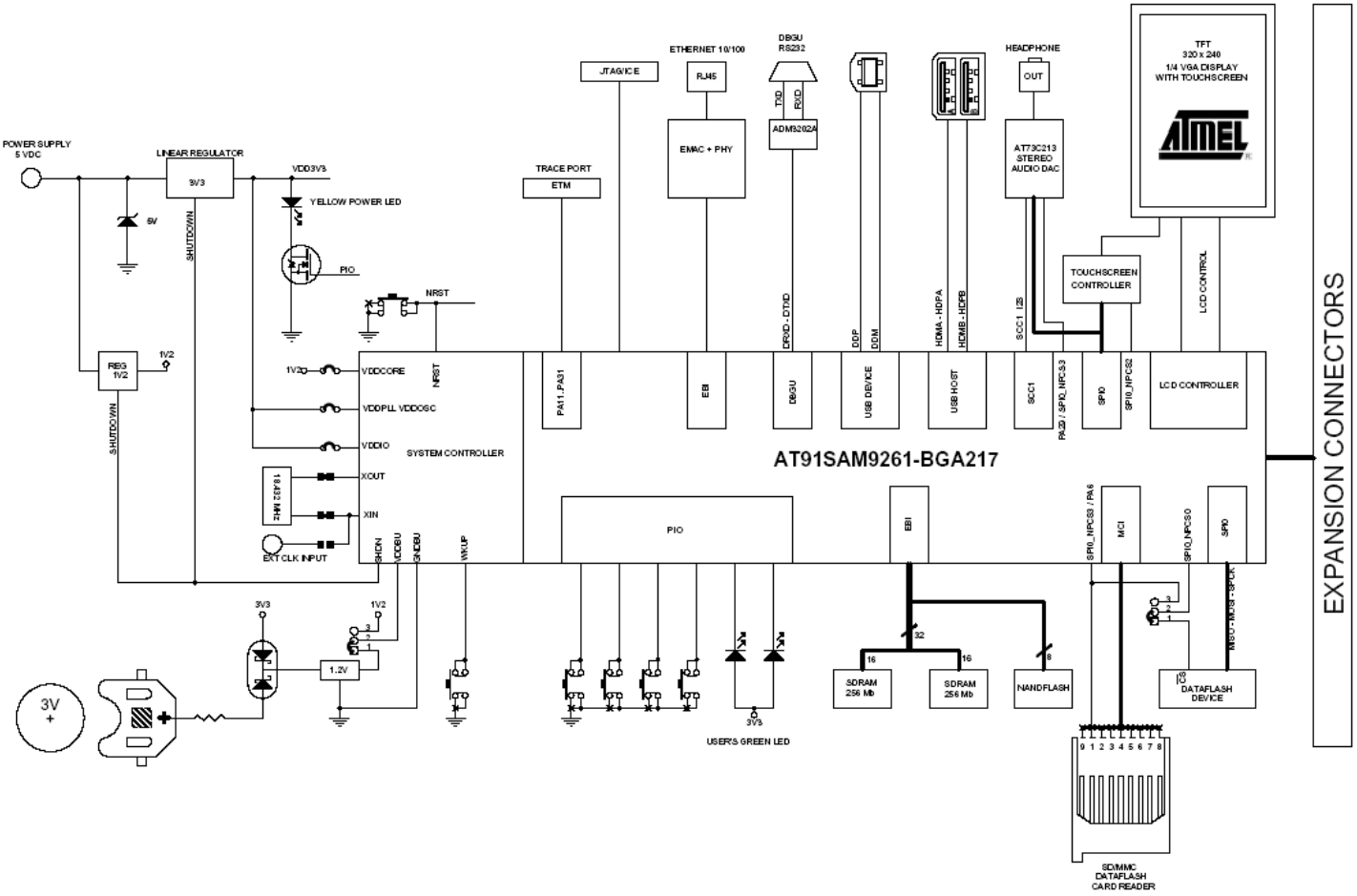
Refer to Table 4-1, “Configuration Jumpers and Straps”.

2.6 Getting Started

The AT91SAM9261-EK evaluation board is delivered with one CD-ROM allowing the user to begin evaluating the AT91 ARM Thumb 32-bit microcontroller quickly. Please refer to the AT91 web site, www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM9261-EK.

2.7 AT91SAM9261-EK Block Diagram

Figure 2-3. Block Diagram



Section 3

Board Description

3.1 AT91SAM9261 Microcontroller

- Incorporates the ARM926EJ-S™ ARM Thumb Processor
  - DSP Instruction Extensions
  - ARM Jazelle® Technology for Java® Acceleration
  - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
  - Mid-level implementation Embedded Trace Macrocell™
- Additional Embedded Memories
  - 32K Bytes of Internal ROM, Single-cycle Access at Maximum Bus Speed
  - 160K Bytes of Internal SRAM, Single-cycle Access at Maximum Processor or Bus Speed
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, NAND Flash and CompactFlash®
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 16-bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode (24-bit per Pixel), Resolution up to 2048 x 2048
- USB
  - USB 2.0 Full Speed (12 Mbits per second) Host Double Port
    Dual On-chip Transceivers
    Integrated FIFOs and Dedicated DMA Channels
  - USB 2.0 Full Speed (12 Mbits per second) Device Port
    On-chip Transceiver, 2-Kbyte Configurable Integrated FIFOs
- Bus Matrix
  - Handles Five Masters and Five Slaves
  - Boot Mode Select Option

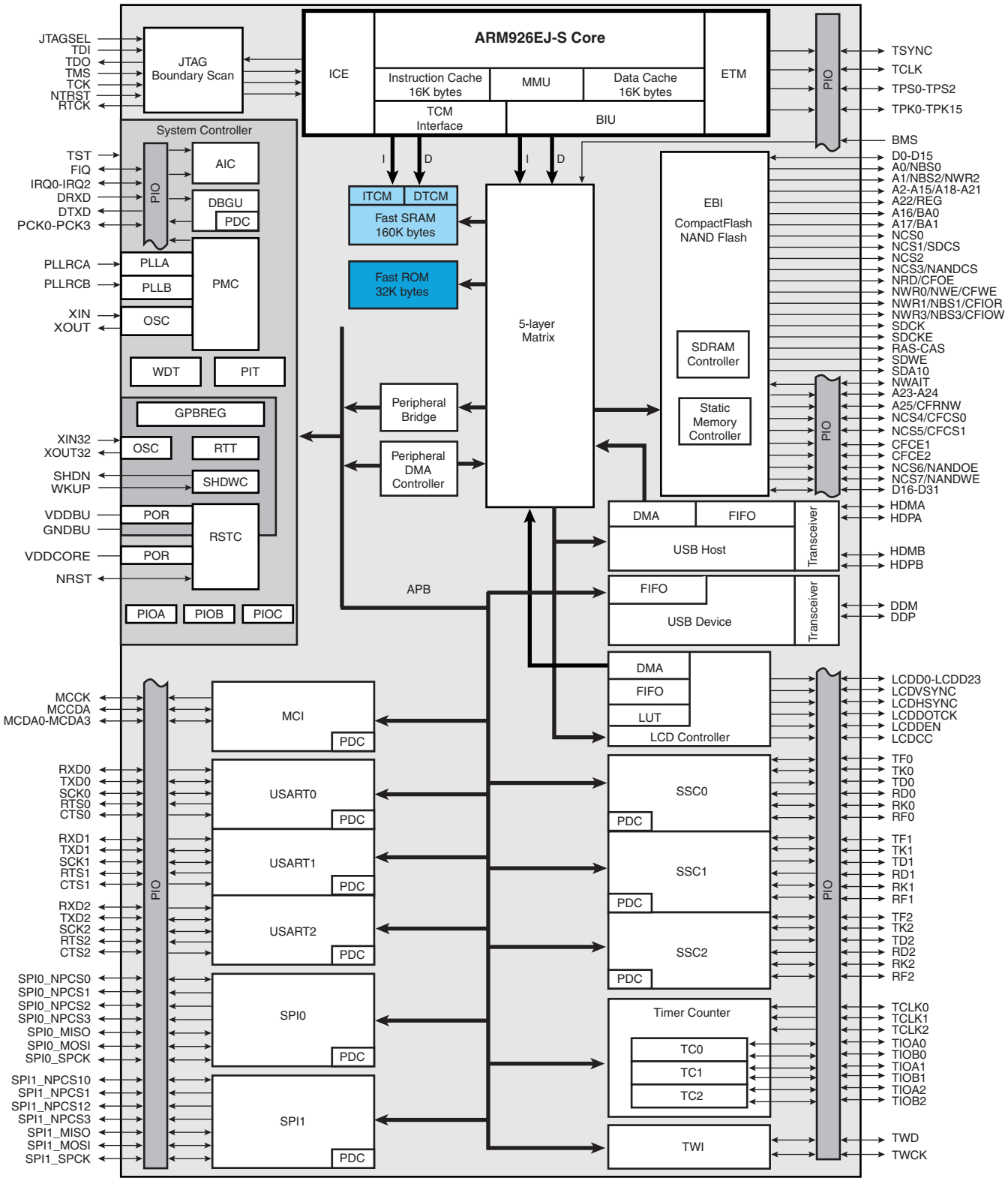
  - Remap Command

- Fully Featured System Controller (SYSC) for Efficient System Management, including
  - Reset Controller, Shutdown Controller, Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
  - Three 32-bit PIO Controllers
- Reset Controller (RSTC)
  - Based on Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32.768 kHz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator and two PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire USART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key Protected, Programmable Only Once, Windowed 12-bit Counter, Running at Slow Clock
- Real-Time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock
- Three 32-bit Parallel Input/Output Controllers (PIO) PIOA, PIOB and PIOC
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Nineteen Peripheral DMA (PDC) Channels

- Multimedia Card Interface (MCI)
  - Compliant with Multimedia Cards and SDCards
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC, MMC and SDCard Compliant
- Three Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware and Software Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel EEPROMs Supported
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 3.0V to 3.6V for VDDOSC and for VDDPLL
  - 2.7V to 3.6V for VDDIOP (Peripheral I/Os)
  - 1.65V to 1.95V and 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 217-ball LFBGA RoHS-compliant Package

3.2 AT91SAM9261 Block Diagram

Figure 3-1. Block Diagram



3.3 Memory

- 32 Kbytes of Internal ROM
- 160 Kbytes of Internal High-speed SRAM
- Atmel serial DataFlash
- 64 Mbytes of SDRAM memory
- 256 Mbytes of NAND Flash memory

3.4 Clock Circuitry

- 18.432 MHz standard crystal for the embedded oscillator
- 32.768 kHz standard crystal for the slow clock oscillator

3.5 Reset Circuitry

- Internal reset controller with a bi-directional reset pin
- External reset push button

3.6 Shutdown Controller

- Programmable shutdown and Wake-Up
- Wake-up push button

3.7 Power Supply Circuitry

- For dynamic power consumption, the AT91SAM9261 consumes a maximum of 50 mA on VDDCORE at maximum speed in typical conditions (1.2V, 25°C), processor running full-performance algorithm
- On-board 1.2V high efficiency step-down charge pump regulator with shutdown control
- On-board 3.3V linear regulator with shutdown control

3.8 Remote Communication

- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket
- USB V2.0 Full-speed Compliant, 12 Mbits per second (UDP)
- Two USB Host port V2.0 Full-speed Compliant, 12 Mbits per second (UHP)
- One Ethernet 100-base TX with three status LEDs

3.9 Audio Stereo Interface

- One Atmel stereo audio DAC AT73C213
- One 32 Ohm/20 mW Stereo Headset output (J20) with Master Volume and Mute Controls

3.10 User Interface

- Four user input pushbuttons
- Two user green LEDs
- One yellow power LED (can be also software controlled)

- One ¼ VGA display LCD with Touchscreen and white LED backlight

3.11 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM Port

3.12 Expansion Slot

- One DataFlash, SD/MMC card slot
- All I/Os of the AT91SAM9261 are routed to peripheral extension footprint connectors (J16 and J17). This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

3.13 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Comments	
PA0	SPI0_MISO	MCDA0	SD/MMC/DATAFLASH SOCKET (J9) & DATAFLASH DEVICE & TOUCH SCREEN CONTROLLER & AUDIO DAC	SPI0_MISO or MCI0_DA0
PA1	SPI0_MOSI	MCCDA	SD/MMC/DATAFLASH SOCKET (J9) & DATAFLASH DEVICE & TOUCH SCREEN CONTROLLER & AUDIO DAC	SPI0_MOSI or MCI0_CDA
PA2	SPI0_SPCK	MCCK	SD/MMC/DATAFLASH SOCKET (J9) & DATAFLASH DEVICE & TOUCH SCREEN CONTROLLER & AUDIO DAC	SPI0_SPCK or MCCK
PA3	SPI0_NPCS0		DATAFLASH DEVICE or DATAFLASH SOCKET (J9)	SPI0_NPCS0
PA4	SPI0_NPCS1	MCDA1	SD/MMC/DATAFLASH SOCKET (J9)	MCDA1
PA5	SPI0_NPCS2	MCDA2	SD/MMC/DATAFLASH SOCKET (J9)	MCDA2
PA6	SPI0_NPCS3	MCDA3	SD/MMC/DATAFLASH SOCKET (J9)	SPI0_NPCS3 or MCDA3
PA7	TWD	PCK0		
PA8	TWCK	PCK1		
PA9	DRXD	PCK2	SERIAL DEBUG PORT (J15)	DRXD
PA10	DTXD	PCK3	SERIAL DEBUG PORT (J15)	DTXD
PA11	TSYNC	SCK1	TOUCH SCREEN CONTROLLER (MN16) BUSY	PA11
PA12	TCLK	RTS1	TFT PANEL CONTROL (J23) POWER CONTROL IN	PA12
PA13	TPS0	CTS1	GREEN USER'S LED 1 (DS8)	PA13
PA14	TPS1	SCK2	GREEN USER'S LED 2 (DS7)	PA14
PA15	TPS2	RTS2		
PA16	TPK0	CTS2		
PA17	TPK1	TF1	I2S AUDIO DAC AT73C213 (MN15) LRFS	TF1
PA18	TPK2	TK1	I2S AUDIO DAC AT73C213 (MN15) BCLK	TK1
PA19	TPK3	TD1	I2S AUDIO DAC AT73C213 (MN15) SDIN	TD1
PA20	TPK4	RD1		
PA21	TPK5	RK1		
PA22	TPK6	RF1		
PA23	TPK7	RTS0	YELLOW POWER LED CONTROL (DS1)	PA23
PA24	TPK8	SPI1_NPCS1	USER'S PUSH BUTTON INPUT (BP6)	PA24
PA25	TPK9	SPI1_NPCS2	USER'S PUSH BUTTON INPUT (BP5)	PA25
PA26	TPK10	SPI1_NPCS3	USER'S PUSH BUTTON INPUT (BP4)	PA26
PA27	TPK11	SPI0_NPCS1	USER'S PUSH BUTTON INPUT (BP3)	PA27
PA28	TPK12	SPI0_NPCS2	TOUCH SCREEN CONTROLLER (MN16)	SPI0_NPCS2
PA29	TPK13	SPI0_NPCS3	I2S AUDIO DAC AT73C213 (MN15)	SPI0_NPCS3
PA30	TPK14	A23		
PA31	TPK15	A24		

Table 3-2. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Comments		
PB0	LCDVSYNC				
PB1	LCDHSYNC		TFT PANEL CONTROL (J23)	LCDHSYNC	
PB2	LCDDOTCK	PCK0	TFT PANEL CONTROL (J23)	LCDDOTCK	
PB3	LCDDEN		TFT PANEL CONTROL (J23)	LCDDEN	
PB4	LCDCC	LCDD2	TFT PANEL CONTROL (J23) BACKLIGHT	LCDCC	
PB5	LCDD0	LCDD3			
PB6	LCDD1	LCDD4			
PB7	LCDD2	LCDD5	TFT PANEL CONTROL (J23)	LCDD2	RED
PB8	LCDD3	LCDD6	TFT PANEL CONTROL (J23)	LCDD3	RED
PB9	LCDD4	LCDD7	TFT PANEL CONTROL (J23)	LCDD4	RED
PB10	LCDD5	LCDD10	TFT PANEL CONTROL (J23)	LCDD5	RED
PB11	LCDD6	LCDD11	TFT PANEL CONTROL (J23)	LCDD6	RED
PB12	LCDD7	LCDD12	TFT PANEL CONTROL (J23)	LCDD7	RED
PB13	LCDD8	LCDD13			
PB14	LCDD9	LCDD14			
PB15	LCDD10	LCDD15	TFT PANEL CONTROL (J23)	LCDD10	GREEN
PB16	LCDD11	LCDD19	TFT PANEL CONTROL (J23)	LCDD11	GREEN
PB17	LCDD12	LCDD20	TFT PANEL CONTROL (J23)	LCDD12	GREEN
PB18	LCDD13	LCDD21	TFT PANEL CONTROL (J23)	LCDD13	GREEN
PB19	LCDD14	LCDD22	TFT PANEL CONTROL (J23)	LCDD14	GREEN
PB20	LCDD15	LCDD23	TFT PANEL CONTROL (J23)	LCDD15	GREEN
PB21	TF0	LCDD16			
PB22	TK0	LCDD17			
PB23	TD0	LCDD18	TFT PANEL CONTROL (J23)	LCDD18	BLUE
PB24	RD0	LCDD19	TFT PANEL CONTROL (J23)	LCDD19	BLUE
PB25	RK0	LCDD20	TFT PANEL CONTROL (J23)	LCDD20	BLUE
PB26	RF0	LCDD21	TFT PANEL CONTROL (J23)	LCDD21	BLUE
PB27	SPI1_NPCS1	LCDD22	TFT PANEL CONTROL (J23)	LCDD22	BLUE
PB28	SPI1_NPCS0	LCDD23	TFT PANEL CONTROL (J23)	LCDD23	BLUE
PB29	SPI1_SPCK	IRQ2	USB DEVICE INTERFACE (J19) USB_CNX	PB29	
PB30	SPI1_MISO	IRQ1			
PB31	SPI1_MOSI	PCK2	I2S AUDIO DAC AT73C213 (MN15) MCLK	PCK2	

Table 3-3. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Comments	
PC0	NANDOE	NCS6	NAND FLASH DEVICE (MN6x)	NANDOE
PC1	NANDWE	NCS7	NAND FLASH DEVICE (MN6x)	NANDWE
PC2	NWAIT	IRQ0	TOUCH SCREEN CONTROLLER (MN16) PENIRQ	IRQ0
PC3	A25/CFRNW			
PC4	NCS4/CFCS0			
PC5	NCS5/CFCS1			
PC6	CFCE1			
PC7	CFCE2			
PC8	TXD0	PCK2		
PC9	RXD0	PCK3		
PC10	RTS0	SCK0	ETHERNET CONTROLLER (MN8) RST	PC10
PC11	CTS0	FIQ	ETHERNET CONTROLLER (MN8) IRQ	PC11
PC12	TXD1	NCS6		
PC13	RXD1	NCS7		
PC14	TXD2	SPI1_NPCS2	NAND FLASH DEVICE (MN6x) CHIP ENABLE (CE)	PC14
PC15	RXD2	SPI1_NPCS3	NAND FLASH DEVICE (MN6x) READY/BUSY (R/B)	PC15
PC16	D16	TCLK0	EBI DATA BUS D16	D16
PC17	D17	TCLK1	EBI DATA BUS D17	D17
PC18	D18	TCLK2	EBI DATA BUS D18	D18
PC19	D19	TIOA0	EBI DATA BUS D19	D19
PC20	D20	TIOB0	EBI DATA BUS D20	D20
PC21	D21	TIOA1	EBI DATA BUS D21	D21
PC22	D22	TIOB1	EBI DATA BUS D22	D22
PC23	D23	TIOA2	EBI DATA BUS D23	D23
PC24	D24	TIOB2	EBI DATA BUS D24	D24
PC25	D25	TF2	EBI DATA BUS D25	D25
PC26	D26	TK2	EBI DATA BUS D26	D26
PC27	D27	TD2	EBI DATA BUS D27	D27
PC28	D28	RD2	EBI DATA BUS D28	D28
PC29	D29	RK2	EBI DATA BUS D29	D29
PC30	D30	RF2	EBI DATA BUS D30	D30
PC31	D31	PCK1	EBI DATA BUS D31	D31

Section 4

Configuration Straps

4.1 Configuration Straps

Table 4-1 gives details on configuration straps on the AT91SAM9261-EK evaluation board and their default settings.

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J2	Closed	3.3V Jumper (1) This jumper footprint is provided for 3.3V power consumption measurement use. By default, it is closed. To use this feature, the user has to open the strap by cutting it before soldering a jumper.
J3	Closed	Forces power on. To use the software shutdown control, J3 must be opened.
J4	Opened	Enables Boot on the internal ROM
	Closed	Enables Boot on the NCS0
J8	Closed	VDDPLL Jumper (1)
J9	2-3	VDDBU Jumper select (1) 1-2 : Lithium 3V Battery 2-3 : 1.2V from VDDCORE
J12	Closed	VDDCORE Jumper (1)
J21	1-2	NPCS0 select 1-2: DataFlash device (MN7) 2-3: DataFlash card interface (J22) **Warning: In this case NPCS03 must be configured as input.**
S2	Opened	Disables the ICE NTRST input
S3	Closed	Enables the ICE RTCK return. S6 must be opened
S4	Closed	Enables the ICE NRST input
S5	Opened	Selects ICE mode or JTAG mode (See Section 6, Errata)
S6	Opened	Disables TCK <-> RTCK local loop. If S6 is closed, S3 must be opened.

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
S7-S8 S9	Closed Opened	Enables the use of 18.432 MHz crystal. If external clock used, S7-S8 must be opened and S9 closed.
S10	Closed	Enables the use of SDRAM (NCS1_SDCS)
S12	Opened	Disables Serial DataFlash write protect.
S13	Closed	Disables NAND FLASH write protect.
S14	Closed	Enables the use of interrupt ETHERNET MAC (PC11_FIQ).
S15	Closed	Enables the use of ETHERNET MAC (NCS2).
S16	Opened	Disables the use of NWAIT ETHERNET MAC signal (PC2_NWAIT)
S19	Closed	Enables the use of the User LED DS7 (PA14)
S20	Closed	Enables the use of the User LED DS8 (PA13)
S21	Closed	Enables the use of the DBGU RXD signal (PA9)
S22	Closed	Enables the use of the USB CNX detection (PB29)
S23	Closed	Enables the use of AUDIO DAC INTERFACE (NPCS03)
S24	Closed	Enables the use of TOUCH SCEEN CONTROLLER (NPCS02)
S25	Closed	Enables the use of TOUCH SCEEN CONTROLLER BUSY signal (PA11)
S26	Closed	Enables the use of TOUCH SCEEN CONTROLLER PENIRQ (PC2_IRQ0)
TP1	N.A	3.3V Test point.
TP2	N.A	GND Test point.
TP3	N.A	1.2V Test point.
TP4	N.A	GND Test point.
TP63	N.A	0 to 3.3V analog user's input
TP64	N.A	0 to 3.3V analog user's input
TP65	N.A	AGND of TP63
TP66	N.A	AGND of TP64

Note: 1. These jumpers are provided for measuring power consumption. By default, they are closed. To use this feature, the user has to open the strap and insert an ammeter.

Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Power Supply and Audio
- AT91SAM9261
- SDRAM and NAND Flash
- Ethernet
- LCD and User Interface
- Serial and I/O Expansion

10 SQUARE CM COPPER AREA FOR HEAT SINKING
WITH NO SOLDER MASK

REGULATED
5V ONLY

J1
C1 330µF
CR1 5V
R2 100K
C2 10µF 10V
MN1 LT1963AEQ-3.3
C3 10µF
C4 10µF
J2
TP1 3.3V
TP2 GND
M5V

R1 120R
POWER LED
DS1 YELLOW
Q1 IRLML2402
PA[0..31]
PA23

Q2 Si1563EDH
J3
FORCE POWER ON
C9 15PF
R5 10K
R6 10K
SHDN

C5 1µF
C6 1µF
C7 22µF
R3 100K
C8 10PF
C10 4.7µF
MN2 TPS60500
R4 200K
TP3 1.2V
TP4 GND

ADHESIVE FEET

Z3	Z4
11.1	11.1
Z7	Z8
11.1	11.1

AUDIO DAC INTERFACE

MN15 AT73C213

PAINN
VBAT
CBP
HPP
HPN
LPHN
PAINP
MONOP
MONON
LINER
LINEL
AUXP
AUXN
HSR
HSL

DOUT SPI0_MISO PA0
DIN SPI0_MOSI PA1
CLK SPI0_SPCK PA2
CS SPI0_NPCS3 PA29
S23
SMODE
RSTB
NRST
VDIG 3V3
AVDD VCC_DAC
AVDDHS
VCM C107 10µF
VREF C111 10µF
C108 100NF C109 100NF
C110 100NF
R67 100K
R68 47R
GND_DAC
MCLK PCK2 PB31
SDIN TD1 PA19
LRFS TF1 PA17
BCLK TK1 PA18
PA[0..31]
PB[0..31]

J20
3.5 PHONEJACK STEREO
C112 100µF 6V3
C113 100µF 6V3

INGND GNDB GNDD
8 33 23
GND_DAC

VCC_DAC L4 4.7µH 3V3
C114 10µF 10V
R69 0R
GND_DAC

REV	MODIF.	DES.	DATE	VER.	DATE
D		JPG	01/18/06		
C		JPG	14/09/05		
B		JPG	04/20/05		
A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05

ATMEL ROUSSET

AT91SAM9261-EK
POWER SUPPLY & AUDIO

SCALE 1/1

REV. D

SHEET 1/6

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AT91SAM9261

PC[0..15]
PB[0..31]
PA[0..31]

BOOT MODE SELECT
PB3 BMS
R7 1K
J4

ETM TRACE PORT

PA13	PIPESTAT[0]	38	37	TRACEPKT[8]	PA24
PA14	PIPESTAT[1]	36	35	TRACEPKT[9]	PA25
PA15	PIPESTAT[2]	34	33	TRACEPKT[10]	PA26
PA11	TRACESYNC	32	31	TRACEPKT[11]	PA27
PA16	TRACEPKT[0]	30	29	TRACEPKT[12]	PA28
PA17	TRACEPKT[1]	28	27	TRACEPKT[13]	PA29
PA18	TRACEPKT[2]	26	25	TRACEPKT[14]	PA30
PA19	TRACEPKT[3]	24	23	TRACEPKT[15]	PA31
PA20	TRACEPKT[4]	22	21	ICE_NTRST	
PA21	TRACEPKT[5]	20	19	TDI	
PA22	TRACEPKT[6]	18	17	TMS	
PA23	TRACEPKT[7]	16	15	TCK	
	VSUPPLY	14	13	ICE_RTCK	
	EXTTRIG	12	11	TDO	
PA12	TRACECLK	8	9	ICE_NRST	
		6	7	DBGRQ	
		4	5	GND	
		2	3		

3V3
R8 10K
R9 0R
C11 100NF
R10 10K
G1 G2 G3 G4 G5 J5
NOT POPULATED

ICE INTERFACE

3V3
RR1 100K
J6

ICE_NTRST	3	4	
TDI	5	6	
TMS	7	8	
TCK	9	10	
ICE_RTCK	11	12	
TDO	13	14	
ICE_NRST	15	16	
	17	18	
	19	20	

S2 S3 S4 S6 NRST

C12 4.7NF R11 1,96K 1%
C13 470pF
C14 4.7NF R12 1,5K 1%
C15 470pF
C16 10PF S7
Y1 18.4320MHz
C17 10PF S8 S9
J7 SMB MALE
C18 100NF
C19 10PF
32.768 kHz Y2
C20 10PF
3V3 J8
VDDOSC + VDDPLL CURRENT MEASURE
C21 100NF

Z14 CR1225 3V
MN10 R1100D121C (VDD GND OUT)
CR2 MMBD1704A
J10
R15 1K
C126 100NF
WAKE UP BP2
1V2 J9
R16 NOT POPULATED
R17 100K
VDDBU SHDN WKUP

PA0	R11	PA0/SPI0_MISO/MCDA0
PA1	T12	PA1/SPI0_MOSI/MCCDA
PA2	U13	PA2/SPI0_SPCK/MCCK
PA3	P10	PA3/SPI0_NPCS0
PA4	T13	PA4/SPI0_NPCS1/MCDA1
PA5	U14	PA5/SPI0_NPCS2/MCDA2
PA6	T14	PA6/SPI0_NPCS3/MCDA3
PA7	R12	PA7/TWD/PCK0
PA8	T15	PA8/TWCK/PCK1
PA9	U16	PA9/DRXD/PCK2
PA10	R13	PA10/DTXD/PCK3
PA11	T16	PA11/TSYNK/SCK1
PA12	U15	PA12/TCLK/RTS1
PA13	R14	PA13/TPS0/CTS1
PA14	T17	PA14/TPS1/SCK2
PA15	P13	PA15/TPS2/RTS2
PA16	P14	PA16/TPK0/CTS2
PA17	R15	PA17/TPK1/TF1
PA18	R17	PA18/TPK2/TK1
PA19	P16	PA19/TPK3/TD1
PA20	P17	PA20/TPK4/RD1
PA21	N15	PA21/TPK5/RK1
PA22	N14	PA22/TPK6/RF1
PA23	N16	PA23/TPK7/RTS0
PA24	N17	PA24/TPK8/SPI1_NPCS1
PA25	M14	PA25/TPK9/SPI1_NPCS2
PA26	M15	PA26/TPK10/SPI1_NPCS3
PA27	L15	PA27/TPK11/SPI0_NPCS1
PA28	M16	PA28/TPK12/SPI0_NPCS2
PA29	M17	PA29/TPK13/SPI0_NPCS3
PA30	L14	PA30/TPK14/A23
PA31	L16	PA31/TPK15/A24

DDP	A12	DDP
DDM	B12	DDM
HDPA	C12	HDPA
HDMA	B14	HDMA
HDPB	A13	HDPB
HDMB	A14	HDMB
	E17	TDI
	C17	TMS
	D17	TCK
	U17	RTCK
	F16	TDO
3V3 S5	B10	JTAGSEL
	F17	NTRST
	U9	PLLRCB
	U10	PLLRCA
	U12	XOUT
	U11	XIN
	T10	VDDOSC
	T11	GNDOSC
	A10	XOUT32
	A11	XIN32
	R10	VDDPLL
	P9	GNDPLL

LCDVSYNC/PB0	L17	PB0
LCDHSYNK/PB1	K16	PB1
LCDDOTCK/PCK0/PB2	K17	PB2
BMSLCDDENV/PB3	K15	PB3
LCDCC/LCDD2/PB4	J17	PB4
LCDD0/LCDD3/PB5	J16	PB5
LCDD1/LCDD4/PB6	H16	PB6
LCDD2/LCDD5/PB7	G17	PB7
LCDD3/LCDD6/PB8	J15	PB8
LCDD4/LCDD7/PB9	H14	PB9
LCDD5/LCDD10/PB10	G16	PB10
LCDD6/LCDD11/PB11	G15	PB11
LCDD7/LCDD12/PB12	H15	PB12
LCDD8/LCDD13/PB13	G14	PB13
LCDD9/LCDD14/PB14	E16	PB14
LCDD10/LCDD15/PB15	E14	PB15
LCDD11/LCDD19/PB16	D16	PB16
LCDD12/LCDD20/PB17	E15	PB17
LCDD13/LCDD21/PB18	B17	PB18
LCDD14/LCDD22/PB19	D15	PB19
LCDD15/LCDD23/PB20	C16	PB20
TF0/LCDD16/PB21	E14	PB21
TK0/LCDD17/PB22	D14	PB22
TD0/LCDD18/PB23	A17	PB23
RD0/LCDD19/PB24	B16	PB24
RK0/LCDD20/PB25	B15	PB25
RF0/LCDD21/PB26	A15	PB26
SPI1_NPCS1/LCDD22/PB27	D13	PB27
SPI1_NPCS0/LCDD23/PB28	D12	PB28
SPI1_SPCK/IRQ2/PB29	C13	PB29
SPI1_MISO/IRQ1/PB30	B13	PB30
SPI1_MOSI/PCK2/PB31		PB31

NANDOE/NCS6/PC0	U2	PC0
NANDWE/NCS7/PC1	P6	PC1
NWAIT/IRQ0/PC2	T4	PC2
A25/CFRNW/PC3	R6	PC3
NCS4/CFCS0/PC4	U3	PC4
NCS5/CFCS1/PC5	T6	PC5
CFCE1/PC6	U5	PC6
CFCE2/PC7	P7	PC7
TXD0/PCK2/PC8	R7	PC8
RXD0/PCK3/PC9	T7	PC9
RTS0/SCK0/PC10	T8	PC10
CTS0/FIQ/PC11	P8	PC11
TXD1/NCS6/PC12	R8	PC12
RXD1/NCS7/PC13	U8	PC13
TXD2/SPI1_NPCS2/PC14	R9	PC14
RXD2/SPI1_NPCS3/PC15	T9	PC15
D16/TCLK0/PC16	P1	D16
D17/TCLK1/PC17	N2	D17
D18/TCLK2/PC18	M3	D18
D19/TIOA0/PC19	R1	D19
D20/TIOB0/PC20	T1	D20
D21/TIOA1/PC21	R2	D21
D22/TIOB1/PC22	P3	D22
D23/TIOA2/PC23	T2	D23
D24/TIOB2/PC24	P4	D24
D25/TF2/PC25	U1	D25
D26/TK2/PC26	T3	D26
D27/TD2/PC27	R4	D27
D28/RD2/PC28	P5	D28
D29/RK2/PC29	R5	D29
D30/RF2/PC30	P2	D30
D31/PCK1/PC31	N3	D31

D[0..31]
A[0..22]

D0	G1	D0
D1	G2	D1
D2	H1	D2
D3	H2	D3
D4	J1	D4
D5	J2	D5
D6	K1	D6
D7	K4	D7
D8	K2	D8
D9	L1	D9
D10	K3	D10
D11	L2	D11
D12	L3	D12
D13	M1	D13
D14	N1	D14
D15	M2	D15

NBS0/A0	D8	A0
NWR2/NBS2/A1	B8	A1
A2	A8	A2
A3	A7	A3
A4	B7	A4
A5	D7	A5
A6	A6	A6
A7	B6	A7
A8	C6	A8
A9	A5	A9
A10	D6	A10
A11	B5	A11
A12	A4	A12
A13	B4	A13
A14	A3	A14
A15	B3	A15
BA0/A16	A2	A16
BA1/A17	C4	A17
A18	B2	A18
A19	A1	A19
A20	B1	A20
A21	C2	A21
A22	C1	A22

RAS	F2	RAS
CAS	J4	CAS
SDWE	G3	SDWE
SDA10	F4	SDA10
SDCKE	F1	SDCKE
SDCK	H4	SDCK
NCS0	F4	NCS0
SDCS/NCS1	D2	SDCS_NCS1
NCS2	D1	NCS2
NANDCS/NCS3	G4	SMCS_NCS3
CFOE/NRD	E3	CFOE_NOE_NRD
CFWE/NWE/NWR0	E2	CFWE_NWE_NWR0
CFIOR/NBS1/NWR1	E1	CFIOR_NBS1_NWR1
CFIOW/NBS3/NWR3	F3	CFIOW_NBS3_NWR3
NRST	F15	NRST
TST	C10	
NC	A9	
NC	C14	
NC	D10	

3V3 R13 1K
R14 1K
BP1 RESET

WKUP	B11	
SHDN	D9	
VDDBU	B9	
GNDBU	C9	
VDDCORE	D5	
VDDCORE	K14	
VDDCORE	M4	
VDDCORE	P12	
GND	A16	
GND	C7	
GND	C11	
GND	D3	
GND	H8	
GND	H9	
GND	H10	
GND	J3	
GND	J8	
GND	J9	
GND	J10	
GND	K8	
GND	K9	
GND	K10	
GND	R3	
GND	R16	
GND	U4	
GND	U7	
VDDIOM	C3	
VDDIOM	C5	
VDDIOM	C8	
VDDIOM	D4	
VDDIOM	H3	
VDDIOM	L4	
VDDIOM	N4	
VDDIOP	C15	
VDDIOP	D11	
VDDIOP	J14	
VDDIOP	P11	
VDDIOP	P15	
VDDIOP	T5	
VDDIOP	U6	

C22 100NF
C24 100NF C26 100NF
C23 10µF 10V C25 100NF C27 100NF
J12 VDDCORE CURRENT MEASURE 1V2

C28 10µF 10V
C29 100NF C30 100NF C31 100NF C32 100NF C33 100NF C34 100NF C35 100NF C36 100NF C37 100NF C38 100NF C39 100NF C40 100NF C41 100NF C42 100NF
3V3 C43 10µF 10V

REV	MODIF.	DES.	DATE	VER.	DATE
D			JPG	01/18/06	
C			JPG	14/09/05	
B			JPG	04/20/05	
A	INIT EDIT		JPG	02/23/05	XXX XX/XX/05

ATMEL ROUSSET
AT91SAM9261-EK
AT91SAM9261
SCALE 1/1
REV. D
SHEET 2/6

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EBI SDRAM INTERFACE

A[0..22]
D[0..31]
RAS
CAS
SDWE
SDA10
SDCKE
SDCK
CFIOR_NBS1_NWR1
CFIOW_NBS3_NWR3
SDCS_NCS1

MN4 MT48LC16M16A2 — 256 Mbits
MN5 MT48LC16M16A2 — 256 Mbits

3V3
R18 100K
S10

C50 100NF, C51 100NF, C52 100NF, C53 100NF
C44 100NF, C45 100NF, C46 100NF
C54 100NF, C55 100NF, C56 100NF, C57 100NF
C47 100NF, C48 100NF, C49 100NF

D[0..31]
PC[0..15]

DUAL FOOTPRINT

MN6A 16-bit bus width — NOT POPULATED
MN6B 8-bit bus width

R19 100K
S13
C60 100NF
C59 100NF

PA[0..31]

MN7

R20 100K
NRST
S12
WRITE PROTECT NORMALLY OPEN
C58 100NF

J21
R72 10K
SD CARD / MMC CARD
DATAFLASH CARD
INTERFACE
J22
FPS009
C115 100NF

D		JPG	01/18/06		
C		JPG	14/09/05		
B		JPG	04/20/05		
A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05
REV	MODIF.	DES.	DATE	VER.	DATE

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AT91SAM9261-EK

SDRAM & NANDFLASH

SCALE 1/1

REV. D

SHEET 3/6

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Note1: 8/16 bit DataBus selection; Removed R27 when using 16-bit mode; otherwise is 8-bit mode.

NOT POPULATED

DM9000

MN8

DS2 GREEN LINK&ACT R21 1K
DS3 YELLOW FULL DUPLEX R22 1K
DS4 GREEN SPEED 100 R24 1K
R23 4,7K
R27 4,7K
R28 4,7K
R31 6,80K 1%
R32 100K
R34 4,7K

L1 742792093
C61 100NF
R25 49R9 1%
R26 49R9 1%
C62 100NF
C63 100NF
R29 49R9 1%
R30 49R9 1%
C64 100NF
J13 J0026D21
1nF
75

Y3 25MHz
C66 22PF
C67 22PF

L2 4.7µH
C76 10µF 10V
C77 100NF
C78 10µF 10V
C79 100NF
R70 0R
R71 0R

C68 100NF
C69 100NF
C70 100NF
C71 100NF
C72 100NF
C73 100NF
C74 100NF
C75 100NF

D[0..15]
A[0..22]
PC[0..15]
NRST
D15 D14 D13 D12 D11 D10 D9 D8
A2
PC11 FIQ S14
CFOE_NOE_NRD
CFWE_NWE_NWR0
NCS2 S15
D0 D1 D2 D3 D4 D5 D6 D7
PC10 RST
PC2 NWAIT S16
NOT USED

D		JPG	01/18/06		
C		JPG	14/09/05		
B		JPG	04/20/05		
A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05
REV	MODIF.	DES.	DATE	VER.	DATE

AT91SAM9261-EK
ETHERNET
SCALE 1/1
REV. D
SHEET 4/6

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Z17 TX09D71VM1CCA

54132-4097

J23

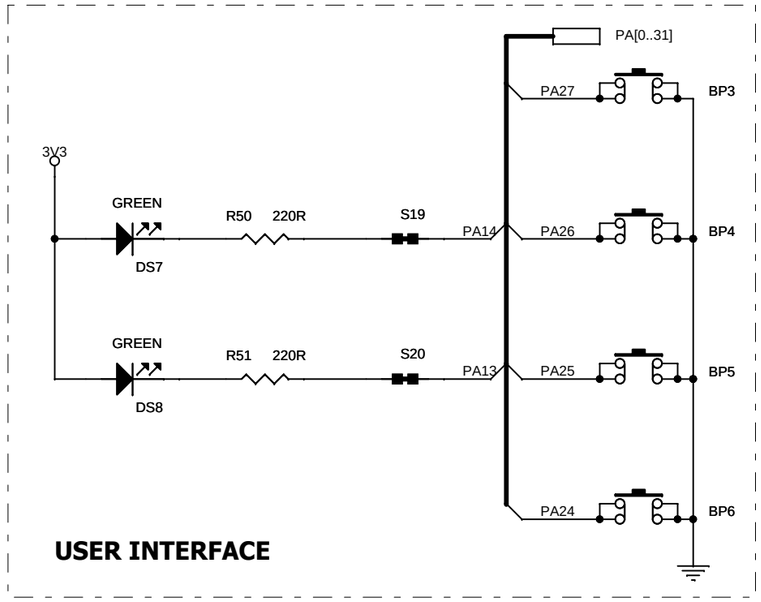
X_RIGHT
Y_LOW
X_LEFT
Y_UP
Vctrl
PCI

B0	LCDD18	PB23	
B1	LCDD19	PB24	
B2	LCDD20	PB25	
B3	LCDD21	PB26	
B4	LCDD22	PB27	
B5	LCDD23	PB28	
G0	LCDD10	PB15	
G1	LCDD11	PB16	
G2	LCDD12	PB17	
G3	LCDD13	PB18	
G4	LCDD14	PB19	
G5	LCDD15	PB20	
R0	LCDD2	PB7	
R1	LCDD3	PB8	
R2	LCDD4	PB9	
R3	LCDD5	PB10	
R4	LCDD6	PB11	
R5	LCDD7	PB12	
DTMG	LCDDEN	PB3	
HSYNC	LCDHSYNC	PB1	
DCLK	LCDDOTCK	PB2	

VCTRL
3V3
PB[0..31]
PB4
LCDCC
R83 10K
C84 100NF
C124 100NF
C125 10V 10µF
R75 10K
C87 4.7NF
MN11
MC34064D
RST N.C
IN N.C
N.C N.C
GND N.C
M5V
PA12 POWER CONTROL IN
Q6 IRLML2402

TOUCH SCREEN CONTROLLER

X_LEFT R73 0R
Y_UP R76 0R
X_RIGHT R77 0R
Y_LOW R78 0R
C116 10NF
C117 10NF
C118 10NF
C119 10NF
NOT POPULATED
R80 100K
R81 100K
TP63
TP64
TP65
TP66
AGND
MN16
XP
YP
XM
YM
IN3
IN4
VREF
VCC
VCC
GND
ADS7843E
DCLK
DIN
DOUT
CS
BUSY
PENIRQ
R84 100K
R74 47R
S24
S25
S26
PA12
PA2
PA1
PA0
PA28
PA11
PC2
SPI0_SPCK
SPI0_MOSI
SPI0_MISO
SPI0_NPCS2
BUSY
IRQ0
PA[0..31]
PC[0..15]
R79 0R
L5 4.7µH
C120 10µF 10V
R82 0R
C122 100NF
C121 100NF
C123 100NF
TWO USER'S ANALOG INPUTS
Full-Scale Input Span 0 to VREF



REV	MODIF.	DES.	DATE	VER.	DATE
D		JPG	01/18/06		
C		JPG	14/09/05		
B		JPG	04/20/05		
A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05

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AT91SAM9261-EK

LCD & USER'S INTERFACE

SCALE 1/1

REV. D

SHEET 5/6

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EXPANSION CONNECTORS

NOT POPULATED

PA[0..31] PB[0..31] PC[0..15]

A[0..22] D[0..31]

J16

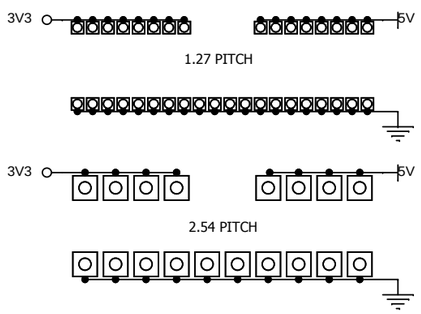
	1	2	
PB0	3	4	PB1
PB2	5	6	PB3
PB4	7	8	PB5
PB6	9	10	PB7
PB8	11	12	PB9
PB10	13	14	PB11
PB12	15	16	PB13
PB14	17	18	PB15
PB16	19	20	PB17
PB18	21	22	PB19
PB20	23	24	PB21
PB22	25	26	PB23
PB24	27	28	PB25
PB26	29	30	PB27
PB28	31	32	PB29
PB30	33	34	PB31
	35	36	
PA0	37	38	PA1
PA2	39	40	PA3
PA4	41	42	PA5
PA6	43	44	PA7
PA8	45	46	PA9
PA10	47	48	PA11
PA12	49	50	PA13
PA14	51	52	PA15
PA16	53	54	PA17
PA18	55	56	PA19
PA20	57	58	PA21
PA22	59	60	PA23
PA24	61	62	PA25
PA26	63	64	PA27
PA28	65	66	PA29
PA30	67	68	PA31
	69	70	
PC0	71	72	PC1
PC2	73	74	PC3
PC4	75	76	PC5
PC6	77	78	PC7
PC8	79	80	PC9
PC10	81	82	PC11
PC12	83	84	PC13
PC14	85	86	PC15
D16	87	88	D17
D18	89	90	D19
D20	91	92	D21
D22	93	94	D23
D24	95	96	D25
D26	97	98	D27
D28	99	100	D29
D30	101	102	D31
	103	104	
	105	106	
NRST	107	108	
VDDBU	109	110	WKUP
	111	112	SHDN
3V3	113	114	
	115	116	3V3
5V	117	118	
	119	120	5V

NOT POPULATED

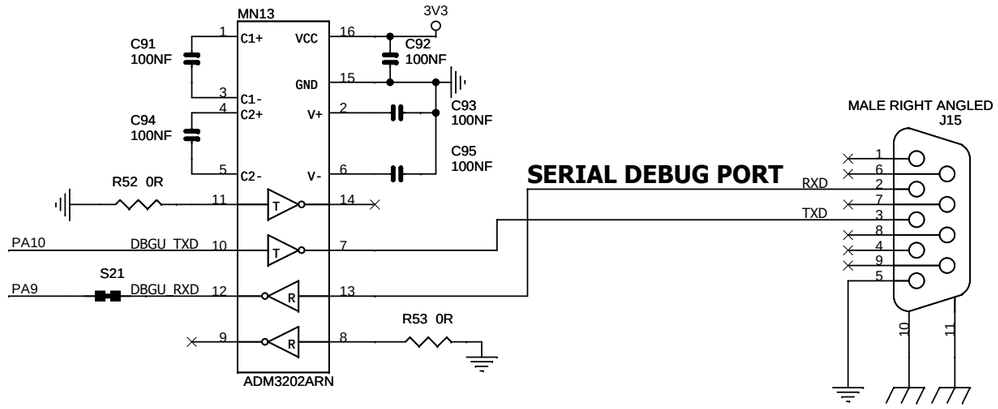
J17

	1	2	
A1	3	4	A2
A4	5	6	A3
A7	7	8	A6
A11	9	10	A9
A13	11	12	A12
A15	13	14	A14
A18	15	16	A16
A0	17	18	A19
A10	19	20	A5
A17	21	22	A8
A21	23	24	A20
A22	25	26	
	27	28	
SDCS_NCS1	29	30	SDCKE
CFIOR_NBS1_NWR1	31	32	NCS2
CFOE_NOE_NRD	33	34	CFWE_NWE_NWR0
CFIOW_NBS3_NWR3	35	36	SDA10
RAS	37	38	NCS0
SDWE	39	40	
CAS	41	42	SDCK
	43	44	
	45	46	SMCS_NCS3
D2	47	48	D1
D3	49	50	D0
D10	51	52	D5
D8	53	54	D7
D12	55	56	D4
D11	57	58	D15
D6	59	60	D13
D9	61	62	D14
	63	64	
	65	66	
	67	68	
	69	70	
3V3	71	72	3V3
	73	74	
3V3	75	76	3V3
	77	78	
5V	79	80	5V

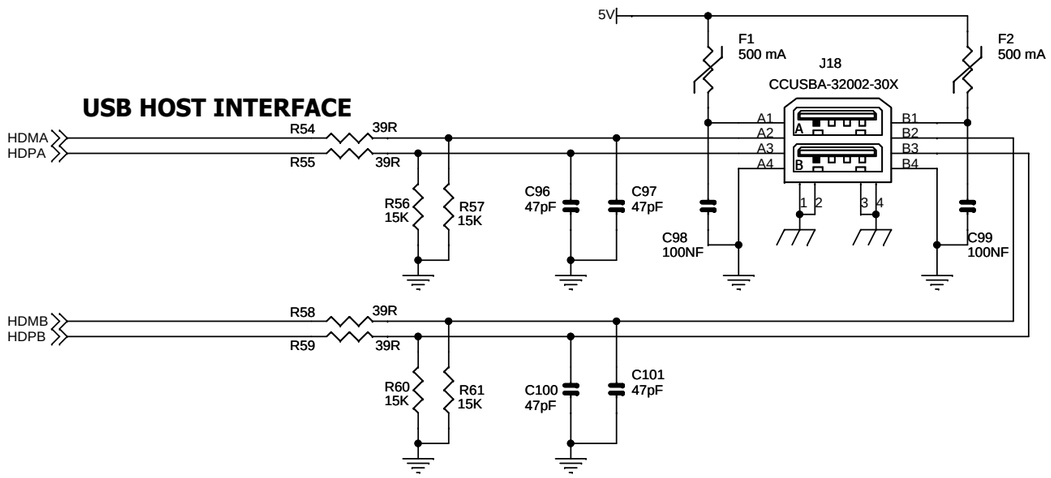
USER'S GRID AERA



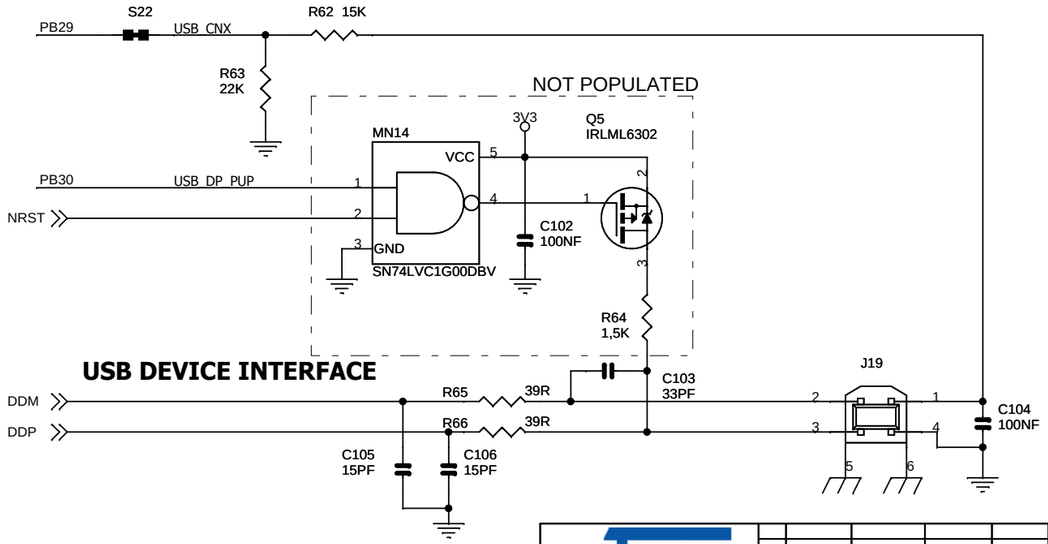
SERIAL DEBUG PORT



USB HOST INTERFACE



USB DEVICE INTERFACE



D		JPG	01/18/06		
C		JPG	14/09/05		
B		JPG	04/20/05		
A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05
REV	MODIF.	DES.	DATE	VER.	DATE

AT91SAM9261-EK

SERIAL & I/O EXPANSION

SCALE 1/1

REV. D

SHEET 6/6

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Section 6

Errata

6.1 JTAGSEL S5 Footprint Selector

For JTAG selection, the S5 footprint must never be soldered, else the chip can be damaged.

By default, the JTAGSEL input pin integrates a pull-down resistor (ICE mode).

To select JTAG mode, the designer should connect the JTAGSEL input pin to VDDBU power.

Section 7

Revision History

7.1 Revision History

Table 7-1.

Document	Comments	Change Request Ref.
6198A	First issue.	
6198B	Removed DataFlash card from list in Section 1.2 ”Deliverables”.	
	Removed references to 32-bit serial DataFlash, ref. AT45DB321C in Section 1.3 ”The AT91SAM9261-EK Evaluation Board”, Figure 2-3 on page 5 “Block Diagram”, Section 3.3 ”Memory”, Table 4-1 “Configuration Jumpers and Straps” and in schematic 3/6 “SDRAM and NANDFLASH”. In Figure 2-3 on page 5 “Block Diagram” changed size of NANDFlash to 2 Gb.	2733
	Specified TRACE PORT as NOT POPULATED in Figure 2-3 on page 5 “Block Diagram”. Changed all instances of DNP to NOT POPULATED in Schematics 2/6 “AT91SAM9261”, 4/6 “Ethernet” and 5/6 “LCD and User Interface”.	2736
6198C	New Figure 2-1 “AT91SAM9261-EK Layout - Top View” and new Figure 2-2 “AT91SAM9261-EK Layout - Bottom View”	3542
	Updated Section 2.6 ”Getting Started”.	
	In Section 2.3 ”Layout”, updated Figure 2-3, “Block Diagram”.	
	Added Section 3.13 ”PIO Usage”.	
	In Section 4.1 ”Configuration Straps”, updated Table 4-1, S5, with reference to Errata section.	
	Updated all schematics in Section 5.1 ”Schematics”.	
	Added Section 6, Errata.	

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