19-0499; Rev 1; 7/98

Low-Power, High-Speed, Single-Supply Op Amp + Comparator + Reference ICs

General Description

The MAX9000 family features the combination of a high-speed operational amplifier, a 185ns comparator, and a precision 1.230V reference. These devices operate from a single +2.5V to +5.5V supply and draw less than 500µA of quiescent current. The MAX9001/MAX9004 feature a shutdown mode that reduces supply current to 2µA and puts the outputs into a high-impedance state, making them ideal for portable and battery-powered applications.

The amplifiers in the MAX9000/MAX9001/MAX9002 are unity-gain stable with a 1.25MHz gain-bandwidth product, while the amplifiers in the MAX9003/MAX9004/MAX9005 are stable for closed-loop gains of +10V/V or greater with an 8MHz gain-bandwidth product. The input common-mode voltage extends from 150mV below the negative supply to within 1.2V of the positive supply for the amplifier, and to within 1.1V for the comparator. The amplifier and comparator outputs can swing Rail-to-Rail® and deliver up to ±2.5mA and ±4.0mA, respectively, to an external load while maintaining excellent DC accuracy. The unique design of the comparator output stage substantially reduces switching current during output transitions, virtually eliminating power-supply glitches.

The comparator's ±2mV of built-in hysteresis provides noise immunity and prevents oscillations even with a slow-moving input signal. The MAX9000/MAX9001/MAX9003/MAX9004 have an internal 1.230V ±1% precision reference with a low 8ppm/°C temperature coefficient that can sink or source up to 1mA. The amplifier and reference are stable with capacitive loads up to 250pF and 100nF, respectively. The comparator's inverting input is internally connected to the reference output in the MAX9000/MAX9003.

Applications

Single-Supply Zero-Crossing Detector	Photodiode Preamps
	Smart Card Readers
Instruments, Terminals, and Bar-Code Readers	Infrared Receivers for Remote Controls
Keyless Entry	Sensor Signal Detection

Features

- ♦ **Op Amp + Comparator + Reference in Space-Saving µMAX Package**
- ♦ **+2.5V to +5.5V Single-Supply Voltage Range**
- ♦ **340µA Supply Current (MAX9002/MAX9005)**
- ♦ **Unity-Gain Stable (GBW = 1.25MHz) and Decompensated ($A_V \geq$ 10V/V, GBW = 8MHz) Options**
- ♦ **Op-Amp/Comparator Outputs Swing Rail-to-Rail**
- ♦ **Ground-Sensing Inputs for Both Op Amp and Comparator**
- ♦ **Op Amp Stable with Capacitive Loads up to 250pF**
- ♦ **Internal ±2mV Comparator Hysteresis**
- ♦ **Fast 185ns Propagation-Delay Comparator**
- ♦ **No Phase Reversal for Overdriven Inputs (Both Op Amp and Comparator)**
- ♦ **Internal 1.230V Precision Reference (MAX9000/MAX9001/MAX9003/MAX9004)**
  - **±1% Initial Accuracy**
  - **Low 8ppm/°C Temperature Drift**
  - **Sink or Source up to 1mA**
  - **Stable for Capacitive Loads up to 100nF**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9000EUA	-40°C to +85°C	8 µMAX
MAX9000ESA	-40°C to +85°C	8 SO
MAX9001EUB	-40°C to +85°C	10 µMAX
MAX9001ESD	-40°C to +85°C	14 SO

Ordering Information continued at end of data sheet.

Pin Configurations and Typical Operating Circuit appear at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Selector Guide

PART	INTERNAL PRECISION REFERENCE	OP-AMP GAIN STABILITY (V/V)	SHUTDOWN	OP-AMP GAIN BANDWIDTH (MHz)	PIN-PACKAGE
MAX9000	Yes	1	No	1.25	8 SO/µMAX
MAX9001	Yes	1	Yes	1.25	10 µMAX, 14 SO
MAX9002	No	1	No	1.25	8 SO/µMAX
MAX9003	Yes	10	No	8	8 SO/µMAX
MAX9004	Yes	10	Yes	8	10 µMAX, 14 SO
MAX9005	No	10	No	8	8 SO/µMAX

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS}) ....-0.3V to +6V
Voltage Inputs (AIN_, CIN_).............(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Output Short-Circuit Duration (AOUT, COUT, REF)...Continuous to either V_{SS} or V_{DD}
Continuous Power Dissipation (T_A = +70°C)
  8-Pin SO (derate 5.88mW/°C above +70°C).................471mW
  8-Pin µMAX (derate 4.1mW/°C above +70°C)..............330mW
  10-Pin µMAX (derate 5.6mW/°C above +70°C)............444mW
  14-Pin SO (derate 8.3mW/°C above +70°C).................667mW
Operating Temperature Range
  MAX900_E _ _...-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.5V to +5.5V, V_{SS} = 0, $\overline{SHDN}$ = V_{DD} (MAX9001/MAX9004 only), $V_{CM(OP\ AMP)}$ = 0, V_{AOUT} = V_{DD} / 2, $V_{CM(COMP)}$ = 0 (for MAX9001/MAX9002/MAX9004/MAX9005), COUT = low, $I_{OUT(REF)}$ = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR tests		2.5		5.5	V
Supply Current	I_{DD}	MAX9000/MAX9001/ MAX9003/MAX9004	V_{DD} = 3V		410	500	µA
			V_{DD} = 5V		450	550	
		MAX9002/MAX9005	V_{DD} = 3V		340	425	µA
			V_{DD} = 5V		375	475	
Supply Current in Shutdown	$I_{\overline{SHDN}}$	MAX9001/MAX9004 ($V_{\overline{SHDN}}$ = 0)			2	5	µA
Shutdown Input Bias Current	$I_{IN(\overline{SHDN})}$	MAX9001/MAX9004 ($V_{\overline{SHDN}}$ = 0 to V_{DD})			1	2.5	µA
Shutdown Logic High	$V_{IH(\overline{SHDN})}$			0.7 x V_{DD}			V
Shutdown Logic Low	$V_{IL(\overline{SHDN})}$					0.3 x V_{DD}	V
OP AMP							
Input Offset Voltage	V_{OS}	MAX900_ES_			±0.5	±1.5	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}	MAX900_ES_			±1		µV/°C
Input Bias Current	I_{BIAS}	AIN+, AIN-			±0.05	±2	nA
Input Offset Current		AIN+, AIN-			±0.02	±1	nA
Input Resistance	R_{IN}	Differential or common mode			1000		MΩ
Input Common-Mode Voltage Range	CMVR	Guaranteed by CMRR test		-0.15		V_{DD} - 1.2	V
Common-Mode Rejection Ratio	CMRR	MAX900_ES_, (V_{SS} - 0.15V) ≤ V_{CM} ≤ (V_{DD} - 1.2V), V_{DD} = 5.5V		72	96		dB
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.5V to 5.5V		74	100		dB
Output Resistance		A_V = 1V/V			0.01		Ω
Output Short-Circuit Current		Shorted to V_{SS}			10		mA
		Shorted to V_{DD}			65		
Disabled Mode Output Leakage	I_{OUT} (DISABLED)	$V_{\overline{SHDN}}$ ≤ (0.3V x V_{DD}), V_{AOUT} = 0 to V_{DD}			±0.01	±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.5V to +5.5V, V_{SS} = 0, $\overline{SHDN}$ = V_{DD} (MAX9001/MAX9004 only), $V_{CM(OP\ AMP)}$ = 0, V_{AOUT} = V_{DD} / 2, $V_{CM(COMP)}$ = 0 (for MAX9001/MAX9002/MAX9004/MAX9005), COUT = low, $I_{OUT(REF)}$ = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	A_{VOL}	V_{DD} = 2.5V	V_{AOUT} = 0.05V to 2.45V, R_L = 100kΩ		94	125		dB
			V_{AOUT} = 0.2V to 2.3V, R_L = 1kΩ		84	115		
		V_{DD} = 5.5V	V_{AOUT} = 0.05V to 5.4V, R_L = 100kΩ		94	120		
			V_{AOUT} = 0.25V to 5.2V, R_L = 1kΩ		86	106		
Output Voltage Swing	V_{OL} / V_{OH}	$\lvert V_{AIN+} - V_{AIN-} \rvert \geq 10mV$	R_L = 100kΩ	V_{DD} - V_{OH}		1	5	mV
				V_{OL}		1	5	
			R_L = 1kΩ	V_{DD} - V_{OH}		140	250	
				V_{OL}		60	100	
Gain-Bandwidth Product	GBW	MAX9000/MAX9001/MAX9002				1.25		MHz
		MAX9003/MAX9004/MAX9005				8		
Phase Margin		MAX9000/MAX9001/MAX9002				75		degrees
		MAX9003/MAX9004/MAX9005				80		
Gain Margin		MAX9000/MAX9001/MAX9002				30		dB
		MAX9003/MAX9004/MAX9005				40		
Total Harmonic Distortion plus Noise	THD+N	f = 10kHz, V_{AOUT} = 2Vp-p, V_{DD} = 5V	MAX9000/MAX9001/ MAX9002 (A_V = 1V/V)			0.009		%
			MAX9003/MAX9004/ MAX9005 (A_V = 10V/V)			0.028		
Slew Rate	SR	V_{DD} = 5V, V_{AOUT} = 4V step	MAX9000/MAX9001/ MAX9002 (A_V = 1V/V)			0.85		V/µs
			MAX9003/MAX9004/ MAX9005 (A_V = 10V/V)			6.0		
Settling Time to within 0.01%		V_{DD} = 5V, V_{AOUT} = 4V step	MAX9000/MAX9001/ MAX9002 (A_V = 1V/V)			6.9		µs
			MAX9003/MAX9004/ MAX9005 (A_V = 10V/V)			2.1		
Input Capacitance	C_{IN}					2.5		pF
Input Noise Voltage Density	V_{NOISE}	f = 10kHz				36		nV/$\sqrt{Hz}$
Input Noise Current Density	I_{NOISE}	f = 10kHz				1		fA/$\sqrt{Hz}$
Shutdown Delay Time						0.2		µs
Enable Delay Time						2		µs
Power-On Time						2		µs
Capacitive-Load Stability	C_{LOAD}	MAX9000/MAX9001/MAX9002 (A_V = 1V/V)				250		pF
		MAX9003/MAX9004/MAX9005 (A_V = 10V/V)				250		
COMPARATOR								
Input Offset Voltage	V_{OS}	MAX900_ES_ (Notes 1, 2)				±1	±2	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}	MAX900_ES_				±1		µV/°C
Input-Referred Hysteresis		V_{DD} = 5V (Notes 2, 3)				4	7	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.5V to +5.5V, V_{SS} = 0, $\overline{SHDN}$ = V_{DD} (MAX9001/MAX9004 only), $V_{CM(OP\ AMP)}$ = 0, V_{AOUT} = V_{DD} / 2, $V_{CM(COMP)}$ = 0 (for MAX9001/MAX9002/MAX9004/MAX9005), COUT = low, $I_{OUT(REF)}$ = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 5V and T_A = +25°C.)

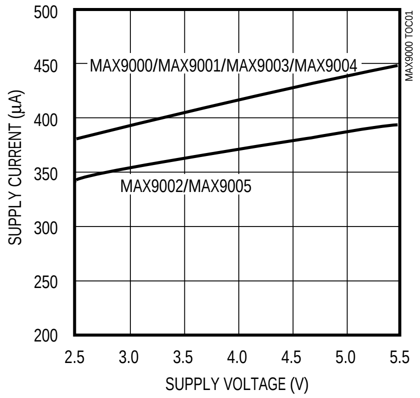
PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Bias Current	I_{BIAS}					8	80	nA
Input Offset Current	I_{OS}	MAX9001/MAX9002/MAX9004/MAX9005				±2	±15	nA
Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test			V_{SS} - 0.15		V_{DD} - 1.1	V
Common-Mode Rejection Ratio	CMRR	MAX9001/MAX9002/MAX9004/MAX9005, 0.15V ≤ V_{CM} ≤ (V_{DD} - 1.1V), V_{DD} = 5.5V			72	100		dB
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.5V to 5.5V			72	100		dB
Output Voltage Swing	V_{OL}/V_{OH}	(V_{CIN+} - V_{CIN-}) ≥ 20mV	V_{DD} - V_{OH}	I_{SOURCE} = 10µA	5			mV
				I_{SOURCE} = 4mA	400			
			V_{OL}	I_{SINK} = 10µA			5	
				I_{SINK} = 4mA			400	
Output Short-Circuit Current						55		mA
Disabled Mode Output Leakage	I_{OUT} (DISABLED)	$V_{\overline{SHDN}}$ ≤ (0.3V x V_{DD}), V_{COUT} = 0 to V_{DD}				±0.01	±1	µA
Propagation Delay	t_{PD+}, t_{PD-}	V_{OD} = 25mV, R_L = 10kΩ, C_L = 15pF (Note 4)				185		ns
Rise/Fall Time	t_R, t_F	V_{DD} = 5V, R_L = 10kΩ, C_L = 15pF (Note 5)				10		ns
Shutdown Delay Time						100		ns
Enable Delay Time						100		ns
Power-On Time						100		ns
VOLTAGE REFERENCE (MAX9000/MAX9001/MAX9003/MAX9004)								
Output Voltage	V_{REF}	MAX900_ES_, V_{DD} = 5V, T_A = +25°C			1.218	1.230	1.242	V
Output Voltage Temperature Coefficient	TCV_{REF}					8		ppm/°C
Line Regulation		V_{DD} = 2.5V to 5.5V				20	250	µV/V
Load Regulation		V_{DD} = 5V, I_{OUT} = 0 to 1mA	Sourcing			0.15	0.8	mV/mA
			Sinking			0.6	2.0	mV/mA
Output Short-Circuit Current		Shorted to V_{SS}				6		mA
		Shorted to V_{DD}				10		
Disabled Mode Output Leakage		$V_{\overline{SHDN}}$ ≤ (0.3V x V_{DD}), V_{REF} = 0 to V_{DD}				±0.01	±1	µA
Output Noise		0.1Hz to 10Hz				20		µVp-p
Shutdown Delay Time						1		µs
Enable Delay Time		R_L = 100kΩ to V_{SS}, V_{REF} within 1%				16		µs
Power-On Time		R_L = 100kΩ to V_{SS}, V_{REF} within 1%				16		µs
Capacitive Load Stability						0 to 100		nF

Note 1: Comparator Input Offset is defined as the center of the input-referred hysteresis zone.
Note 2: Measured at $V_{CM(COMP)}$ = 0 for the MAX9001/MAX9002/MAX9004/MAX9005; or $V_{CM(COMP)}$ = V_{REF} for the MAX9000/MAX9003.
Note 3: Input-referred hysteresis is defined as the difference of the trip points required to change comparator output states.
Note 4: V_{OD} is the overdrive that is beyond the offset and hysteresis-determined trip points.
Note 5: Rise and fall times are measured between 10% and 90% at COUT.

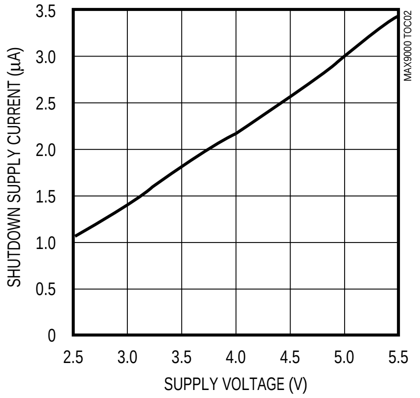
Typical Operating Characteristics

(V_{DD} = +5V, V_{SS} = 0, V_{CM} (op amp) = 0, $\overline{SHDN}$ = V_{DD}, COUT = low, R_L = ∞, T_A = +25°C, unless otherwise noted.)

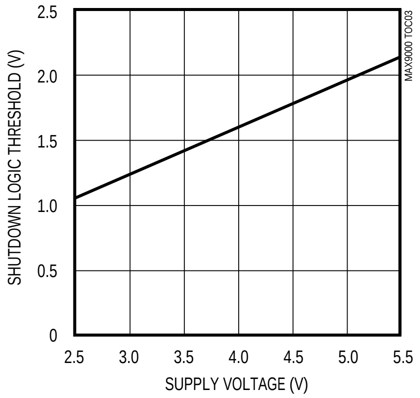
SUPPLY CURRENT vs. SUPPLY VOLTAGE



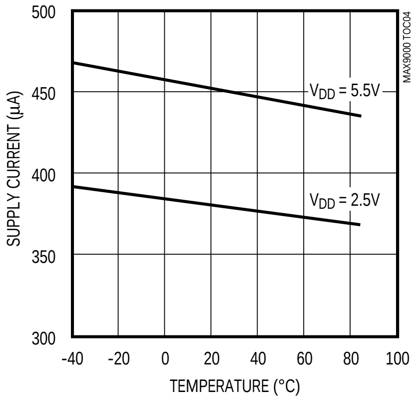
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



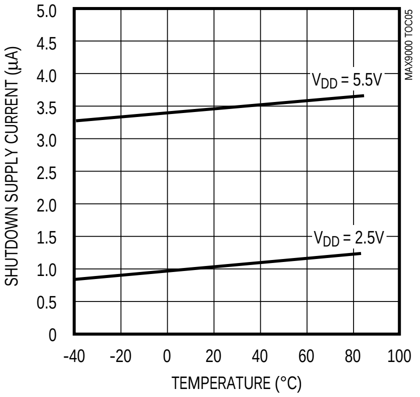
SHUTDOWN LOGIC THRESHOLD vs. SUPPLY VOLTAGE



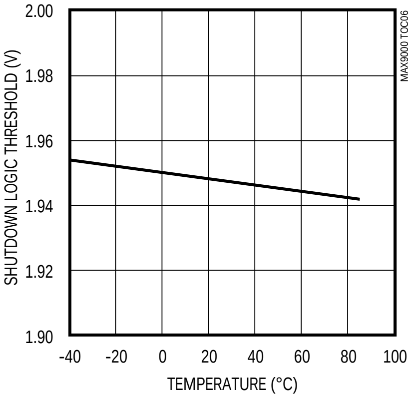
MAX9000/MAX9001/MAX9003/MAX9004 SUPPLY CURRENT vs. TEMPERATURE



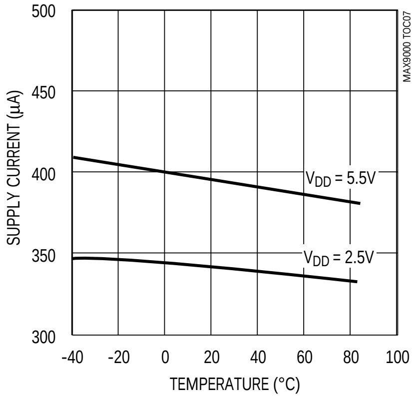
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



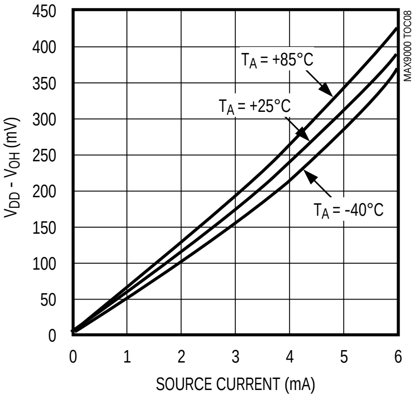
SHUTDOWN LOGIC THRESHOLD vs. TEMPERATURE



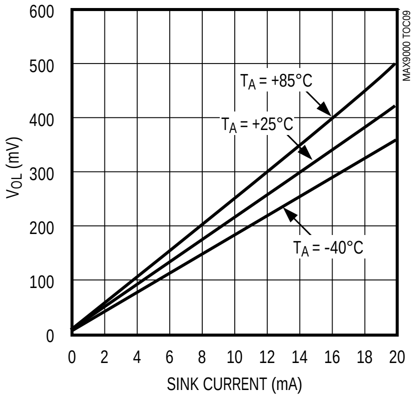
MAX9002/MAX9005 SUPPLY CURRENT vs. TEMPERATURE



OP-AMP OUTPUT VOLTAGE SWING HIGH (V_{OH}) vs. SOURCE CURRENT



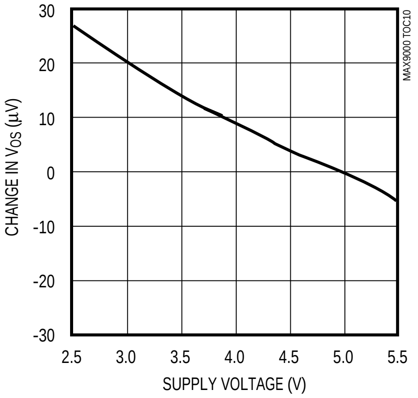
OP-AMP OUTPUT VOLTAGE SWING LOW (V_{OL}) vs. SINK CURRENT



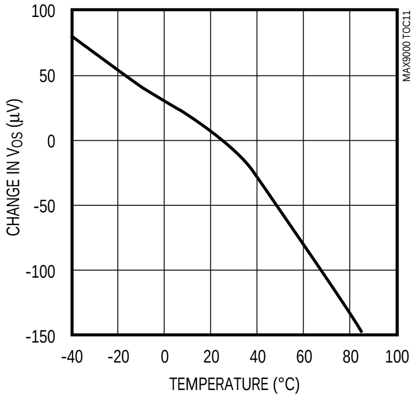
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0, V_{CM} (op amp) = 0, $\overline{SHDN}$ = V_{DD}, COUT = low, R_L = ∞, T_A = +25°C, unless otherwise noted.)

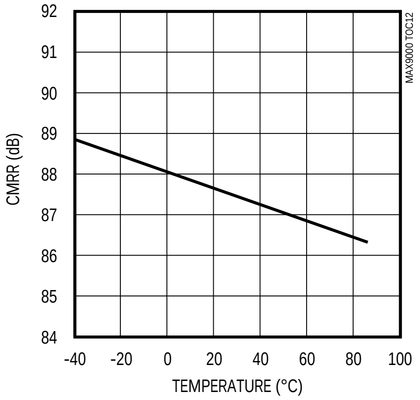
CHANGE IN OP-AMP OFFSET VOLTAGE (V_{OS}) vs. SUPPLY VOLTAGE



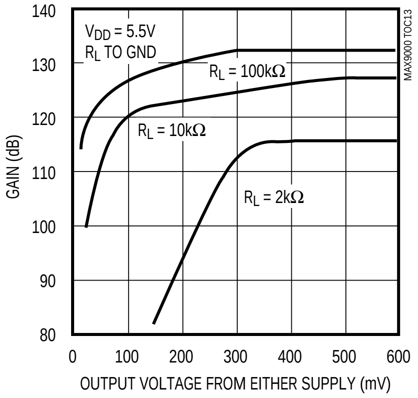
CHANGE IN OP-AMP OFFSET VOLTAGE (V_{OS}) vs. TEMPERATURE



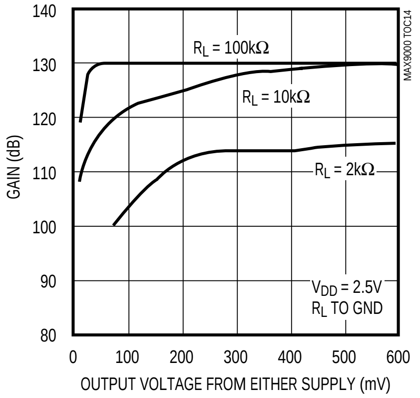
OP-AMP COMMON-MODE REJECTION RATIO vs. TEMPERATURE



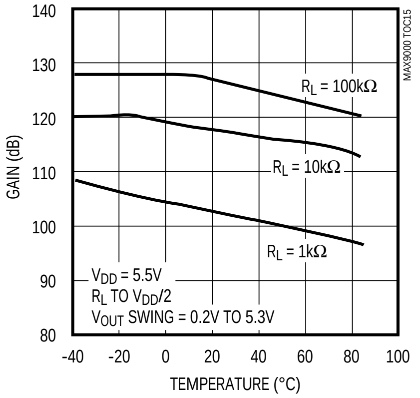
OP-AMP LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



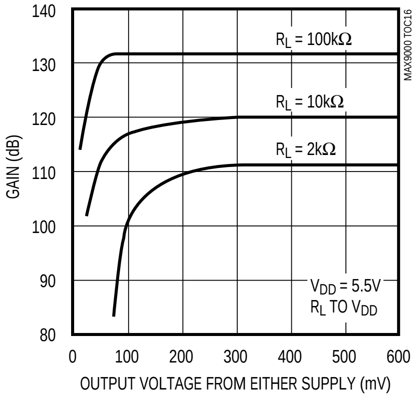
OP-AMP LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



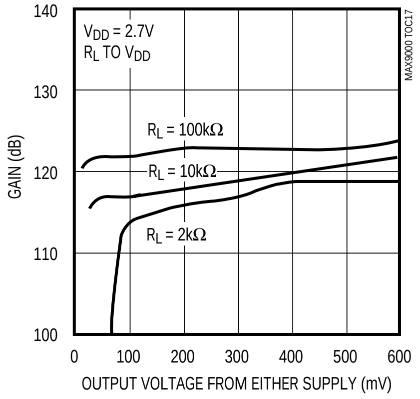
OP-AMP LARGE-SIGNAL GAIN vs. TEMPERATURE



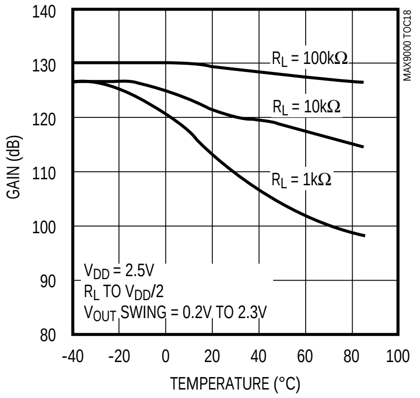
OP-AMP LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



OP-AMP LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



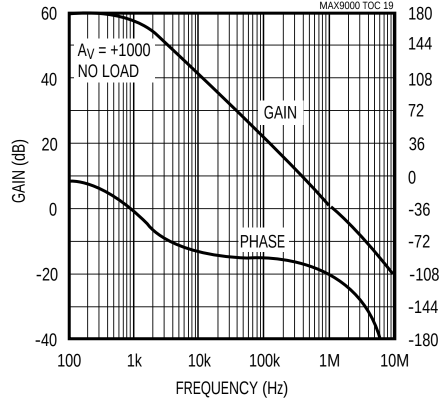
OP-AMP LARGE-SIGNAL GAIN vs. TEMPERATURE



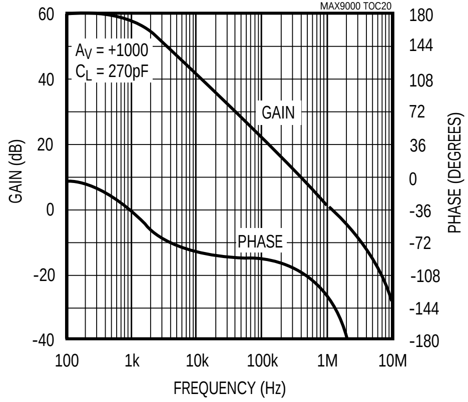
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0, V_{CM} (op amp) = 0, $\overline{SHDN}$ = V_{DD}, COUT = low, R_L = ∞, T_A = +25°C, unless otherwise noted.)

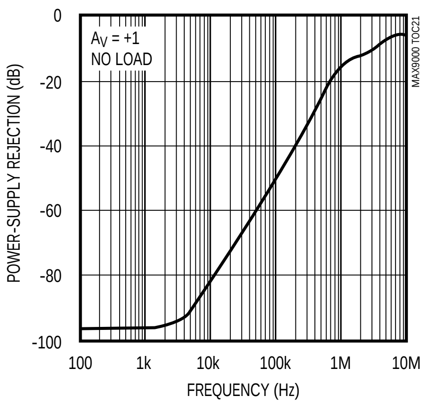
MAX9000/MAX9001/MAX9002
OP-AMP GAIN AND PHASE
vs. FREQUENCY (NO LOAD)



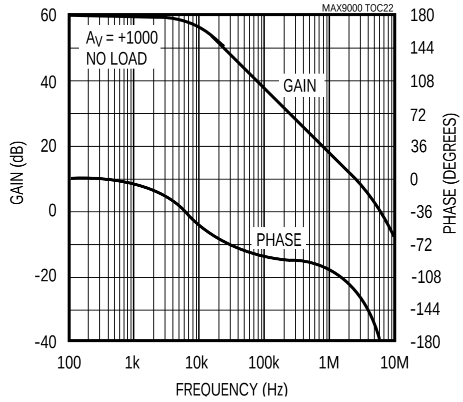
MAX9000/MAX9001/MAX9002
OP-AMP GAIN AND PHASE
vs. FREQUENCY (WITH C_{LOAD})



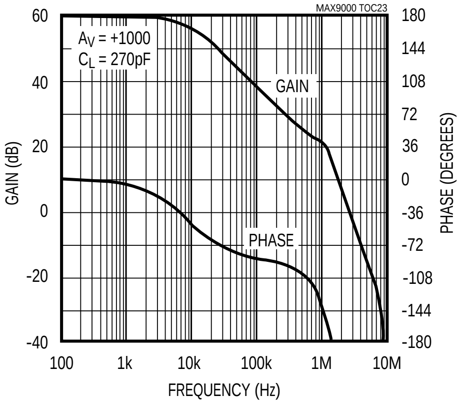
MAX9000/MAX9001/MAX9002
OP-AMP POWER-SUPPLY REJECTION
vs. FREQUENCY



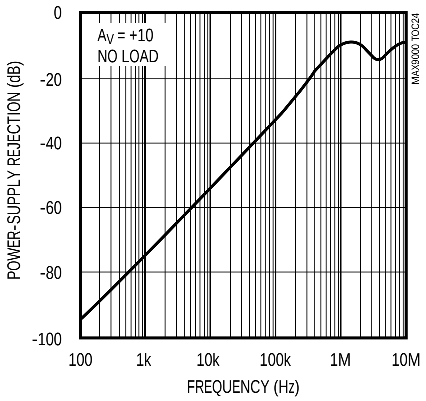
MAX9003/MAX9004/MAX9005
OP-AMP GAIN AND PHASE
vs. FREQUENCY (NO LOAD)



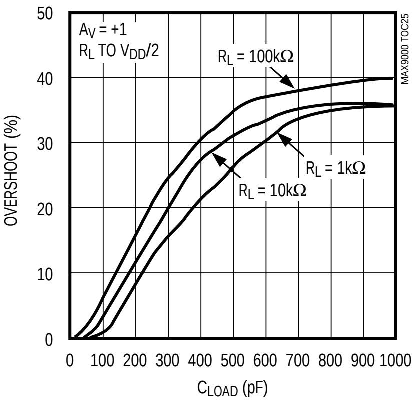
MAX9003/MAX9004/MAX9005
OP-AMP GAIN AND PHASE
vs. FREQUENCY (WITH C_{LOAD})



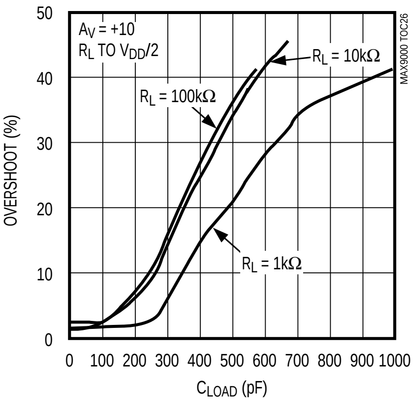
MAX9003/MAX9004/MAX9005
OP-AMP POWER-SUPPLY REJECTION
vs. FREQUENCY



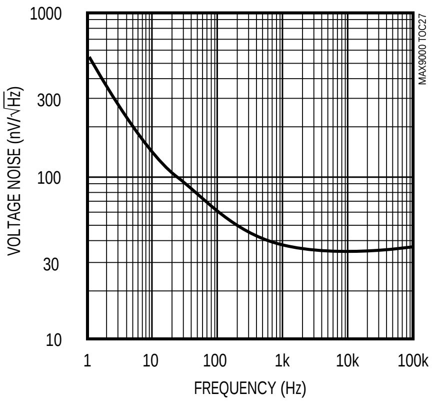
MAX9000/MAX9001/MAX9002
OP-AMP PERCENT OVERSHOOT
vs. LOAD CAPACITANCE



MAX9003/MAX9004/MAX9005
OP-AMP PERCENT OVERSHOOT
vs. LOAD CAPACITANCE



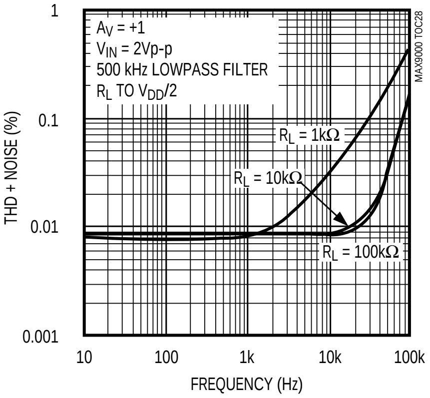
OP-AMP VOLTAGE NOISE DENSITY
vs. FREQUENCY



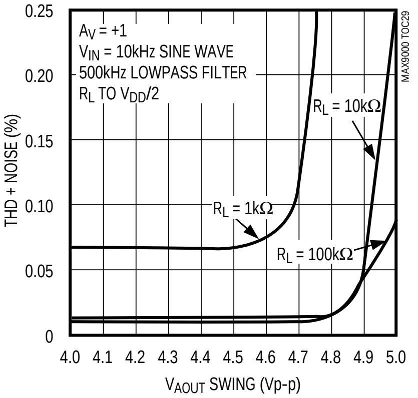
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0, V_{CM} (op amp) = 0, $\overline{SHDN}$ = V_{DD}, COUT = low, R_L = ∞, T_A = +25°C, unless otherwise noted.)

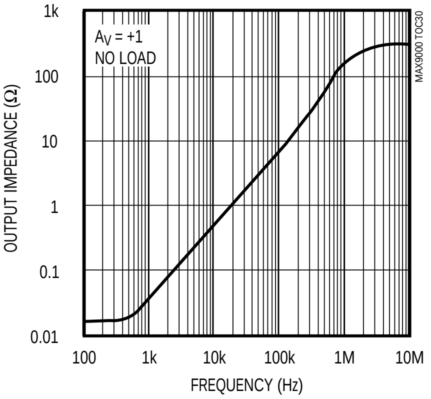
MAX9000/MAX9001/MAX9002 OP-AMP TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



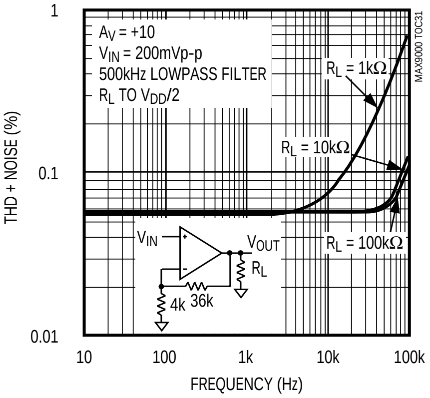
MAX9000/MAX9001/MAX9002 OP-AMP TOTAL HARMONIC DISTORTION PLUS NOISE vs. V_{AOUT}



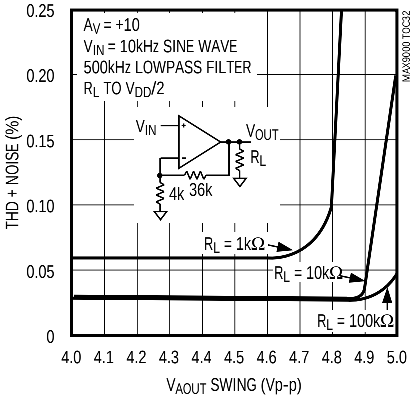
MAX9000/MAX9001/MAX9002 OP-AMP OUTPUT IMPEDANCE vs. FREQUENCY



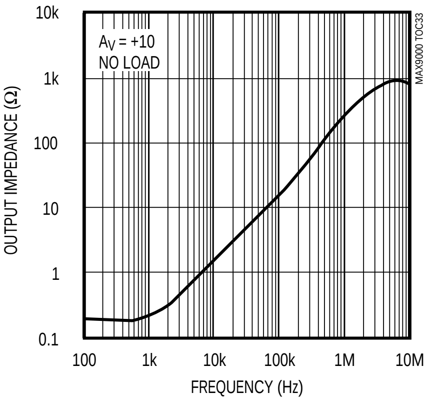
MAX9003/MAX9004/MAX9005 OP-AMP TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



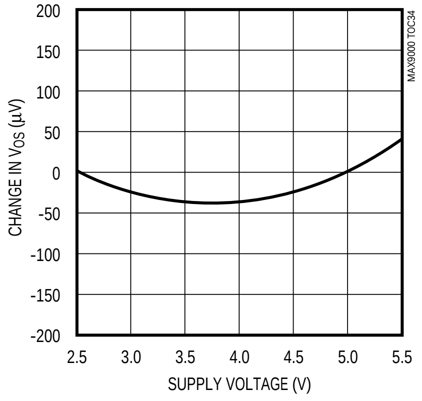
MAX9003/MAX9004/MAX9005 OP-AMP TOTAL HARMONIC DISTORTION PLUS NOISE vs. V_{AOUT}



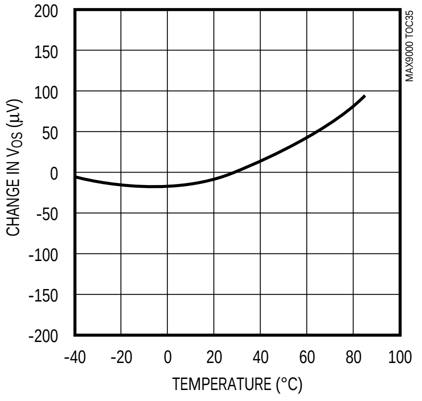
MAX9003/MAX9004/MAX9005 OP-AMP OUTPUT IMPEDANCE vs. FREQUENCY



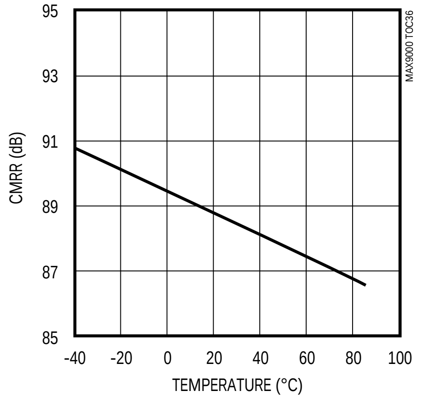
CHANGE IN COMPARATOR OFFSET VOLTAGE (V_{OS}) vs. SUPPLY VOLTAGE



CHANGE IN COMPARATOR OFFSET VOLTAGE (V_{OS}) vs. TEMPERATURE

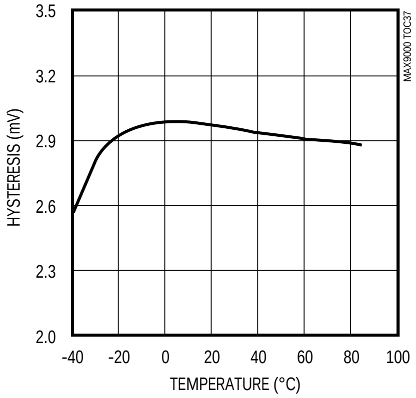


COMPARATOR COMMON-MODE REJECTION RATIO (CMRR) vs. TEMPERATURE

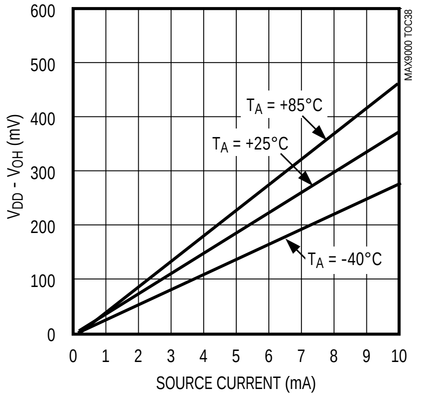


Typical Operating Characteristics (continued)

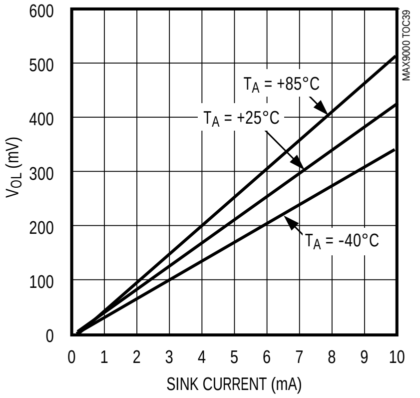
(V_{DD} = +5V, V_{SS} = 0, V_{CM} (op amp) = 0, $\overline{SHDN}$ = V_{DD}, COUT = low, $R_L = \infty$, T_A = +25°C, unless otherwise noted.)



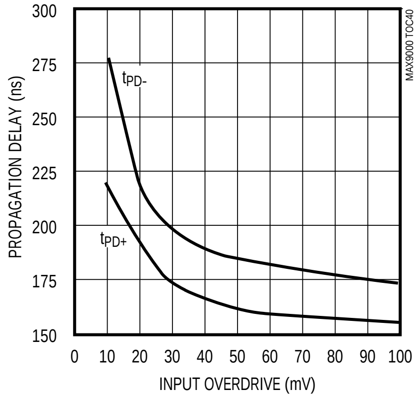
COMPARATOR HYSTERESIS vs. TEMPERATURE



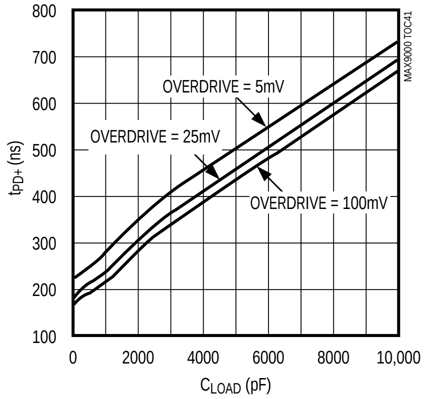
COMPARATOR OUTPUT VOLTAGE SWING HIGH (V_{OH}) vs. SOURCE CURRENT



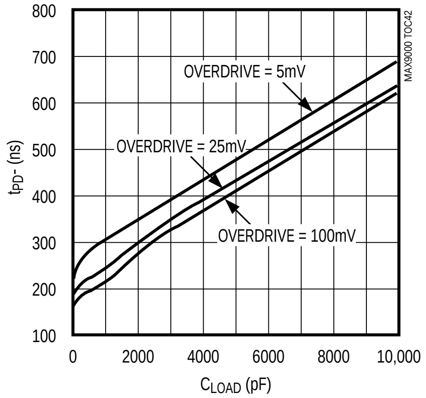
COMPARATOR OUTPUT VOLTAGE SWING LOW (V_{OL}) vs. SINK CURRENT



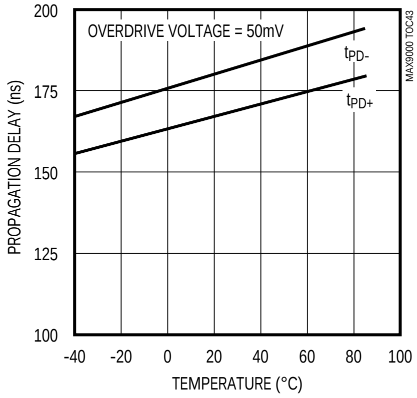
COMPARATOR PROPAGATION DELAY vs. INPUT OVERDRIVE



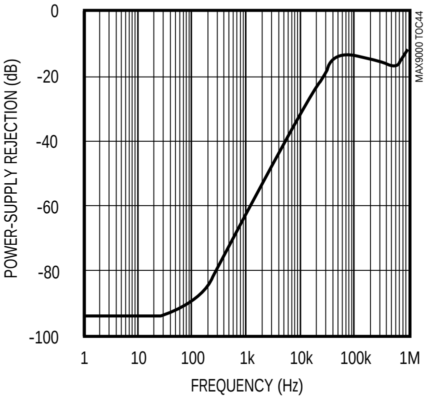
POSITIVE COMPARATOR PROPAGATION DELAY (t_{PD+}) vs. LOAD CAPACITANCE



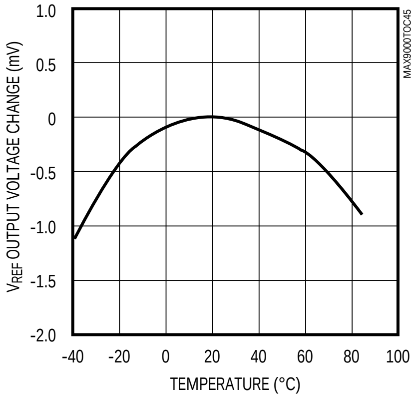
NEGATIVE COMPARATOR PROPAGATION DELAY (t_{PD-}) vs. LOAD CAPACITANCE



COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



V_{REF} POWER-SUPPLY REJECTION vs. FREQUENCY

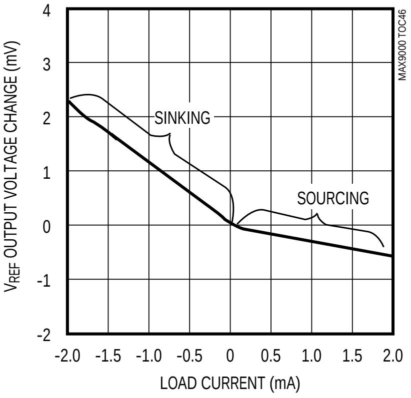


V_{REF} OUTPUT VOLTAGE CHANGE vs. TEMPERATURE

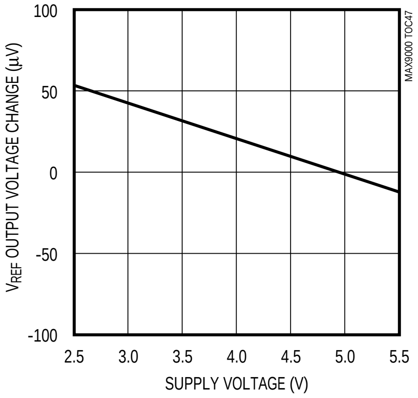
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0, V_{CM} (op amp) = 0, $\overline{SHDN}$ = V_{DD}, COUT = low, $R_L = \infty$, T_A = +25°C, unless otherwise noted.)

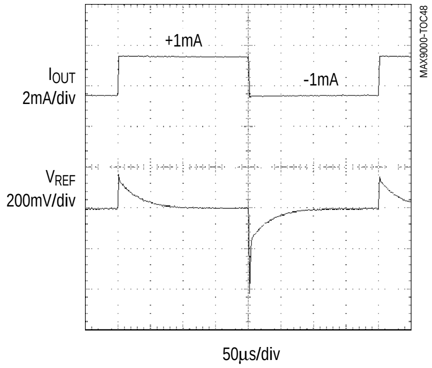
V_{REF} OUTPUT VOLTAGE CHANGE vs. LOAD CURRENT



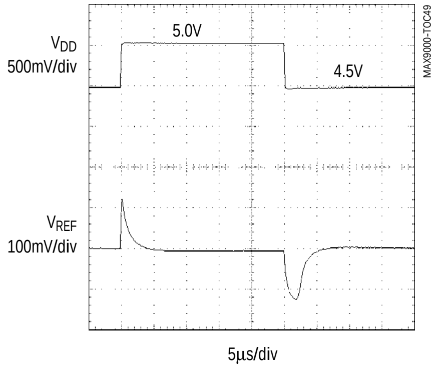
V_{REF} OUTPUT VOLTAGE CHANGE vs. SUPPLY VOLTAGE



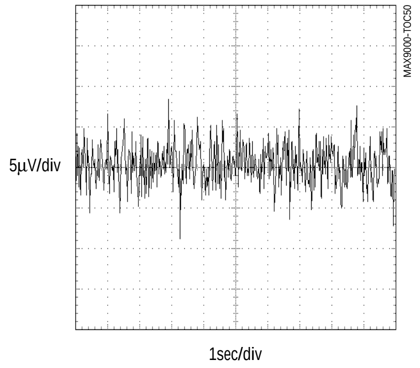
V_{REF} LOAD-TRANSIENT RESPONSE



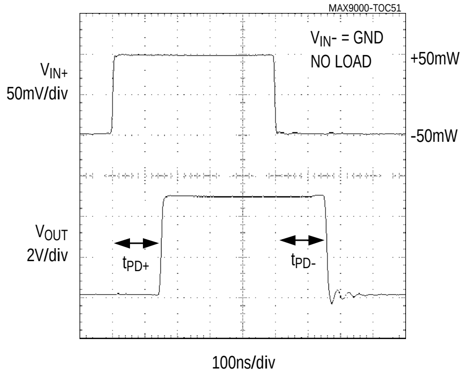
V_{REF} LINE-TRANSIENT RESPONSE



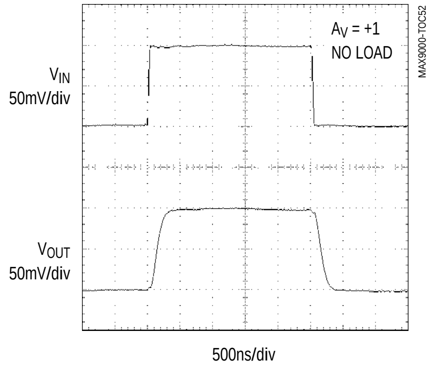
V_{REF} 0.1Hz to 10Hz VOLTAGE NOISE



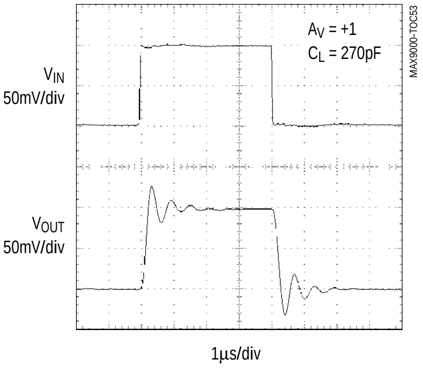
COMPARATOR PROPAGATION DELAY



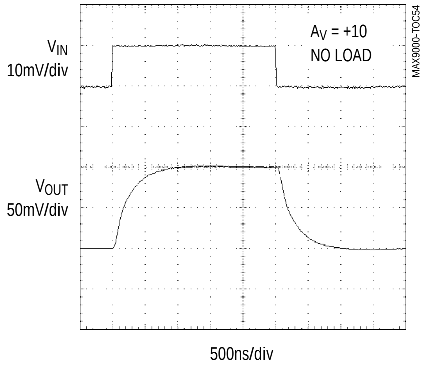
MAX9000/MAX9001/MAX9002 OP-AMP SMALL-SIGNAL TRANSIENT RESPONSE



MAX9000/MAX9001/MAX9002 OP-AMP SMALL-SIGNAL TRANSIENT RESPONSE WITH C_{LOAD}



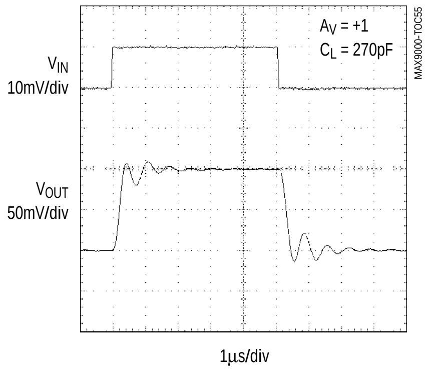
MAX9003/MAX9004/MAX9005 OP-AMP SMALL-SIGNAL TRANSIENT RESPONSE



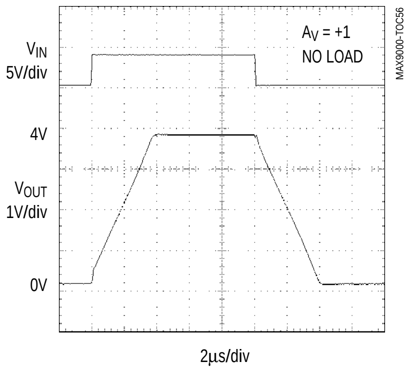
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0, V_{CM} (op amp) = 0, $\overline{SHDN}$ = V_{DD}, COUT = low, R_L = ∞, T_A = +25°C, unless otherwise noted.)

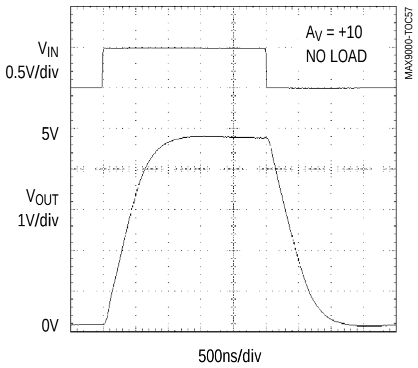
MAX9003/MAX9004/MAX9005 OP-AMP SMALL-SIGNAL TRANSIENT RESPONSE WITH C_{LOAD}



MAX9000/MAX9001/MAX9002 OP-AMP LARGE-SIGNAL TRANSIENT RESPONSE



MAX9003/MAX9004/MAX9005 OP-AMP LARGE-SIGNAL TRANSIENT RESPONSE



Pin Description

PIN				NAME	FUNCTION
MAX9000/ MAX9003	MAX9002/ MAX9005	MAX9001/MAX9004			
		10 µMAX	14 SO		
—	—	1	2	$\overline{SHDN}$	Shutdown Logic Input
1	1	2	3	AOUT	Op-Amp Output
2	2	3	4	AIN-	Inverting Op-Amp Input
3	3	4	5	AIN+	Noninverting Op-Amp Input
4	4	5	6	V_{SS}	Negative Supply or Ground
5	—	6	9	REF	Internal Reference Output
—	5	7	10	CIN-	Inverting Comparator Input
6	6	8	11	CIN+	Noninverting Comparator Input
7	7	9	12	COUT	Comparator Output
8	8	10	13	V_{DD}	Positive Supply
—	—	—	1, 7, 8, 14	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX9001–MAX9005 are combinations of a high-speed operational amplifier, a 185ns comparator, and a 1%-accurate, 8ppm/°C, 1.230V reference. The devices are offered in space-saving 8-pin and 10-pin µMAX packages. The comparator's inverting input is internally connected to the reference output in the MAX9000/MAX9003. The MAX9002/MAX9005 do not have an internal reference, but the inverting input of the comparator is available externally. The MAX9001/MAX9004 include both the inverting input and the reference output. The MAX9000/MAX9001/MAX9003/MAX9004 typically consume only 410µA of quiescent current, while the MAX9002/MAX9004 typically consume 340µA. These low-power, Rail-to-Rail devices provide excellent AC and DC performance and are ideally suited to operate from a single supply. The MAX9001/MAX9004 feature a shutdown mode that sets the outputs in a high-impedance state and reduces the supply current to 2µA, making these devices ideal for portable and battery-powered systems.

Op Amp

The op amps in the MAX9000/MAX9001/MAX9002 are unity-gain stable with a gain-bandwidth product of 1.25MHz and a slew rate of 0.85V/µs. The amplifiers in the MAX9003/MAX9004/MAX9005 are stable at closed-loop gains greater than or equal to 10V/V, with a gain-bandwidth product of 8MHz and a slew rate of 6.0V/µs.

The common-mode input voltage range extends from 150mV below the negative rail to within 1.2V of the positive rail. The amplifier output does not undergo phase reversal when the common-mode input range is exceeded, and the input impedance is relatively constant for input voltages within both supply rails. The MOS differential inputs of the amplifiers feature extremely high input impedance and ultra-low input bias currents. The CMOS output stage achieves true rail-to-rail operation; the outputs swing to within a few millivolts of the supply rails, thus extending the dynamic range. A proprietary design achieves high open-loop gain, enabling these devices to operate at low quiescent currents yet maintain excellent DC and AC characteristics under various load conditions. These devices have been designed to maintain low offset voltage over the entire operating-temperature, common-mode, and supply-voltage ranges.

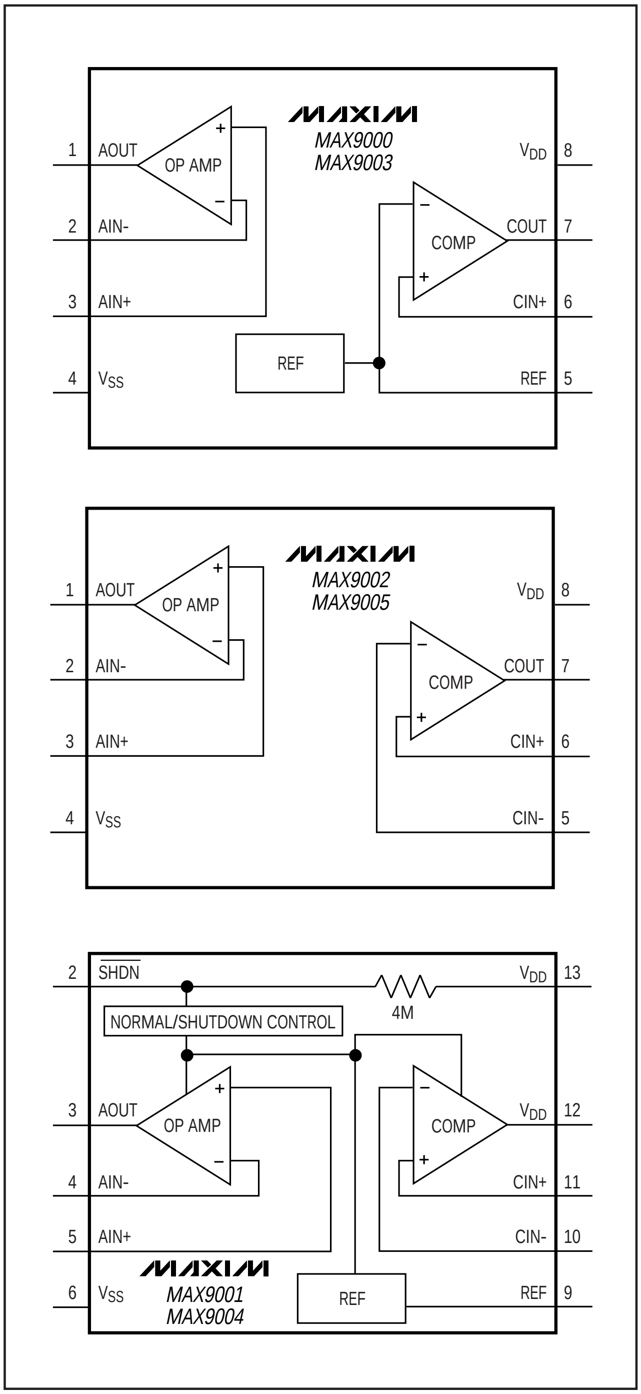


Figure 1. MAX9000–MAX90005 Functional Diagrams

Comparator

The common-mode input range extends from 150mV below the negative rail to within 1.1V of the positive rail. The bipolar differential inputs of the comparator feature high input impedance and low input bias currents. The comparators are designed to maintain low offset voltage over the entire operating-temperature, common-mode, and supply-voltage ranges. In the MAX9000/MAX9003, the comparator's inverting input is internally connected to the reference output.

The CMOS output stage achieves true rail-to-rail operation; the outputs swing to within a few millivolts of the supply rails. The comparator's propagation delay is 185ns and is a function of the overdrive (see *Typical Operating Characteristics*). TTL/CMOS compatibility is maintained even with a ±4mA output load. A proprietary design of the output stage substantially reduces the cross-conduction current during output transitions, thereby minimizing power-supply glitches typical of most comparators. In addition, the comparator's ±2mV of built-in hysteresis provides noise immunity and prevents unstable outputs even with slow-moving input signals.

Voltage Reference

The 1%-accurate, precision 1.230V internal bandgap reference in the MAX9000/MAX9001/MAX9003/MAX9004 achieves an 8ppm/°C temperature coefficient (tempco). The reference can sink or source 1mA of load current with excellent load regulation. The output typically changes only 60µV for a 3V change in input voltage (line regulation). The reference is stable for capacitive loads up to 100nF.

Applications Information

The MAX9000–MAX9005 offer excellent performance and low power consumption, and are available in space-saving µMAX packages. The following section provides some practical application guidelines.

Bypassing and Layout

The MAX9000–MAX9005 operate from a +2.5V to +5.5V single supply or from ±1.25V to ±2.75V dual supplies. (In the MAX9000/MAX9001/MAX9003/MAX9004, the reference voltage is referred to as V_{SS}.). For single-supply operation, bypass the power supply with a 0.1µF capacitor. For dual supplies, bypass each supply to ground. Bypass with capacitors as close as possible to the device to minimize lead inductance and noise. Use a low-inductance ground plane if possible. A printed circuit board with a ground plane is recommended. Avoid using wire-wrap boards, breadboards, or IC sockets. For heavy loads at the comparator's and/or amplifier's output, add a 1µF to 10µF power-supply bypass capacitor.

The device has a high degree of isolation between the various blocks. To maintain isolation, careful layout is required. Take special precautions to avoid crossing signal traces, especially from the outputs to the inputs. For sensitive applications, shielding might be required. In addition, stray capacitance may affect the stability and frequency response of the amplifier. Decrease stray capacitance by minimizing lead lengths in the board layout, as well as placing external components as close to the device as possible.

Op-Amp Frequency Stability

Driving large capacitive loads can cause instability in most low-power, rail-to-rail output amplifiers. These amplifiers are stable with capacitive loads up to 250pF in their minimum gain configuration. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op-amp output, as shown in Figure 2. This resistor improves the circuit's phase margin by isolating the load capacitor from the amplifier's output. Figures 3 and 4 show the response of the amplifier with and without an isolation resistor, respectively.

The total capacitance at the op amp's inputs (input capacitance + stray capacitance) along with large-value feedback resistors can cause additional poles within the amplifier's bandwidth, thus degrading the phase margin. To compensate for this effect, place a 2pF to 10pF capacitor across the feedback resistor, as shown in Figure 5.

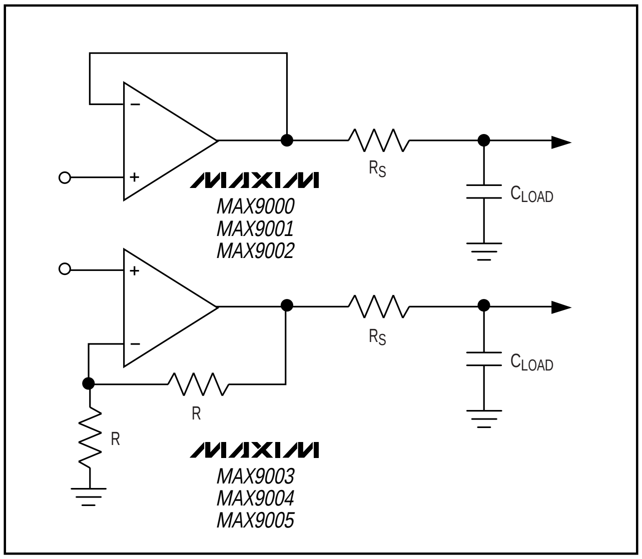


Figure 2. Isolation Resistors to Drive Capacitive Loads

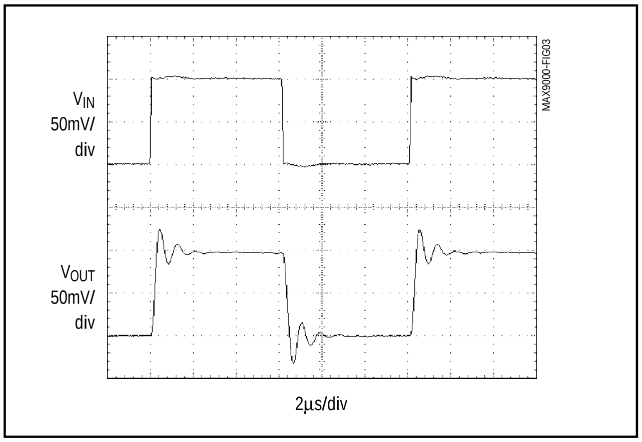


Figure 3. MAX9000/MAX9001/MAX9002 Op-Amp Small-Signal Transient Response with Capacitive Load (C_L = 510pF) and Isolation Resistor (R_{ISO} = 91Ω)

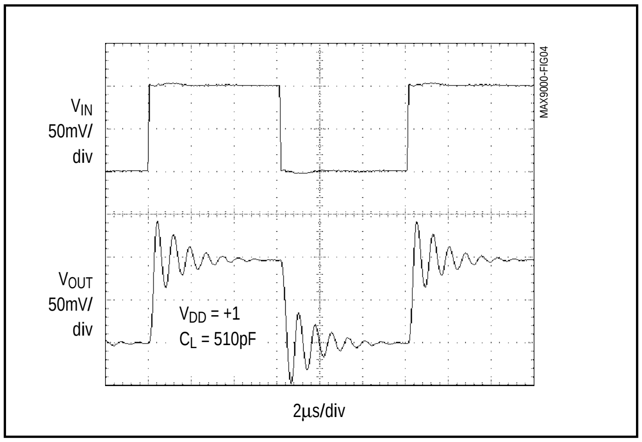


Figure 4. MAX9000/MAX9001/MAX9002 Op-Amp Small-Signal Transient Response with Capacitive Load (C_L = 510pF) and No Isolation Resistor

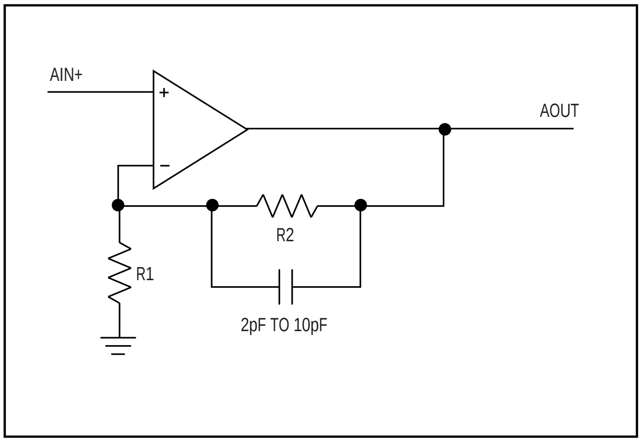


Figure 5. Compensation for Input Capacitance

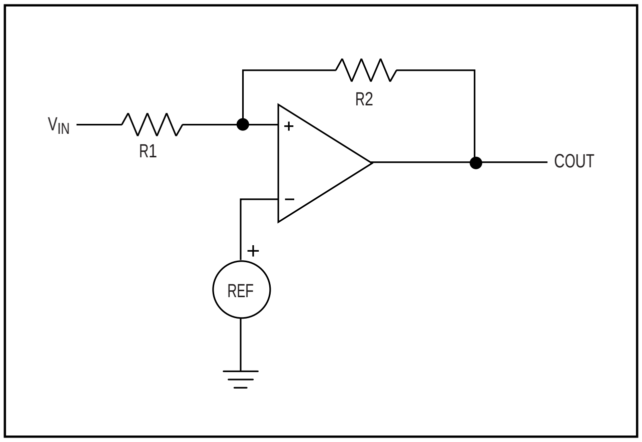


Figure 6. External Hysteresis

Reference Bypassing

While the internal reference is stable with capacitive loads up to 100nF, it does not require an output capacitor for stability. However, in applications where the load or the supply could experience large step changes, an output capacitor reduces the amount of overshoot and improves the circuit's transient response.

Comparator Input Stage

The comparator's input bias current is typically 8nA. To reduce the offset error caused by the bias current flowing through the external source impedance, match the effective impedance seen by each input. High source impedance together with the comparator's input capacitance can increase the propagation delay through the comparator. The outputs do not undergo phase reversal when the input common-mode range is exceeded, and the input impedance is relatively constant for input voltages within both supply rails.

Comparator Hysteresis

Built-in ±2mV hysteresis improves the comparator's noise immunity. It prevents unstable outputs with slow-moving or noisy input signals. If additional hysteresis is required, add positive feedback as shown in Figure 6. This configuration increases the hysteresis band to desired levels, but also increases power consumption and slows down the output response.

To add hysteresis, use the following procedure:

Step 1: The device's input bias current can be as high as 80nA. To minimize error due to the input bias, choose a value for R2 of 100kΩ (V_{REF} / R2), which allows a current of 12.33µA at the upper trip point.

Step 2: Choose the width of the hysteresis band. In this example, choose 20mV for the added external hysteresis (V_{EHYST} = 20mV). Total hysteresis = V_{EHYST} + V_{IHYST} = 24mV.

$$R1 = R2 (V_{EHYST} - 2V_{IHYST}) / (V_{DD} + 2V_{IHYST})$$

where ${}_{IHYST}$ is the device's internal hysteresis.

Step 3: Determine R1. If V_{DD} = 5V, then R1 = 319Ω.

Step 4: Check the hysteresis trip points. The following equation represents the upper trip point ($V_{IN(H)}$):

$$V_{IN(H)} = [(R1 + R2) / R2] (V_{REF} + V_{IHYST}) = 1.238V$$

The lower trip point is 24mV lower than upper trip point. $V_{IN(L)}$ = 1.238V - 0.024V = 1.214V.

Comparator Propagation Delay

The comparator's propagation delay is a function of the input overdrive voltage. Overdrive voltage is measured from beyond the edge of the offset and hysteresis-determined trip points (see *Typical Operating Characteristics* for a graph of Propagation Delay vs. Input Overdrive). High source impedance coupled with the comparator's input capacitance increases the propagation delay. Large capacitive loads also increase the propagation delay.

Shutdown ($\overline{SHDN}$)

Shutdown is active-low enabled. The $\overline{SHDN}$ input for the MAX9001/MAX9004 can be taken above the positive supply without an increase in the $\overline{SHDN}$ input current, allowing them to be driven from independent logic circuits powered from a different supply voltage. However, the logic threshold voltage requirements must be met for proper operation. If $\overline{SHDN}$ is left unconnected, the device defaults to the enabled mode through an internal 4MΩ pull-up to V_{DD}. If $\overline{SHDN}$ is to be left unconnected, take proper care to ensure that no signals are coupled to this pin, as this may cause false triggering.

In shutdown mode, all outputs are set to a high-impedance state and the supply current reduces to 2µA. Enable times for the op amp, comparator, and reference are 2µs, 100ns, and 16µs, respectively. Shutdown delay times for the op amp, comparator, and reference are 200ns, 100ns, and 1µs, respectively (Figure 7).

Application Circuits

Radio Receiver for Alarms and Detectors

Figure 8's circuit is useful as a front end for RF alarms. An unshielded inductor is used with capacitors C1A, C1B, and C1C in a resonant circuit to provide frequency selectivity. The op amp from a MAX9003 amplifies the signal received. The comparator improves noise immunity, provides a signal-strength threshold, and translates the received signal into a pulse train. The tuned LC circuit in Figure 8 is set for 300kHz. The layout and routing of components for the amplifier should be tight to minimize 60Hz interference and crosstalk from the comparator. Metal shielding is recommended to prevent RFI from the comparator or digital circuitry from exciting the receiving antenna. The transmitting

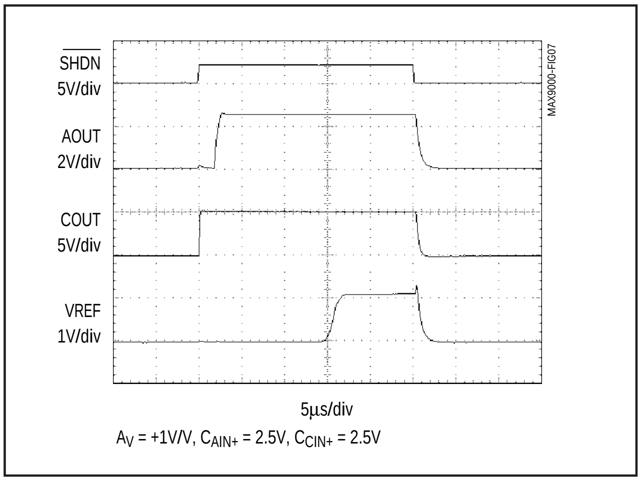


Figure 7. Enable/Disable Response of Op Amp, Comparator, and Reference to $\overline{SHDN}$

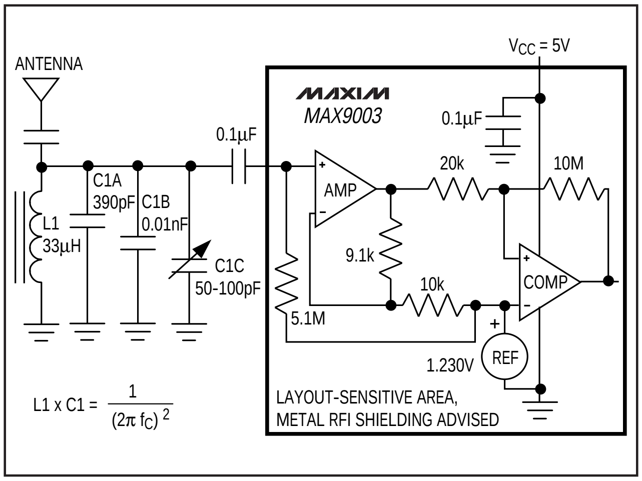


Figure 8. Radio Receiver Application

antenna can be long parallel wires spaced about 7.2cm apart, with equal but opposite currents. Radio waves from this antenna are detectable when the receiver is brought within close proximity, but cancel out at greater distances.

Infrared Receiver Front End for Remote Controls and Data Links

The circuit in Figure 9 uses the MAX9003 as a PIN photodiode preamplifier and discriminator for an infrared receiver. The op amp is configured as a Delyiannis-noise and eliminates low-frequency interference from sunlight, fluorescent lights, etc. This circuit is applicable for TV remote controls and low-frequency data links up to 200kbps. Carrier frequencies are limited to around 100kHz, as in the example circuit. Component layout and routing for the amplifier should be tight to reduce stray capacitance, 60Hz interference, and RFI from the comparator. Crosstalk from comparator edges distorts the amplifier signal. To minimize this effect, add a lowpass RC filter to the connection from the reference to the op amp's noninverting input.

Signal Conditioning

For incoming signals that require filtering, the internal amplifier provides an opportunity to create an active filter. This may be required for relatively high-speed signals that require adequate filtering of high-speed carrier frequencies, harmonics, and external noise. In addition, the amplifier can be used to amplify the signal prior to digitizing it through the comparator to improve the comparator's overall output response and improve its noise immunity.

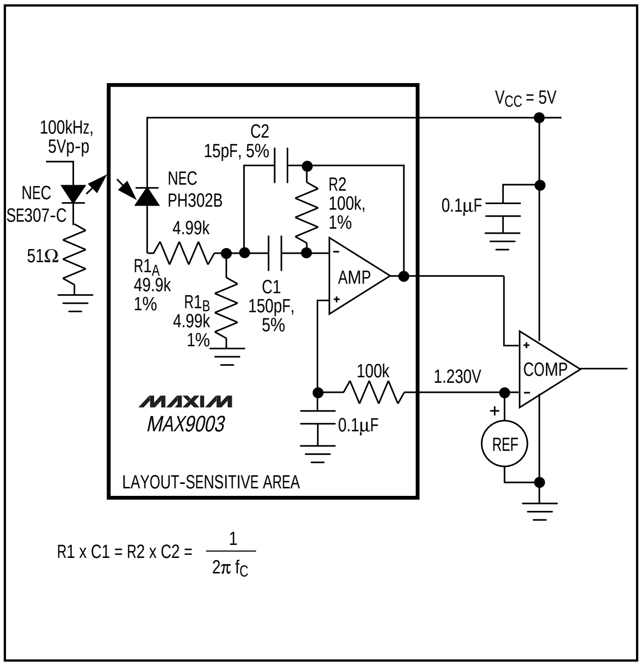
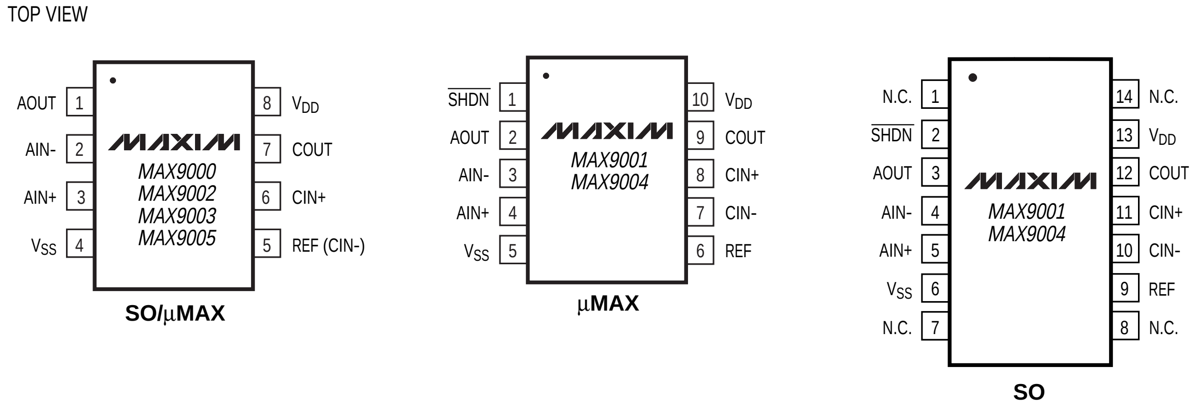


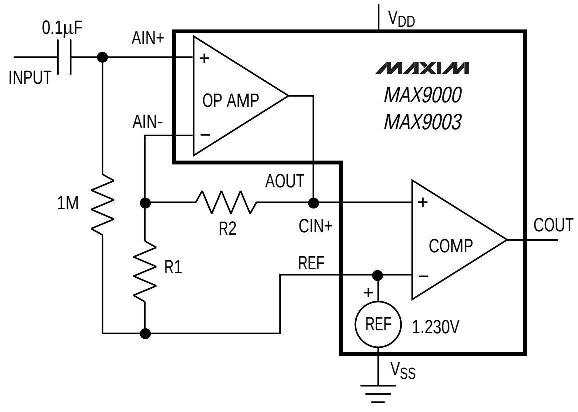
Figure 9. Infrared Receiver Application

Pin Configurations



( ) ARE FOR THE MAX9002/MAX9005.

Typical Operating Circuit



Low-Power, High-Speed, Single-Supply Op Amp + Comparator + Reference ICs

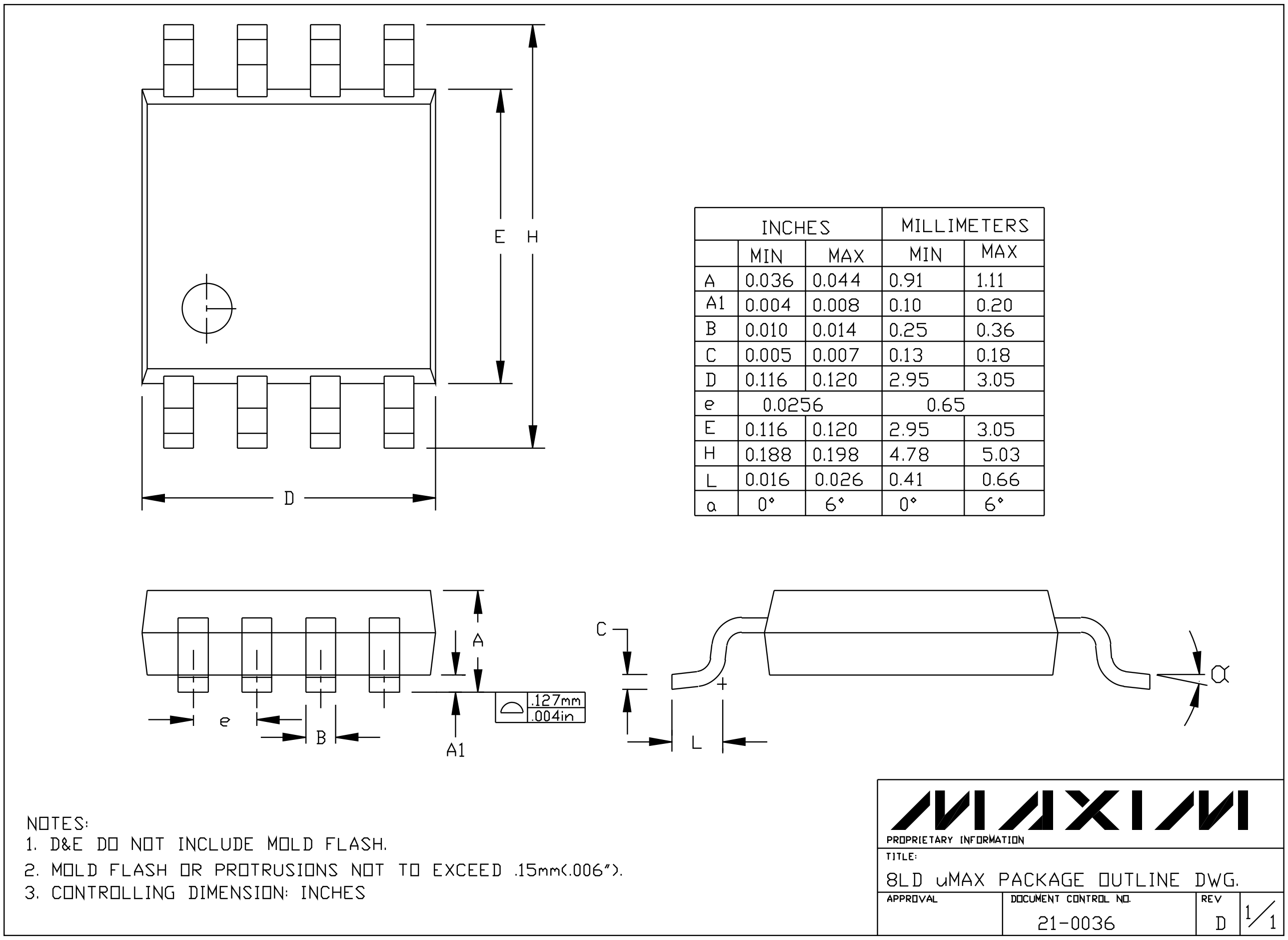
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX9002EUA	-40°C to +85°C	8 µMAX
MAX9002ESA	-40°C to +85°C	8 SO
MAX9003EUA	-40°C to +85°C	8 µMAX
MAX9003ESA	-40°C to +85°C	8 SO
MAX9004EUB	-40°C to +85°C	10 µMAX
MAX9004ESD	-40°C to +85°C	14 SO
MAX9005EUA	-40°C to +85°C	8 µMAX
MAX9005ESA	-40°C to +85°C	8 SO

Chip Information

TRANSISTOR COUNT: 283

Package Information

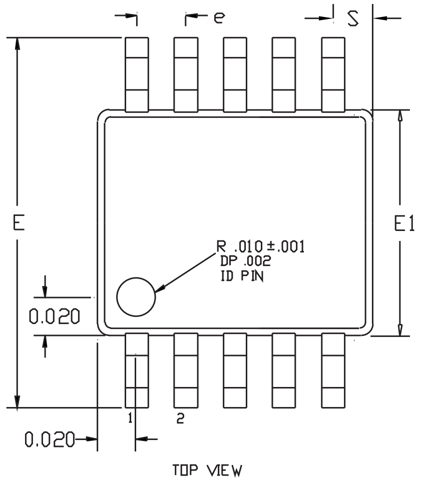


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

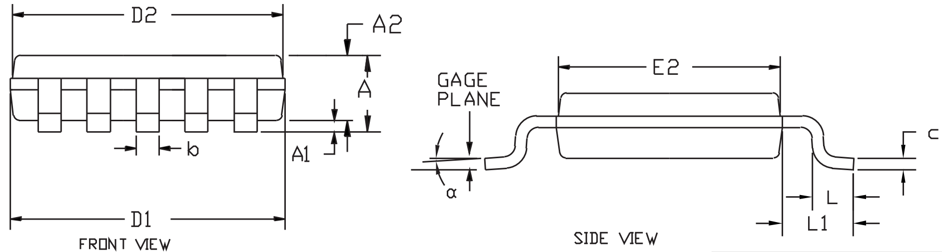
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

Package Information (continued)

10LUMAXB.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.037	0.043	0.939	1.092
A1	0.002	0.006	0.051	0.152
A2	0.030	0.038	0.762	0.965
D1	0.112	0.124	2.845	3.150
D2	0.110	0.122	2.794	3.099
E1	0.112	0.124	2.845	3.150
E2	0.110	0.122	2.794	3.099
E	0.185	0.201	4.699	5.105
L	0.0155	0.0275	0.394	0.699
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		.498 REF	
α	0°	6°	0°	6°

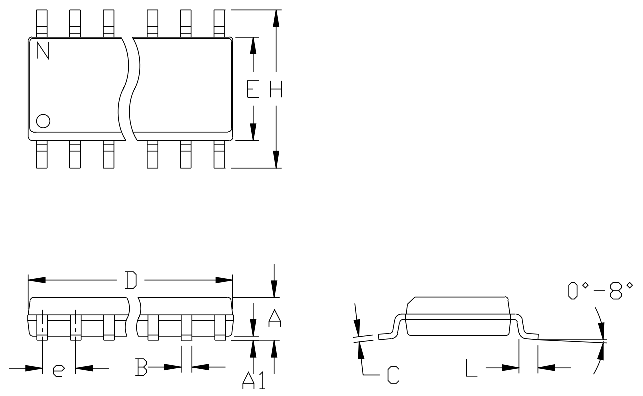


NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 10L MICRO MAX

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0061	B	1/1

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT
   TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN
   .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN
   IN ABOVE TABLE
6. N = NUMBER OF PINS

120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150"
TITLE

1/1

21-0041 A
DOCUMENT CONTROL NUMBER REV

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