

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4520B **MSI** Dual binary counter

Product specification
File under Integrated Circuits, IC04

January 1995

Dual binary counter

HEF4520B

MSI

DESCRIPTION

The HEF4520B is a dual 4-bit internally synchronous binary counter. The counter has an active HIGH clock input (CP₀) and an active LOW clock input ($\overline{\text{CP}}_1$), buffered outputs from all four bit positions (O₀ to O₃) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP₀ input if $\overline{\text{CP}}_1$ is HIGH or the HIGH to

LOW transition of the $\overline{\text{CP}}_1$ input if CP₀ is low. Either CP₀ or $\overline{\text{CP}}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O₀ to O₃ = LOW) independent of CP₀, $\overline{\text{CP}}_1$. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

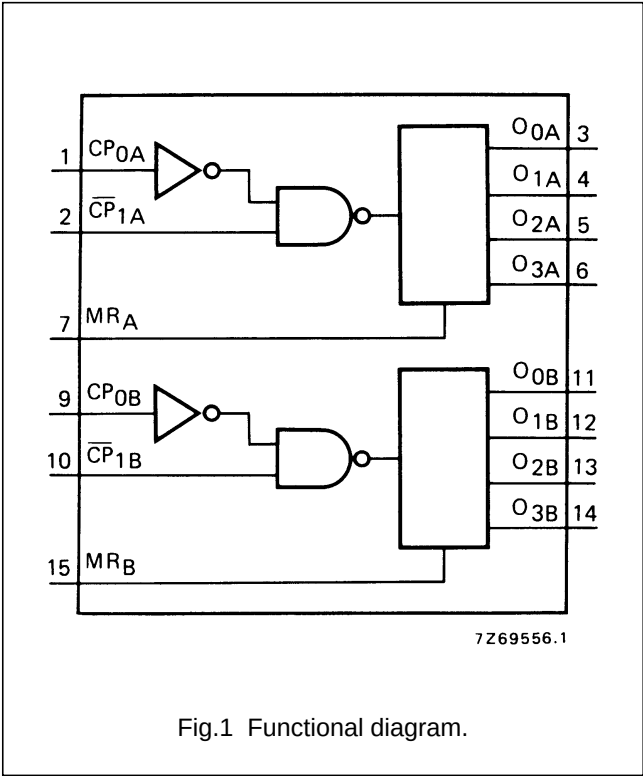


Fig.1 Functional diagram.

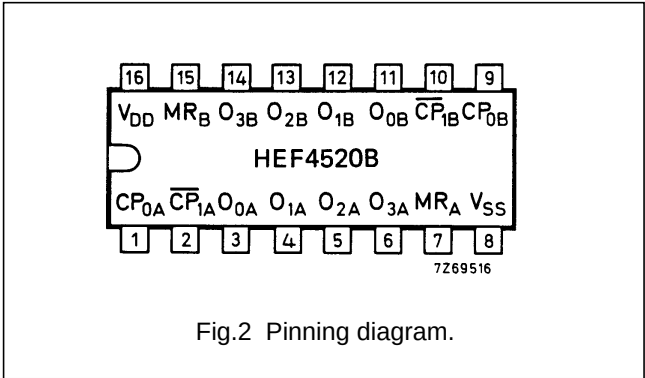


Fig.2 Pinning diagram.

- HEF4520BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4520BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4520BT(D): 16-lead SO; plastic (SOT109-1) (SOT109-1)
(): Package Designator North America

PINNING

- CP_{0A}, CP_{0B} clock inputs (L to H triggered)
 $\overline{\text{CP}}_{1A}$, $\overline{\text{CP}}_{1B}$ clock inputs (H to L triggered)
MR_A, MR_B master reset inputs
O_{0A} to O_{3A} outputs
O_{0B} to O_{3B} outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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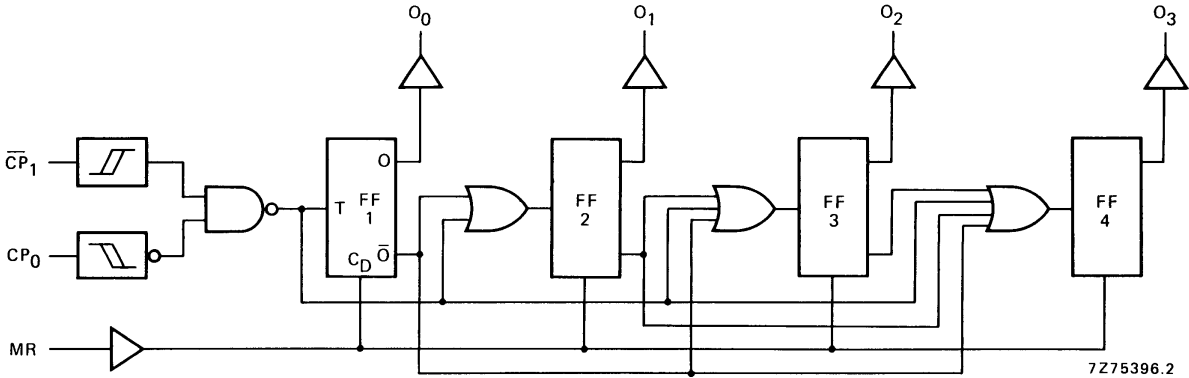


Fig.3 Logic diagram (one counter).

FUNCTION TABLE

CP ₀	$\overline{\text{CP}}_1$	MR	MODE
	H	L	counter advances
L		L	counter advances
	X	L	no change
X		L	no change
	L	L	no change
H		L	no change
X	X	H	O ₀ to O ₃ = LOW

Notes

1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
 = positive-going transition
 = negative-going transition

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AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $CP_0, \overline{CP}_1 \rightarrow O_n$ HIGH to LOW LOW to HIGH MR $\rightarrow O_n$ HIGH to LOW	5	t_{PHL}	110	220	ns	83 ns + (0,55 ns/pF) C_L
	10		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
	5	t_{PLH}	110	220	ns	83 ns + (0,55 ns/pF) C_L
	10		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
	5	t_{PHL}	75	150	ns	48 ns + (0,55 ns/pF) C_L
	10		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW LOW to HIGH	5	t_{THL}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum CP_0 pulse width; LOW	5 10 15	t_{WCPL}	60 30 20	30 15 10	ns ns ns	see also waveforms Figs 4 and 5
Minimum $\overline{CP}_1$ pulse width; HIGH	5 10 15	t_{WCPH}	60 30 20	30 15 10	ns ns ns	
Minimum MR pulse width; HIGH	5 10 15	t_{WMRH}	30 20 16	15 10 8	ns ns ns	
Recovery time for MR	5 10 15	t_{RMR}	50 30 20	25 15 10	ns ns ns	
Set-up times $CP_0 \rightarrow \overline{CP}_1$	5 10 15	t_{su}	50 30 20	25 15 10	ns ns ns	
$\overline{CP}_1 \rightarrow CP_0$	5 10 15	t_{su}	50 30 20	25 15 10	ns ns ns	
Maximum clock pulse frequency	5 10 15	f_{max}	8 15 20	16 30 40	MHz MHz MHz	

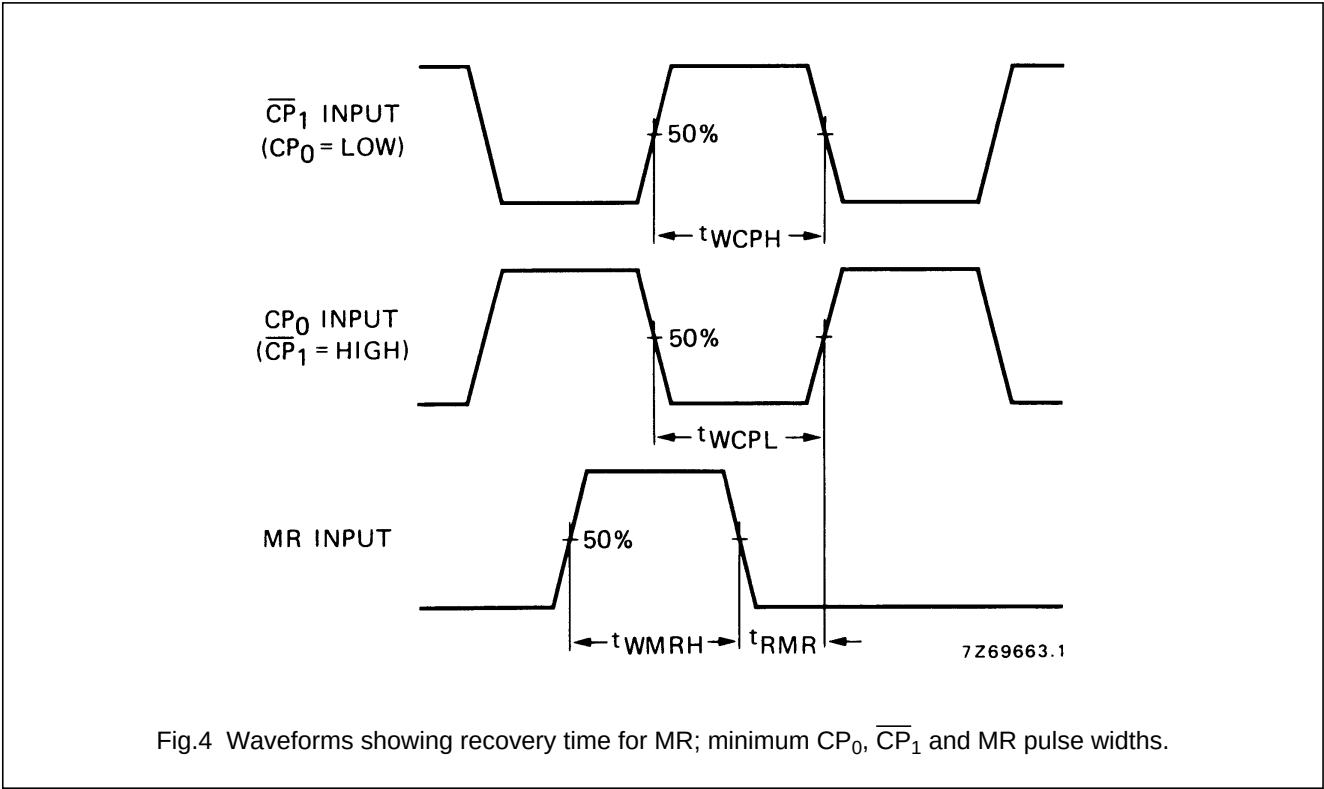
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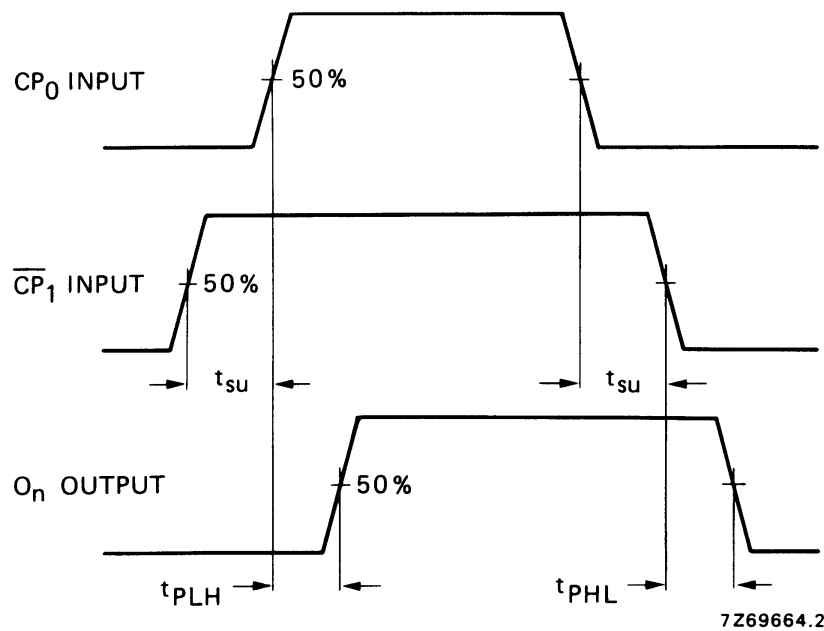
AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	850 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	3 800 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	10 200 f _i + ∑ (f _o C _L) × V _{DD} ²	



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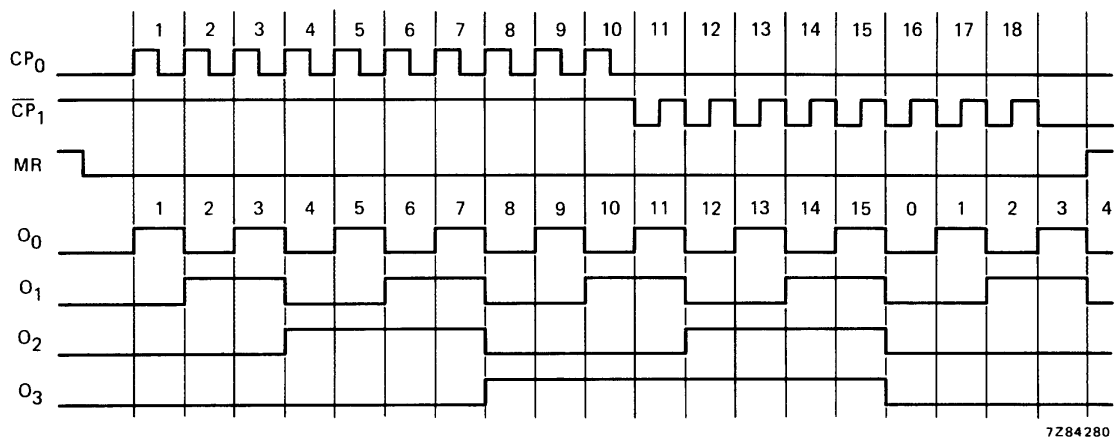


Fig.6 Timing diagram.



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