Features

- **EE Programmable 65,536 x 1-, 131,072 x 1-, 262,144 x 1-, 524,288 x 1-, 1,048,576 x 1- and 2,097,152 x 1-bit Serial Memories Designed to Store Configuration Programs for Altera® FLEX® and APEX™ FPGAs (Device Selection Guide Included)**
- **Available as a 3.3V (±10%) and 5.0V (±5% Commercial, ±10% Industrial) Version**
- **In-System Programmable (ISP) via 2-wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with Atmel AT6000, AT40K and AT94K Devices, Altera FLEX, APEX Devices, ORCA® FPGAs, Xilinx® XC3000, XC4000, XC5200, Spartan®, Virtex™ FPGAs, Motorola MPA1000 FPGAs**
- **Cascadable Read-back to Support Additional Configurations or Higher-density Arrays**
- **Very Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available 8-lead PDIP, 20-lead PLCC and 32-lead TQFP Packages (Pin Compatible Across Product Family)**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Low-power Standby Mode**
- **High-reliability**
  - **Endurance: 100,000 Write Cycles**
  - **Data Retention: 90 Years for Industrial Parts (at 85°C) and 190 Years for Commercial Parts (at 70°C)**
- **Green (Pb/Halide-free/RoHS Compliant) Package Options Available**

FPGA Configuration EEPROM Memory

AT17LV65A
AT17LV128A
AT17LV256A
AT17LV512A
AT17LV010A
AT17LV002A

3.3V and 5V System Support

1. Description

The AT17A series FPGA configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17A series device is packaged in the 8-lead PDIP[1], 20-lead PLCC and 32-lead TQFP, see Table 1-1. The AT17A series configurator uses a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function by programming four EEPROM bytes.These devices also support a write-protection mechanism within its programming mode.

Note: 1. The 8-lead LAP, PDIP and SOIC packages for the AT17LV65A/128A/256A do not have an A label. However, the 8-lead packages are pin compatible with the 8-lead package of Altera's EEPROMs, refer to the AT17LV65/128/256/512/010/002/040 datasheet available on the Atmel web site for more information.

The AT17A series configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

Table 1-1. AT17A Series Packages

Package	AT17LV65A/ AT17LV128A/ AT17LV256A	AT17LV512A	AT17LV010A	AT17LV002A
8-lead PDIP	Yes	Yes	Yes	–
20-lead PLCC	Yes	Yes	Yes	Yes
32-lead TQFP	–	–	Yes	Yes

2322G–CNFG–03/06

2. Pin Configuration

Figure 2-1. 8-lead PDIP

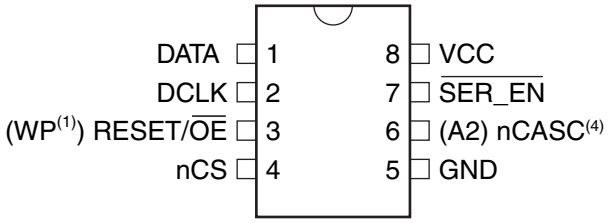


Figure 2-2. 20-lead PLCC

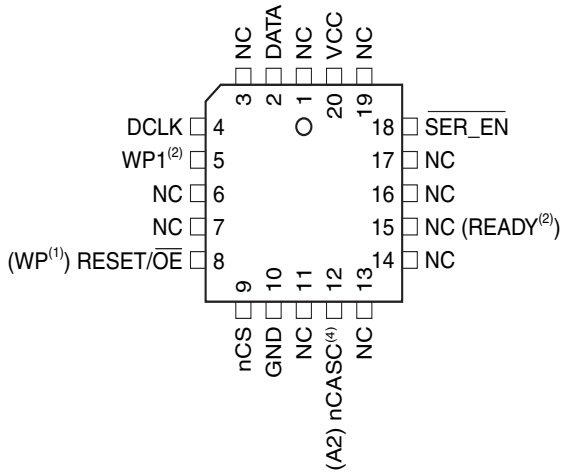
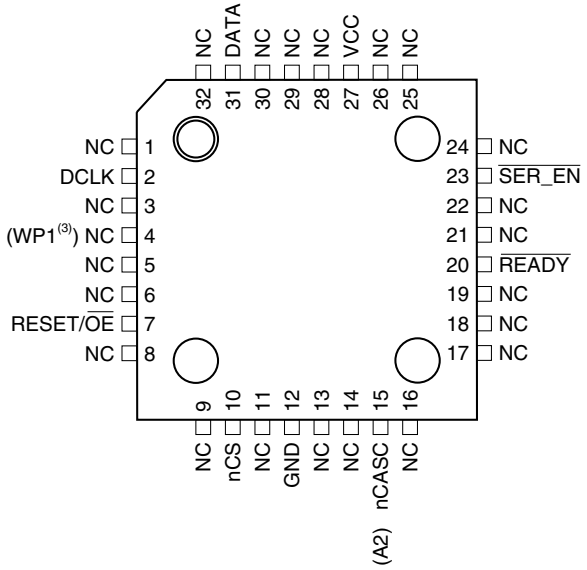
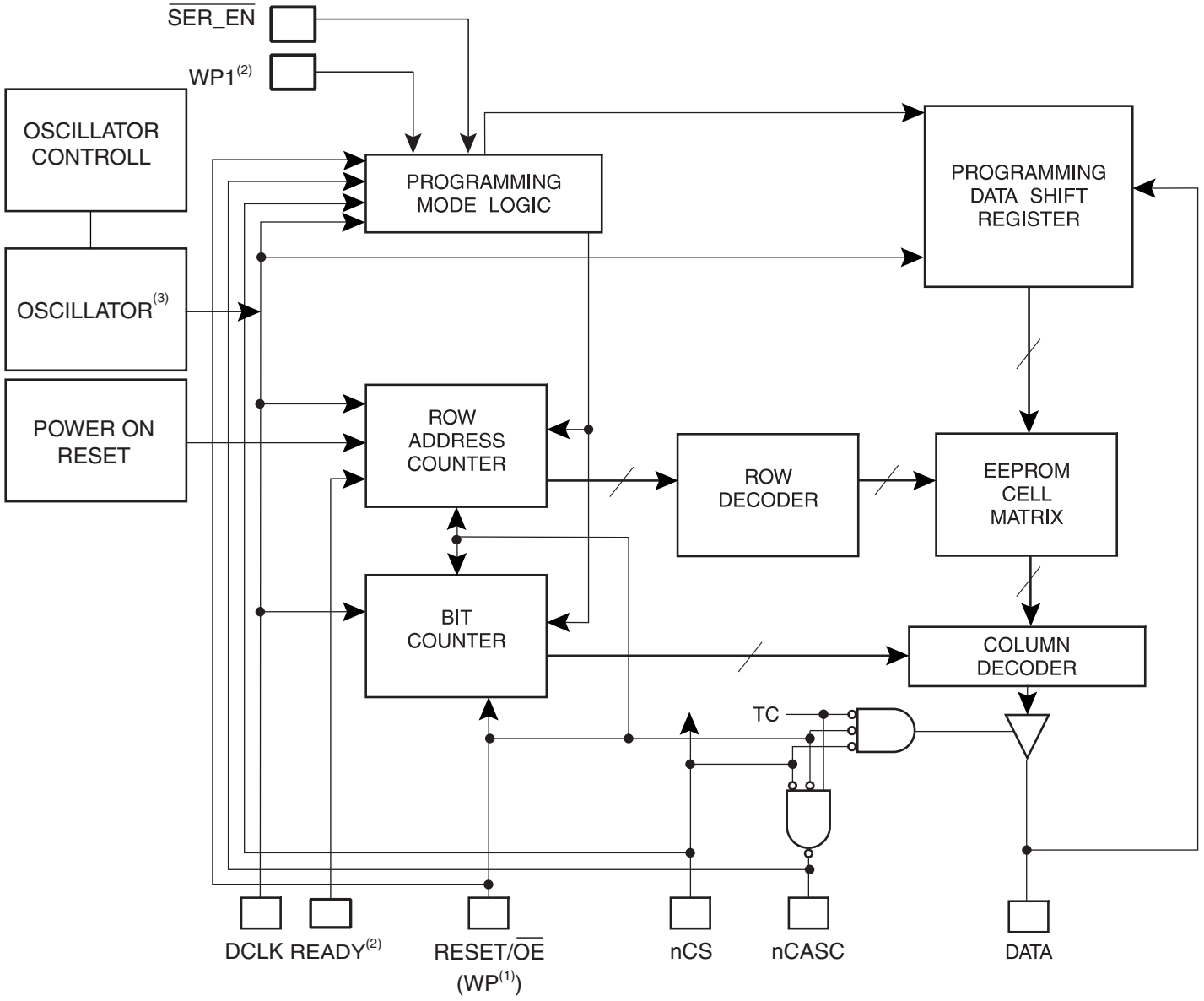


Figure 2-3. 32-lead TQFP



Notes:
1. This pin is only available on AT17LV65A/128A/256A devices.
2. This pin is only available on AT17LV512A/010A/002A devices.
3. This pin is only available on AT17LV010A/002A devices.
4. The nCASC feature is not available on the AT17LV65A device.

Figure 2-4. Block Diagram



Notes: 1. This pin is only available on AT17LV65A/128A/256A devices.
2. This pin is only available on AT17LV512A/010A/002A devices.
3. The nCASC feature is not available on the AT17LV65A device.

3. Device Description

The control signals for the configuration EEPROM (nCS, RESET/$\overline{OE}$ and DCLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external controller.

The configuration EEPROM's RESET/$\overline{OE}$ and nCS pins control the tri-state buffer on the DATA output pin and enable the address counter and the oscillator. When RESET/$\overline{OE}$ is driven Low, the configuration EEPROM resets its address counter and tri-states its DATA pin. The nCS pin also controls the output of the AT17A series configurator. If nCS is held High after the RESET/$\overline{OE}$ pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven subsequently Low, the counter and the DATA output pin are enabled. When RESET/$\overline{OE}$ is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of the nCS.

When the configurator has driven out all of its data and nCASC is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

This is the default setting for the device. Since almost all FPGAs use RESET Low and OE High, this document will describe $\overline{RESET}$/OE.

4. Pin Description

Name	I/O	AT17LV65A/ AT17LV128A/ AT17LV256A	AT17LV512A/ AT17LV010A			AT17LV002A	
		20 PLCC	8 PDIP	20 PLCC	32 TQFP	20 PLCC	32 TQFP
DATA	I/O	2	1	2	31	2	31
DCLK	I	4	2	4	2	4	2
WP1	I	–	–	5	4	5	4
RESET/$\overline{OE}$	I	8	3	8	7	8	7
$\overline{nCS}$	I	9	4	9	10	9	10
GND		10	5	10	12	10	12
$\overline{nCASC}$	O	12	6	12	15	12	15
A2	I						
READY	O	–	–	15	20	15	20
$\overline{SER_EN}$	I	18	7	18	23	18	23
V_{CC}		20	8	20	27	20	27

Note: 1. The nCASC feature is not available on the AT17LV65A device.

4.1 DATA

Three-state DATA output for configuration. Open-collector bi-directional pin for programming.

4.2 DCLK

Clock output or clock input. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the RESET/$\overline{OE}$ input is held High, the nCS input is held Low, and all configuration data has not been transferred to the target device (otherwise, as the master device, the DCLK pin drives Low).

4.3 WP1

WRITE PROTECT (1). This pin is used to protect portions of memory during programming, and it is disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations. This pin is only available on AT17LV512A/010A/002A devices.

4.4 $\overline{RESET/OE}$

Output Enable (active High) and RESET (active Low) when $\overline{SER_EN}$ is High. A Low logic level resets the address counter. A High logic level (with nCS Low) enables DATA and permits the address counter to count. In the mode, if this pin is Low (reset), the internal oscillator becomes inactive and DCLK drives Low. The logic polarity of this input is programmable and must be programmed active High (RESET active Low) by the user during programming for Altera applications.

4.5 WP

Write protect (WP) input (when $\overline{nCS}$ is Low) during programming only ($\overline{SER_EN}$ Low). When WP is Low, the entire memory can be written. When WP is enabled (High), the lowest block of the memory cannot be written. This pin is only available on AT17LV65A/128A/256A devices.

4.6 $\overline{nCS}$

Chip Select input (active Low). A Low input (with OE High) allows DCLK to increment the address counter and enables DATA to drive out. If the AT17A series is reset with nCS Low, the device initializes as the first (and master) device in a daisy-chain. If the AT17A series is reset with nCS High, the device initializes as a subsequent AT17A series device in the chain.

4.7 GND

Ground pin. A 0.2 µF decoupling capacitor between V_{CC} and GND is recommended.

4.8 nCASC

Cascade Select Output (active Low). This output goes Low when the address counter has reached its maximum value. In a daisy-chain of AT17A series devices, the nCASC pin of one device is usually connected to the nCS input pin of the next device in the chain, which permits DCLK from the master configurator to clock data from a subsequent AT17A series device in the chain. This feature is not available on the AT17LV65A device.

4.9 A2

Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{SER_EN}$ is Low). A2 has an internal pull-down resistor.

4.10 READY

Open collector reset state indicator. Driven Low during power-on reset cycle, released when power-up is complete. (recommended 4.7 kΩ pull-up on this pin if used).

4.11 $\overline{\text{SER_EN}}$

Serial enable must be held High during FPGA loading operations. Bringing $\overline{\text{SER_EN}}$ Low enables the 2-wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER_EN}}$ should be tied to V_{CC}.

4.12 V_{CC}

3.3V (±10%) and 5.0V (±5% Commercial, ±10% Industrial) power supply pin.

5. FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17A Serial Configuration EEPROM has been designed for compatibility with the Master Serial mode.

This document discusses the Altera FLEX FPGA device interfaces

6. Control of Configuration

Most connections between the FPGA device and the AT17A Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17A series configurator drives DIN of the FPGA devices.
- The master FPGA DCLK output or external clock source drives the DCLK input of the AT17A series configurator.
- The nCASC output of any AT17A series configurator drives the nCS input of the next configurator in a cascaded chain of EEPROMs.
- $\overline{\text{SER_EN}}$ must be connected to V_{CC} (except during ISP).

7. Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the next clock signal to the configurator asserts its nCASC output low and disables its DATA line driver. The second configurator recognizes the low level on its nCS input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the RESET/$\overline{\text{OE}}$ on each configurator is driven to a Low level.

If the address counters are not to be reset upon completion, then the RESET/$\overline{\text{OE}}$ input can be tied to a High level.

The AT17LV65A devices do not have the nCASC feature to perform cascaded configurations.

8. AT17A Series Reset Polarity

The AT17A series configurator allows the user to program the polarity of the RESET/$\overline{OE}$ pin as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This feature is supported by industry-standard programmer algorithms.

9. Programming Mode

The programming mode is entered by bringing $\overline{SER_EN}$ Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip.

10. Standby Mode

The AT17LV65A/128A/256A enters a low-power standby mode whenever nCS is asserted High. In this mode, the configurator consumes less than 50 µA of current at 3.3V (100 µA for the AT17LV512A/010A/002A). The output remains in a high-impedance state regardless of the state of the RESET/$\overline{OE}$ input.

11. Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

12. Operating Conditions

Symbol	Description		3.3V		5V		Units
			Min	Max	Min	Max	
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	3.0	3.6	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	3.0	3.6	4.5	5.5	V

13. DC Characteristics

V_{CC} = 3.3V ± 10%

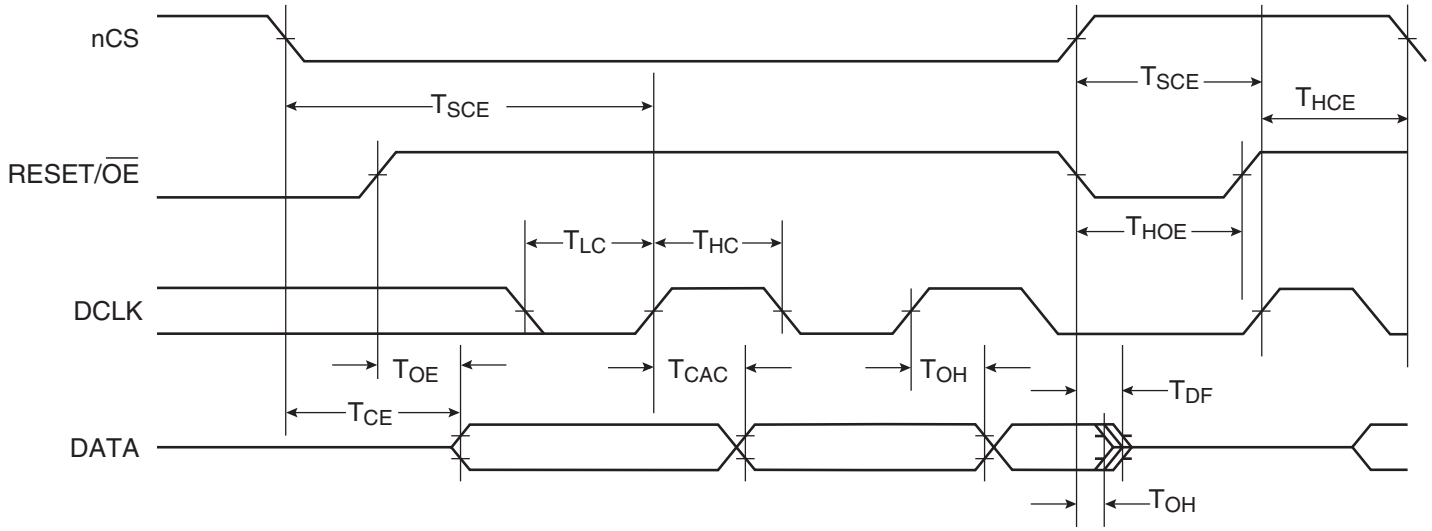
Symbol	Description		AT17LV65A/ AT17LV128A/ AT17LV256A		AT17LV512A/ AT17LV010A		AT17LV002A		Units
			Min	Max	Min	Max	Min	Max	
V_{IH}	High-level Input Voltage		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	2.4		2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4		0.4		0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	2.4		2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4		0.4		0.4	V
I_{CCA}	Supply Current, Active Mode			5		5		5	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	-10	10	-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		50		100		150	µA
		Industrial		100		100		150	µA

14. DC Characteristics

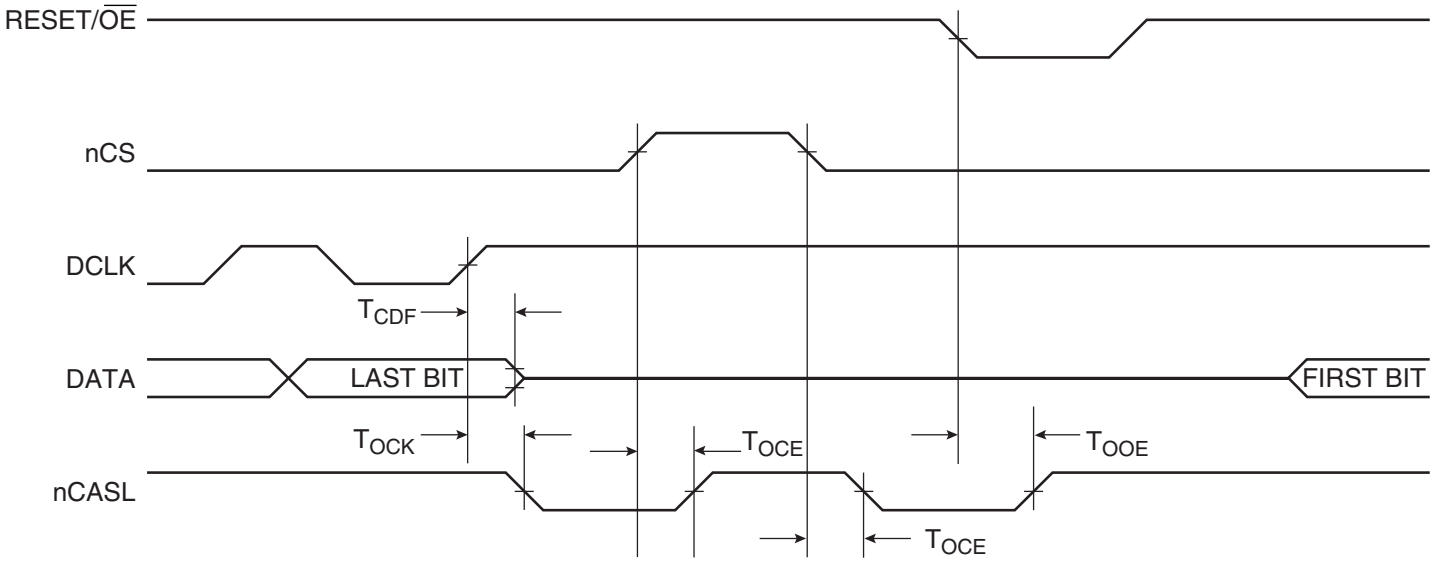
V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial

Symbol	Description		AT17LV65A/ AT17LV128A/ AT17LV256A		AT17LV512A/ AT17LV010A		AT17LV002A		Units
			Min	Max	Min	Max	Min	Max	
V_{IH}	High-level Input Voltage		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	3.7		3.86		3.86		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.32		0.32		0.32	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	3.6		3.76		3.76		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.37		0.37		0.37	V
I_{CCA}	Supply Current, Active Mode			10		10		10	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	-10	10	-10	10	µA
I_{CCS1}	Supply Current, Standby Mode	Commercial		75		200		350	µA
		Industrial		150		200		350	µA

15. AC Waveforms



16. AC Waveforms when Cascading



17. AC Characteristics

V_{CC} = 3.3V ± 10%

Symbol	Description	AT17LV65A/128A/256A				AT17LV512A/010A/002A				Units
		Commercial		Industrial		Commercial		Industrial		
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{OE} (1)	OE to Data Delay		50		55		50		55	ns
T_{CE} (1)	$\overline{CE}$ to Data Delay		60		60		55		60	ns
T_{CAC} (1)	CLK to Data Delay		75		80		55		60	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		0		0		0		ns
T_{DF} (2)	$\overline{CE}$ or OE to Data Float Delay		55		55		50		50	ns
T_{LC}	CLK Low Time	25		25		25		25		ns
T_{HC}	CLK High Time	25		25		25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		60		30		35		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	25		25		25		25		ns
F_{MAX}	Maximum Input Clock Frequency	10		10		15		10		MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

18. AC Characteristics when Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	AT17LV65A/128A/256A				AT17LV512A/010A/002A				Units
		Commercial		Industrial		Commercial		Industrial		
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{CDF} (2)	CLK to Data Float Delay		60		60		50		50	ns
T_{OCK} (1)	CLK to $\overline{CEO}$ Delay		55		60		50		55	ns
T_{OCE} (1)	$\overline{CE}$ to $\overline{CEO}$ Delay		55		60		35		40	ns
T_{OOE} (1)	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		40		45		35		35	ns
F_{MAX}	Maximum Input Clock Frequency	8		8		12.5		10		MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

19. AC Characteristics

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial

		AT17LV65A/128A/256A				AT17LV512A/010A/002A				
		Commercial		Industrial		Commercial		Industrial		
Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
T_{OE}[1]	OE to Data Delay		30		35		30		35	ns
T_{CE}[1]	$\overline{CE}$ to Data Delay		45		45		45		45	ns
T_{CAC}[1]	CLK to Data Delay		50		55		50		50	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		0		0		0		ns
T_{DF}[2]	$\overline{CE}$ or OE to Data Float Delay		50		50		50		50	ns
T_{LC}	CLK Low Time	20		20		20		20		ns
T_{HC}	CLK High Time	20		20		20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	35		40		20		25		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	20		20		20		20		ns
F_{MAX}	Maximum Input Clock Frequency	12.5		12.5		15		15		MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

20. AC Characteristics when Cascading

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial

		AT17LV65A/128A/256A				AT17LV512A/010A/002A				
		Commercial		Industrial		Commercial		Industrial		
Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Units
T_{CDF}[2]	CLK to Data Float Delay		50		50		50		50	ns
T_{OCK}[1]	CLK to $\overline{CEO}$ Delay		35		40		35		40	ns
T_{OCE}[1]	$\overline{CE}$ to $\overline{CEO}$ Delay		35		35		35		35	ns
T_{OOE}[1]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		30		35		30		30	ns
F_{MAX}	Maximum Input Clock Frequency	10		10		12.5		12.5		MHz

Notes: 1. AC test lead = 50 pF.

2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

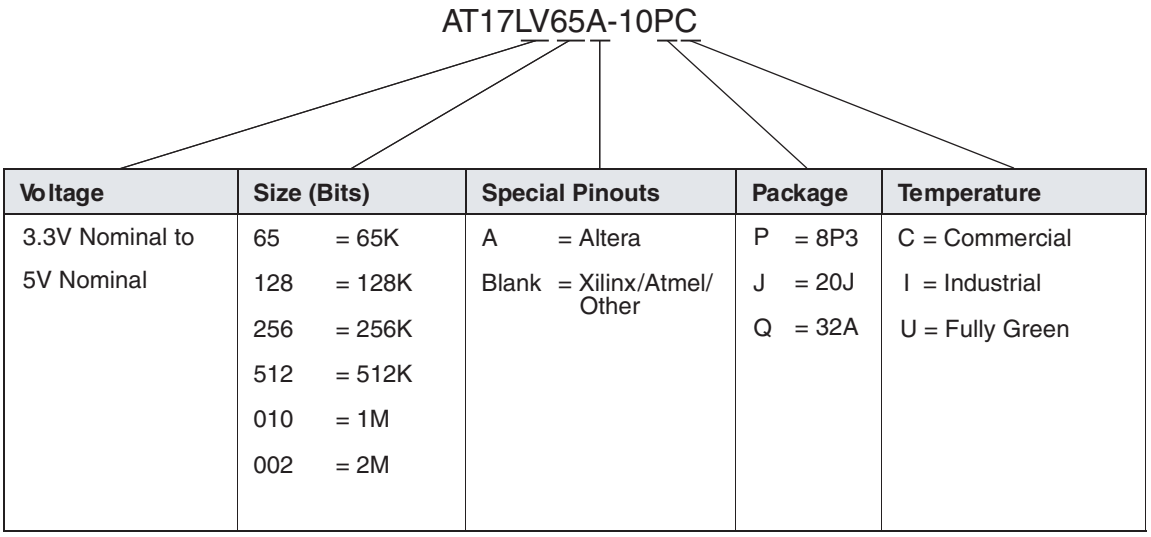
21. Thermal Resistance Coefficients[1]

Package Type			AT17LV65A/ AT17LV128A/ AT17LV256A	AT17LV512A/ AT17LV010A	AT17LV002A
8P3	Plastic Dual Inline Package (PDIP)	θ_{JC} [°C/W]		37	
		θ_{JA} [°C/W][2]		107	
20J	Plastic Leaded Chip Carrier (PLCC)	θ_{JC} [°C/W]	35	35	35
		θ_{JA} [°C/W][2]	90	90	90
32A	Thin Plastic Quad Flat Package (TQFP)	θ_{JC} [°C/W]			
		θ_{JA} [°C/W][2]			
44J	Plastic Leaded Chip Carrier (PLCC)	θ_{JC} [°C/W]	–	–	15
		θ_{JA} [°C/W][2]	–	–	50

Notes: 1. For more information refer to the “Thermal Characteristics of Atmel’s Packages”, available on the Atmel web site.
2. Airflow = 0 ft/min.

22. Ordering Information

Figure 22-1. Ordering Code[1]



Voltage	Size (Bits)	Special Pinouts	Package	Temperature
3.3V Nominal to 5V Nominal	65 = 65K 128 = 128K 256 = 256K 512 = 512K 010 = 1M 002 = 2M	A = Altera Blank = Xilinx/Atmel/ Other	P = 8P3 J = 20J Q = 32A	C = Commercial I = Industrial U = Fully Green

Note: 1. The 8-lead LAP and SOIC packages for the AT17LV65A/128A/256A do not have an A label. However, the 8-lead packages are pin compatible with the 8-lead package of Altera's EEPROMs, refer to the AT17LV65/128/256/512/010/002/040 datasheet available on the Atmel web site for more information.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP)

22.1 Standard Package Options[1]

Memory Size	Ordering Code	Package	Operation Range
64-Kbit[2][7]	AT17LV65A-10JC	20J	Commercial (0°C to 70°C)
	AT17LV65A-10JI	20J	Industrial (-40°C to 85°C)
128-Kbit[7]	AT17LV128A-10JC	20J	Commercial (0°C to 70°C)
	AT17LV128A-10JI	20J	Industrial (-40°C to 85°C)
256-Kbit[3][7]	AT17LV256A-10JC	20J	Commercial (0°C to 70°C)
	AT17LV256A-10JI	20J	Industrial (-40°C to 85°C)
512-Kbit[4][7]	AT17LV512A-10PC AT17LV512A-10JC	8P3 20J	Commercial (0°C to 70°C)
	AT17LV512A-10PI AT17LV512A-10JI	8P3 20J	Industrial (-40°C to 85°C)
1-Mbit[5][7]	AT17LV010A-10PC AT17LV010A-10JC AT17LV010A-10QC	8P3 20J 32A	Commercial (0°C to 70°C)
	AT17LV010A-10PI AT17LV010A-10JI AT17LV010A-10QI	8P3 20J 32A	Industrial (-40°C to 85°C)
2-Mbit[6][7]	AT17LV002A-10JC AT17LV002A-10QC	20J 32A	Commercial (0°C to 70°C)
	AT17LV002A-10JI AT17LV002A-10QI	20J 32A	Industrial (-40°C to 85°C)

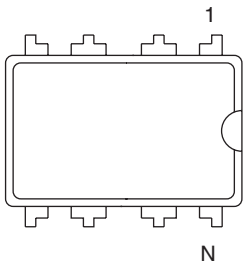
22.2 Green Package Options (Pb/Halide-free/RoHS Compliant)[1]

Memory Size	Ordering Code	Package	Operation Range
512-Kbit[4][7]	AT17LV512A-10JU	20J	Industrial (-40°C to 85°C)
1-Mbit[5][7]	AT17LV010A-10JU AT17LV010A-10PU	20J 8P3	Industrial (-40°C to 85°C)
2-Mbit[4][7]	AT17LV002A-10JU	20J	Industrial (-40°C to 85°C)

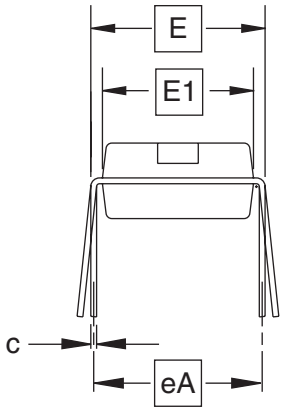
Notes:
1. Currently, there are two types of low-density configurators. The new version will be identified by a “B” after the datacode. The “B” version is fully backward-compatible with the original devices so existing customers will not be affected. The new parts no longer require a MUX for ISP. See programming specification for more details.
2. Use 64-Kbit density parts to replace Altera EPC1064.
3. Use 256-Kbit density parts to replace Altera EPC1213.
4. Use 512-Kbit density parts to replace Altera EPC1441.
5. Use 1-Mbit density parts to replace Altera EPC1
6. Use 2-Mbit density parts to replace Altera EPC2. Atmel AT17LV002A devices do not support JTAG programming; Atmel AT17LV002A devices use a 2-wire serial interface for in-system programming.
7. For operating voltage of 5V ±10%, please refer to the 5V ±10% AC and DC Characteristics.

23. Packaging Information

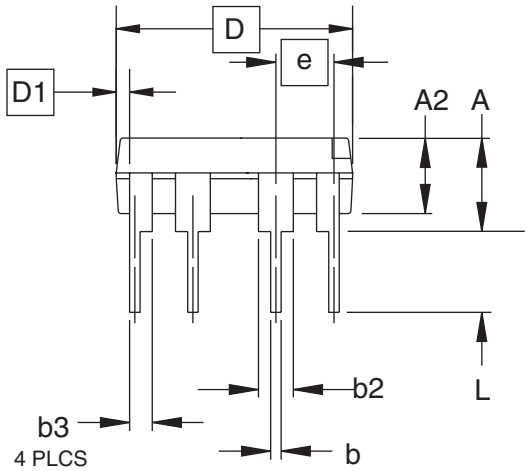
23.1 8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

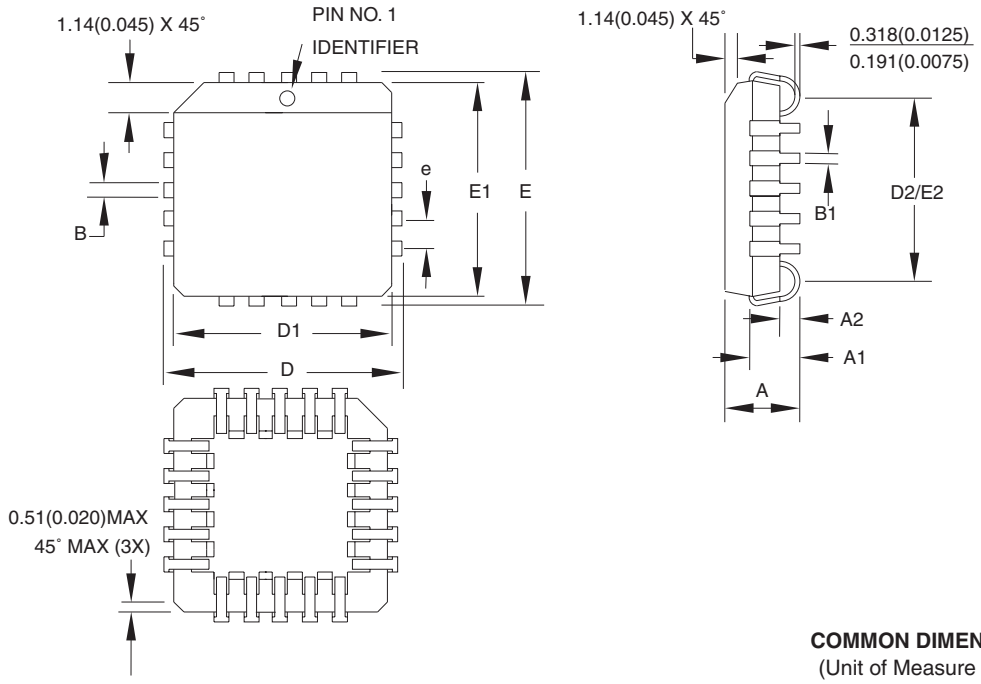
SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B

23.2 20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

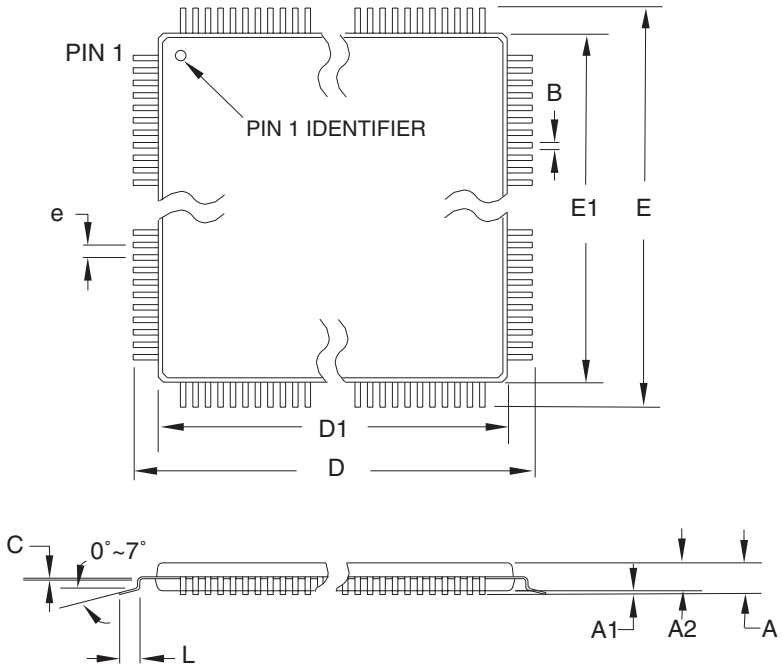
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

23.3 32A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32A,** 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	32A	B

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