- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **Low Noise**
  V_n = 18 nV/$\sqrt{Hz}$ Typ at f = 1 kHz
- **High Input Impedance . . . JFET Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

description/ordering information

The JFET-input operational amplifiers in the TL07x series are similar to the TL08x series, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07x series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

description/ordering information (continued)

ORDERING INFORMATION

T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	10 mV	PDIP (P)	Tube of 50	TL071CP	TL071CP
			Tube of 50	TL072CP	TL072CP
		PDIP (N)	Tube of 25	TL074CN	TL074CN
		SOIC (D)	Tube of 75	TL071CD	TL071C
			Reel of 2500	TL071CDR	
			Tube of 75	TL072CD	TL072C
			Reel of 2500	TL072CDR	
			Tube of 50	TL074CD	TL074C
			Reel of 2500	TL074CDR	
		SOP (NS)	Reel of 2000	TL074CNSR	TL074
		SOP (PS)	Reel of 2000	TL071CPSR	TL071
			Reel of 2000	TL072CPSR	T072
		TSSOP (PW)	Reel of 2000	TL072CPWR	T072
			Tube of 90	TL074CPW	T074
			Reel of 2000	TL074CPWR	
	6 mV	PDIP (P)	Tube of 50	TL071ACP	TL071ACP
			Tube of 50	TL072ACP	TL072ACP
		PDIP (N)	Tube of 25	TL074ACN	TL074ACN
		SOIC (D)	Tube of 75	TL071ACD	071AC
			Reel of 2500	TL071ACDR	
			Tube of 75	TL072ACD	072AC
			Reel of 2500	TL072ACDR	
			Tube of 50	TL074ACD	TL074AC
			Reel of 2500	TL074ACDR	
		SOP (PS)	Reel of 2000	TL072ACPSR	T072A
		SOP (NS)	Reel of 2000	TL074ACNSR	TL074A
	3 mV	PDIP (P)	Tube of 50	TL071BCP	TL071BCP
			Tube of 50	TL072BCP	TL072BCP
		PDIP (N)	Tube of 25	TL074BCN	TL074BCN
		SOIC (D)	Tube of 75	TL071BCD	071BC
			Reel of 2500	TL071BCDR	
			Tube of 75	TL072BCD	072BC
			Reel of 2500	TL072BCDR	
			Tube of 50	TL074BCD	TL074BC
			Reel of 2500	TL074BCDR	
		SOP (NS)	Reel of 2000	TL074BCNSR	TL074B

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

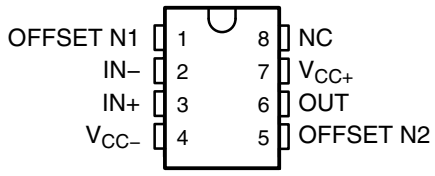
description/ordering information (continued)

ORDERING INFORMATION

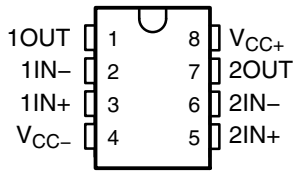
T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL071IP	TL071IP
			Tube of 50	TL072IP	TL072IP
		PDIP (N)	Tube of 25	TL074IN	TL074IN
		SOIC (D)	Tube of 75	TL071ID	TL071I
			Reel of 2500	TL071IDR	
			Tube of 75	TL072ID	TL072I
			Reel of 2500	TL072IDR	
			Tube of 50	TL074ID	TL074I
			Reel of 2500	TL074IDR	
–55°C to 125°C	6 mV	CDIP (JG)	Tube of 50	TL072MJGB	TL072MJGB
		CFP (U)	Tube of 150	TL072MUB	TL072MUB
		LCCC (FK)	Tube of 55	TL072MFKB	TL072MFKB
	9 mV	CDIP (J)	Tube of 25	TL074MJB	TL074MJB
		CFP (W)	Tube of 25	TL074MWB	TL074MWB
		LCCC (FK)	Tube of 55	TL074MFKB	TL074MFKB

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

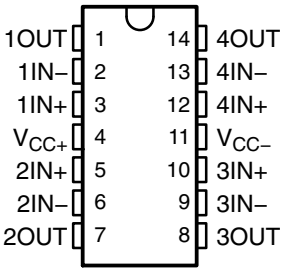
TL071, TL071A, TL071B
D, P, OR PS PACKAGE
(TOP VIEW)



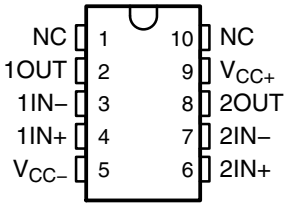
TL072, TL072A, TL072B
D, JG, P, PS, OR PW PACKAGE
(TOP VIEW)



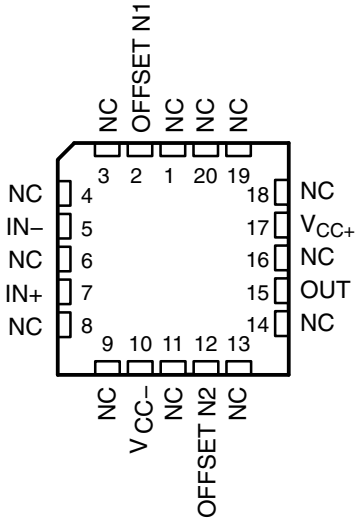
TL074A, TL074B
D, J, N, NS, OR PW PACKAGE
TL074 . . . D, J, N, NS, PW,
OR W PACKAGE
(TOP VIEW)



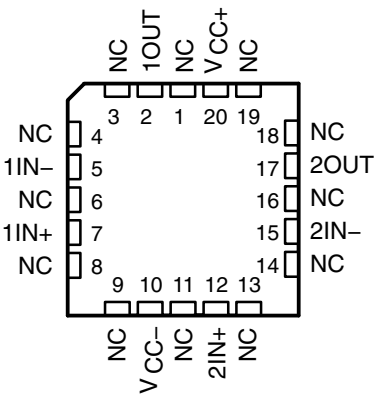
TL072
U PACKAGE
(TOP VIEW)



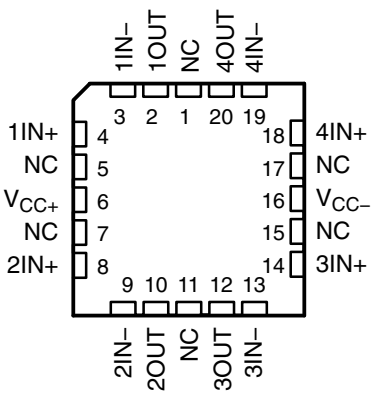
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



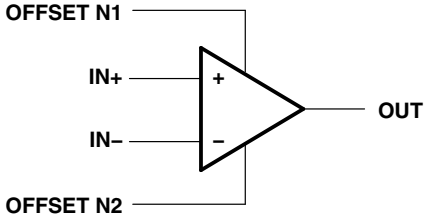
TL074
FK PACKAGE
(TOP VIEW)



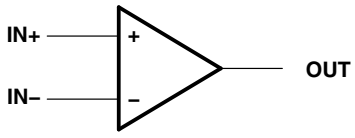
NC – No internal connection

symbols

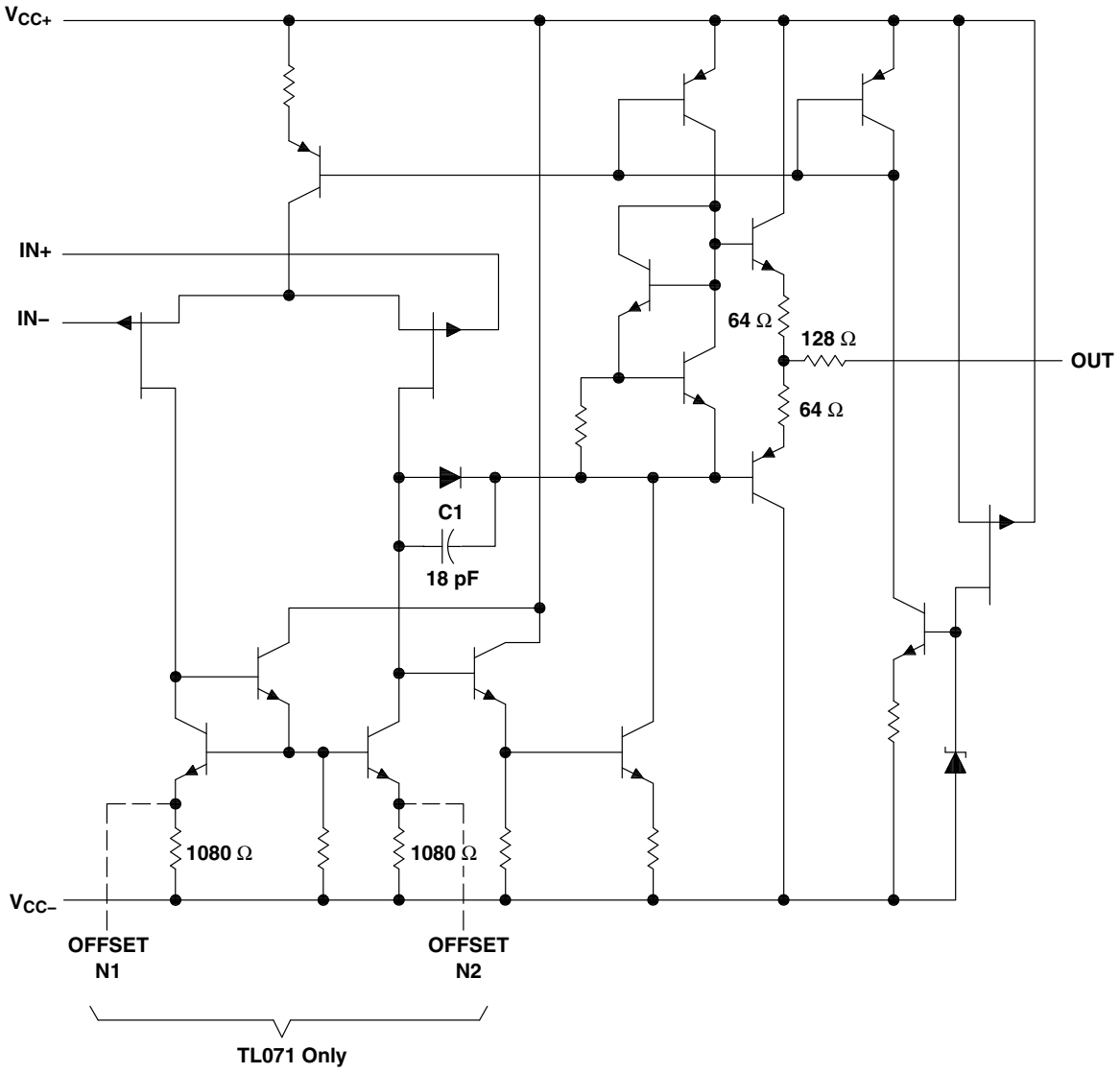
TL071



TL072 (each amplifier)
TL074 (each amplifier)



schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1):	V_{CC+}	18 V
	V_{CC-}	–18 V
Differential input voltage, V_{ID} (see Note 2)		±30 V
Input voltage, V_I (see Notes 1 and 3)		±15 V
Duration of output short circuit (see Note 4)		Unlimited
Package thermal impedance, θ_{JA} (see Notes 5 and 6):	D package (8 pin)	97°C/W
	D package (14 pin)	86°C/W
	N package	80°C/W
	NS package	76°C/W
	P package	85°C/W
	PS package	95°C/W
	PW package (8 pin)	149°C/W
	PW package (14 pin)	113°C/W
	U package	185°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8):	FK package	5.61°C/W
	J package	15.05°C/W
	JG package	14.5°C/W
	W package	14.65°C/W
Operating virtual junction temperature, T_J		150°C
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package		300°C
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+, with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10		3	6		2	3		3	6	mV
			Full range			13			7.5			5			8	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100		5	100		5	100	pA
			Full range			10			2			2			2	nA
I_{IB}	Input bias current§	V_O = 0	25°C		65	200		65	200		65	200		65	200	pA
			Full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	100		75	100		75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

‡ Full range is T_A = 0°C to 70°C for TL07_C,TL07_AC, TL07_BC and is T_A = −40°C to 85°C for TL07_I.

§ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

† Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = −55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	5	13		8	13		V/μs
t_r	Rise-time overshoot factor	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		μs
					20%			20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, $R_L \geq$ 2 kΩ, f = 1 kHz	A_{VD} = 1, $R_S \leq$ 1 kΩ,		0.003 %			0.003%		

PARAMETER MEASUREMENT INFORMATION

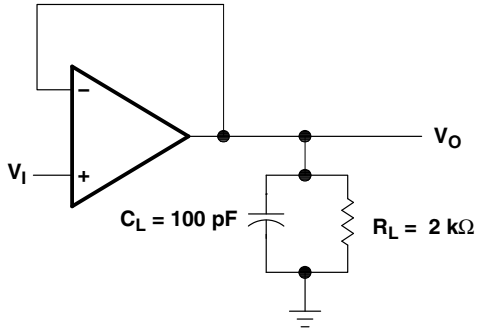


Figure 1. Unity-Gain Amplifier

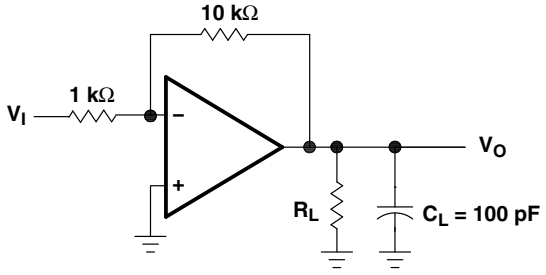


Figure 2. Gain-of-10 Inverting Amplifier

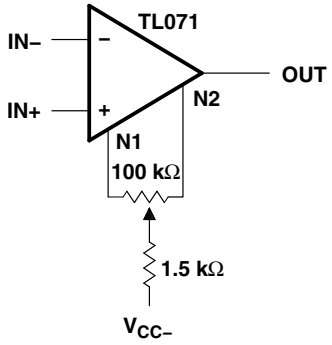


Figure 3. Input Offset-Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	4
V_{OM}	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
CMRR	Common-mode rejection ratio	vs Free-air temperature	14
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	15 16
P_D	Total power dissipation	vs Free-air temperature	17
	Normalized slew rate	vs Free-air temperature	18
V_n	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
	Large-signal pulse response	vs Time	21
V_O	Output voltage	vs Elapsed time	22

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

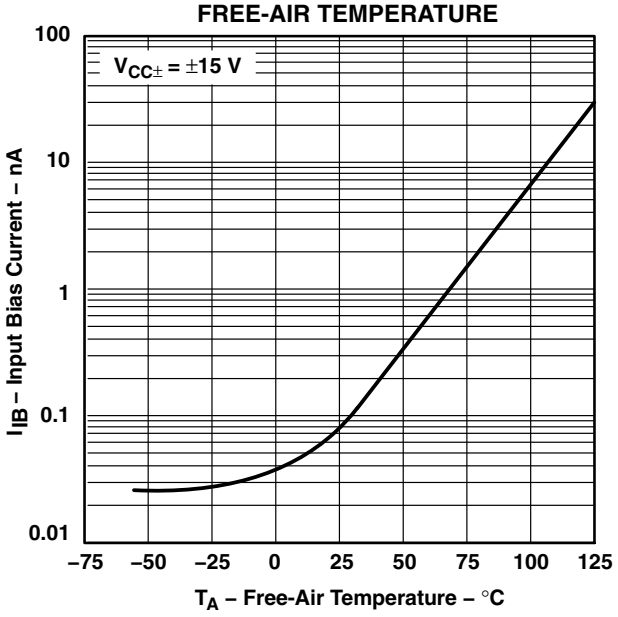


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

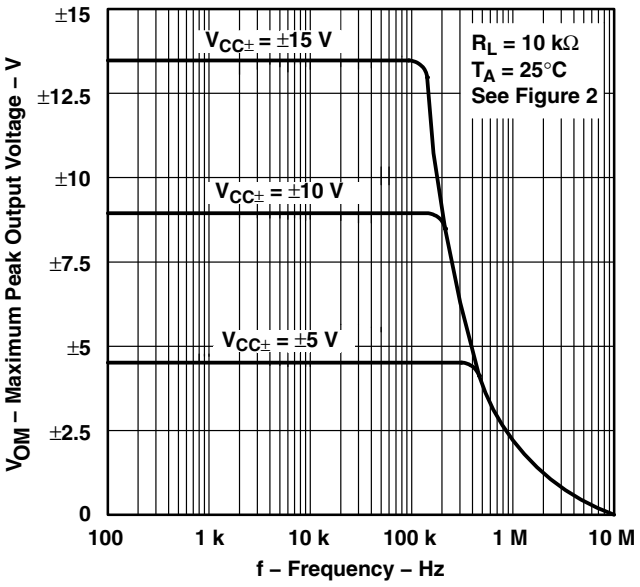


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

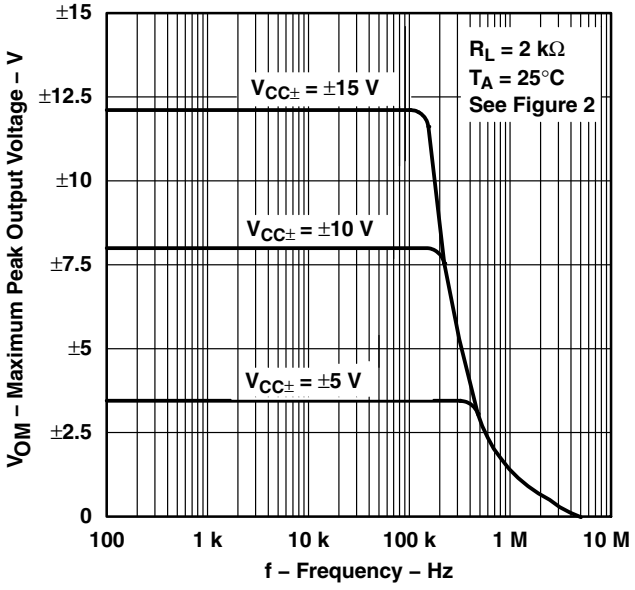


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

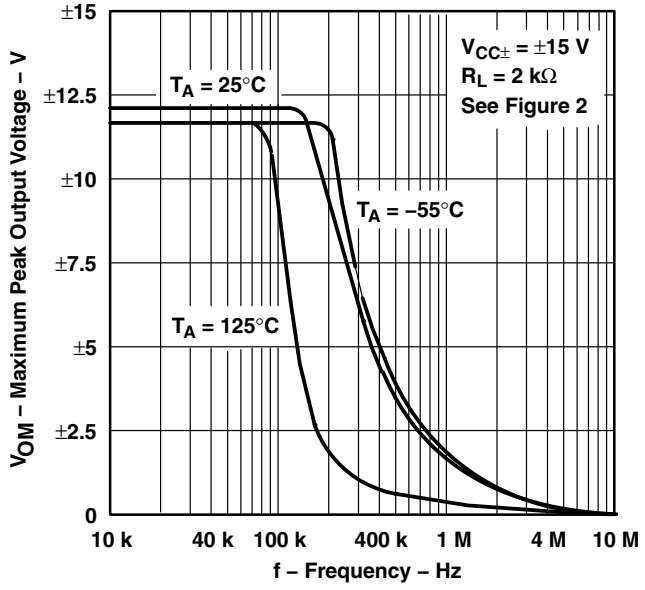


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

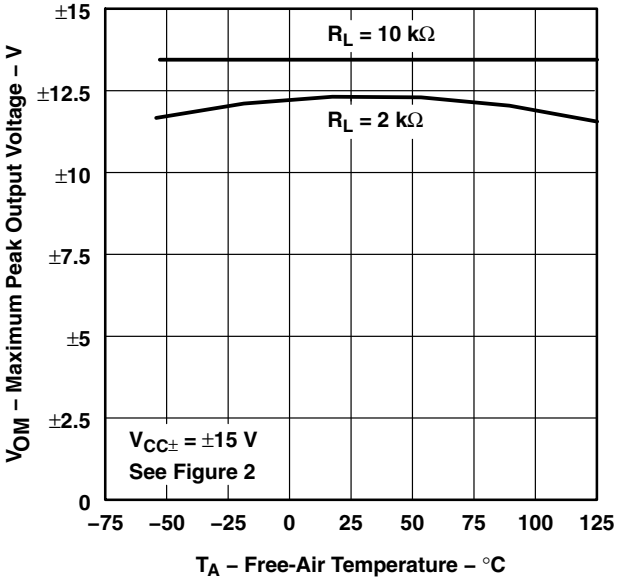


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

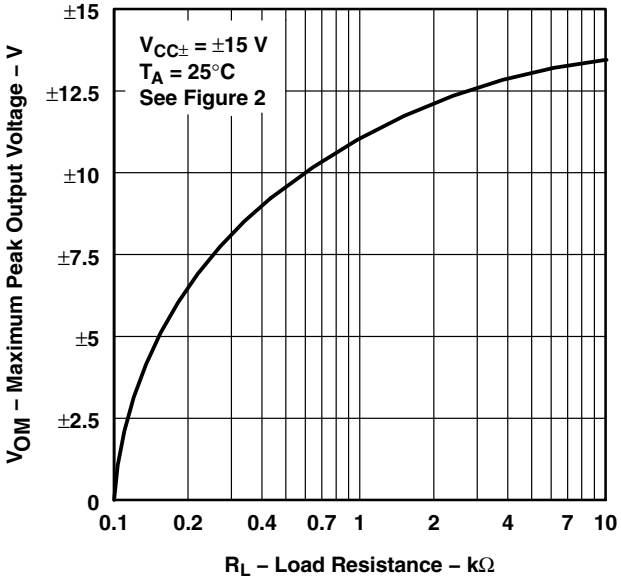


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

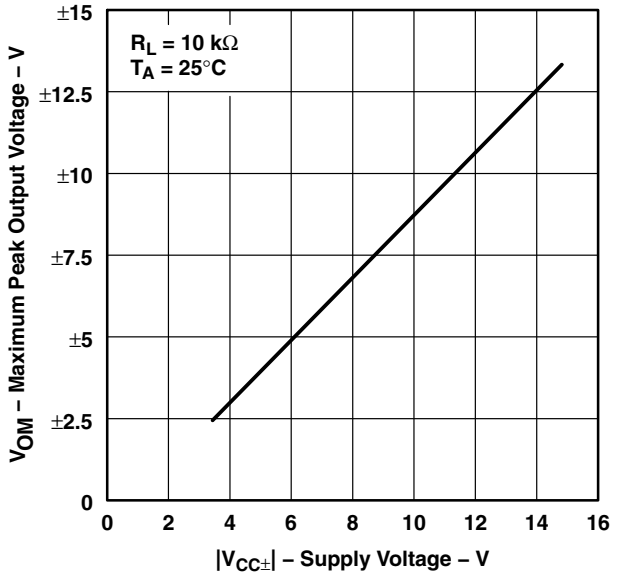


Figure 10

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

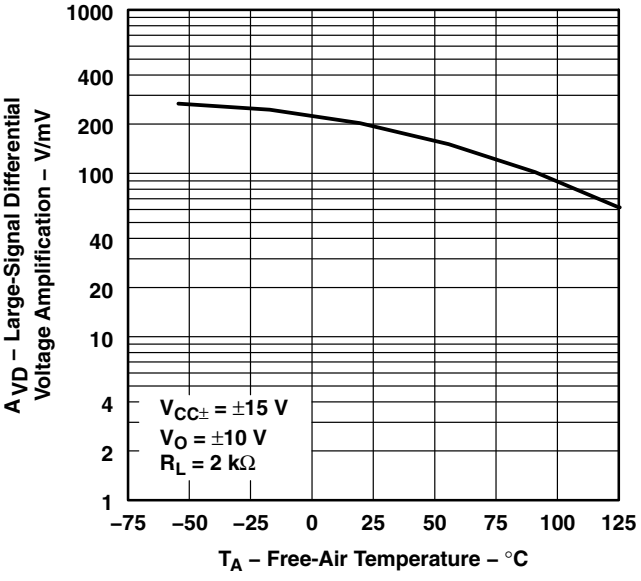


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

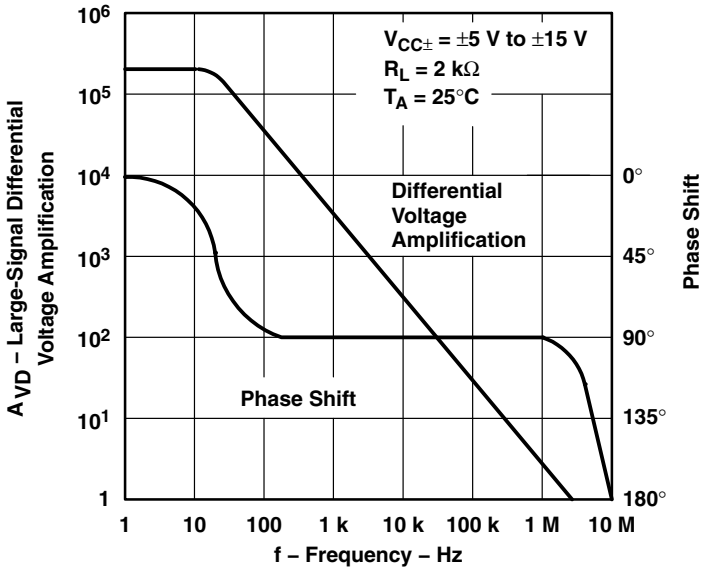


Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE

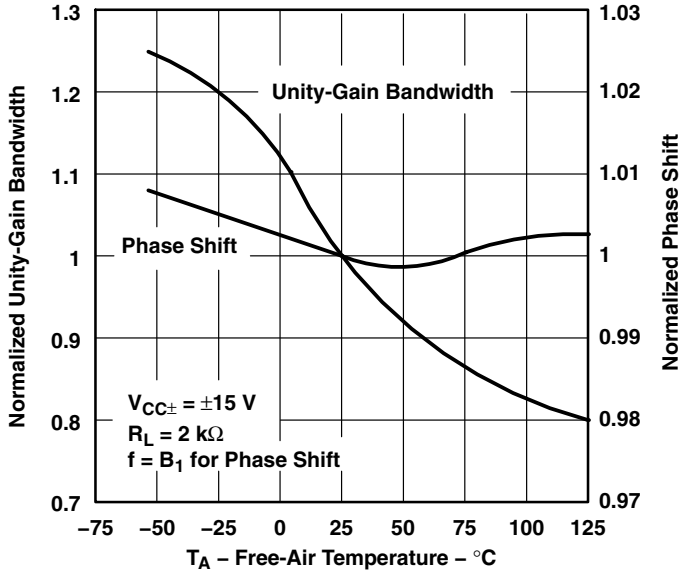


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

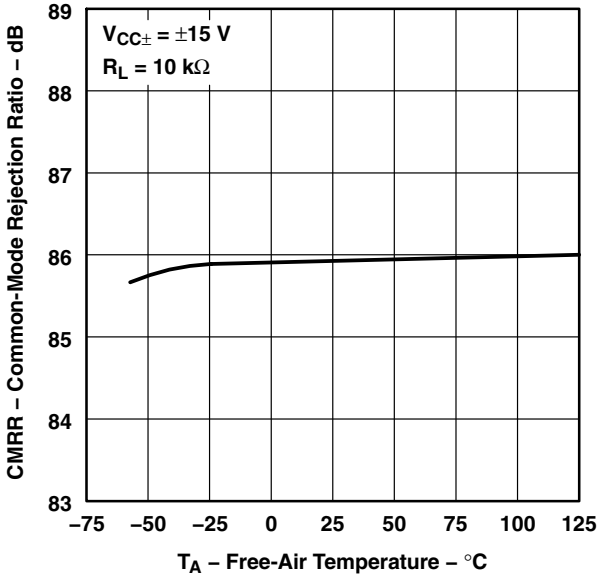


Figure 14

SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

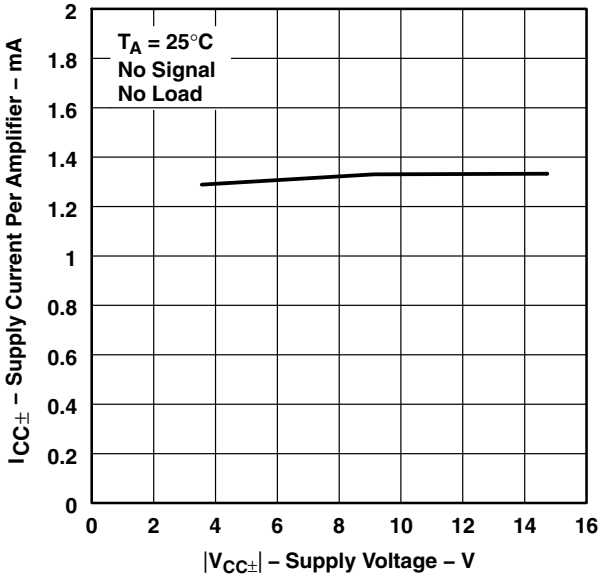


Figure 15

SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

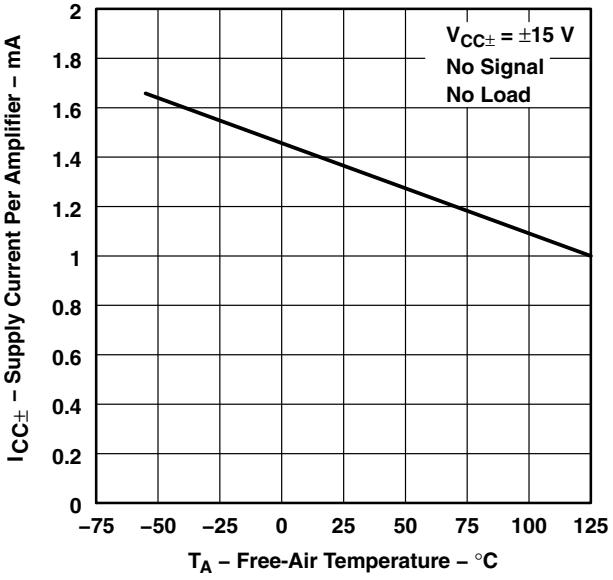


Figure 16

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

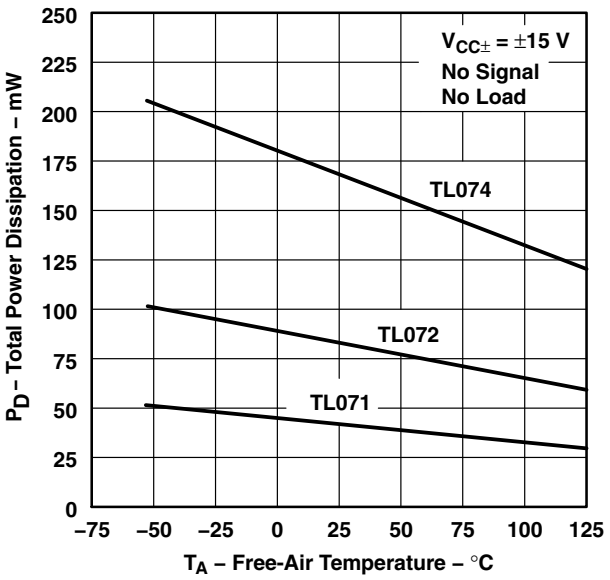


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

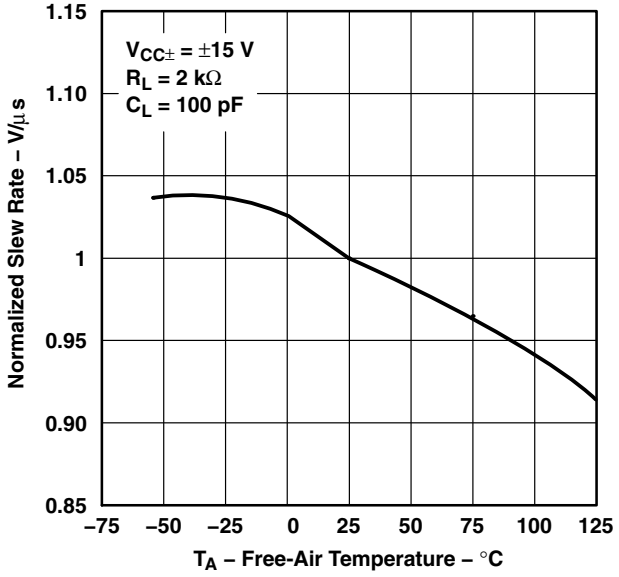


Figure 18

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

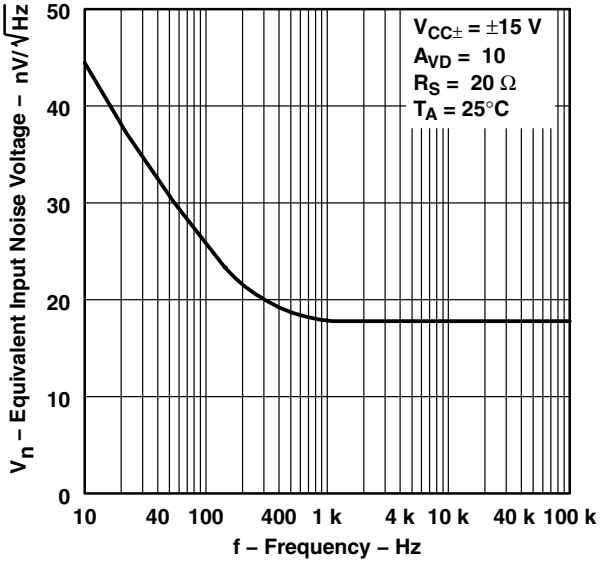


Figure 19

TOTAL HARMONIC DISTORTION vs FREQUENCY

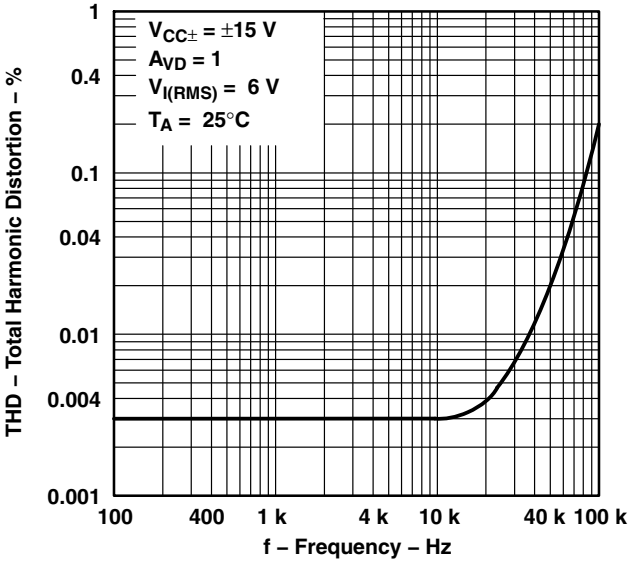


Figure 20

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

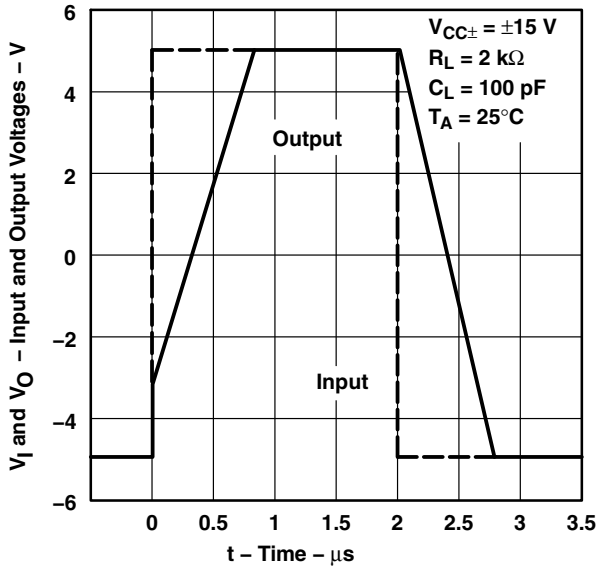


Figure 21

TYPICAL CHARACTERISTICS

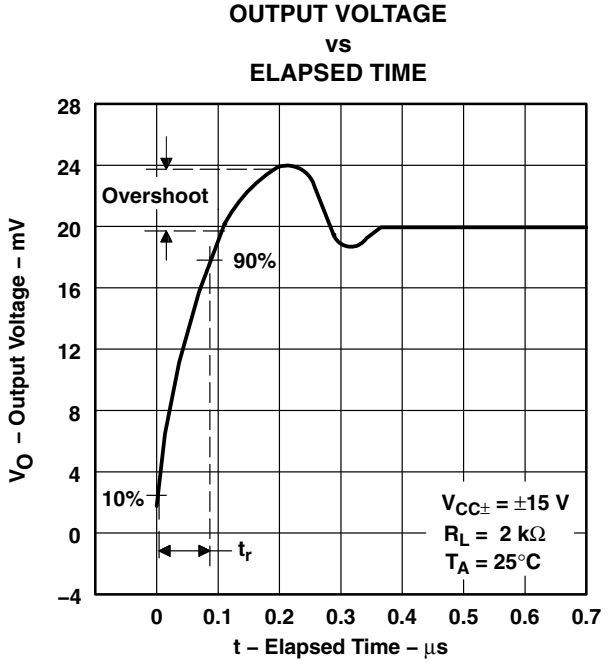


Figure 22

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27

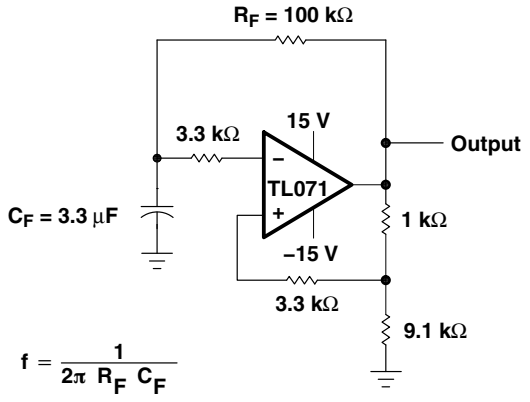


Figure 23. 0.5-Hz Square-Wave Oscillator

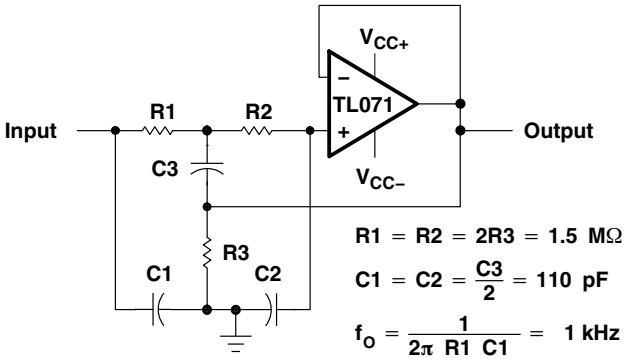


Figure 24. High-Q Notch Filter

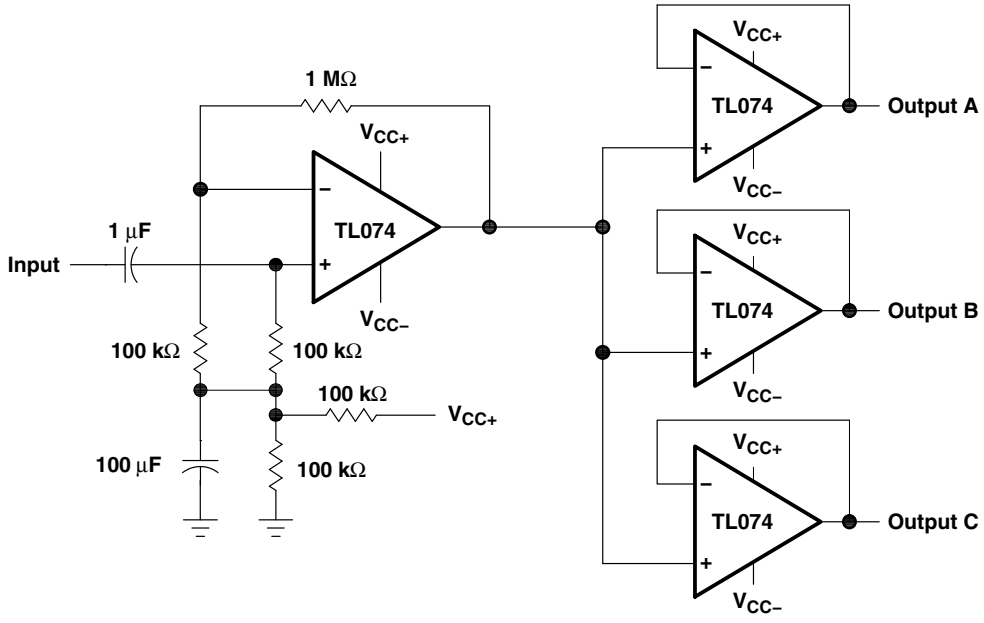
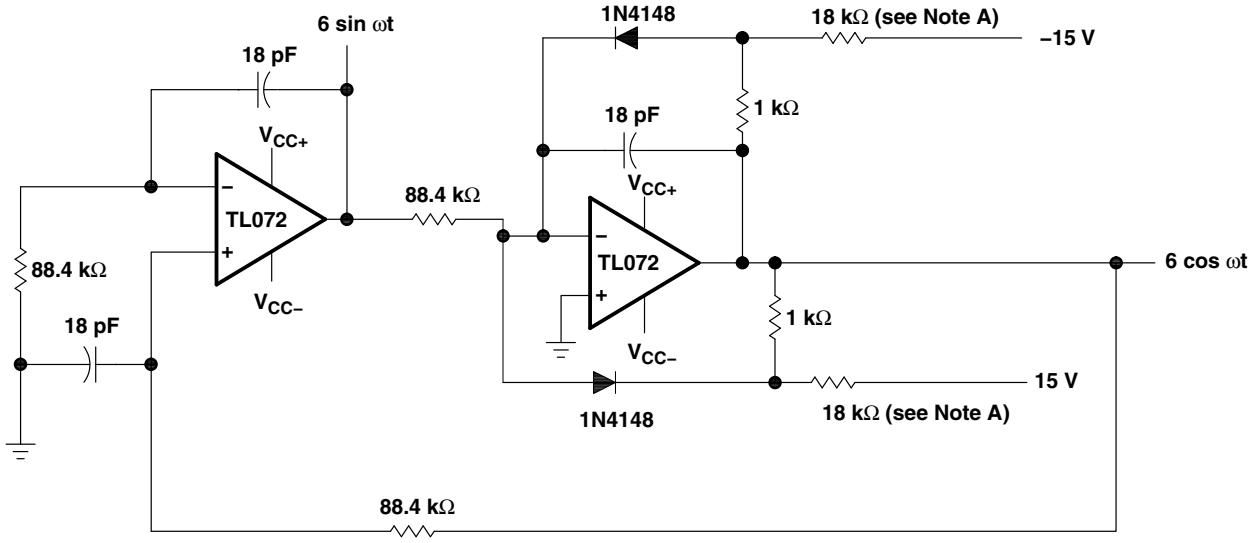


Figure 25. Audio-Distribution Amplifier

APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-kHz Quadrature Oscillator

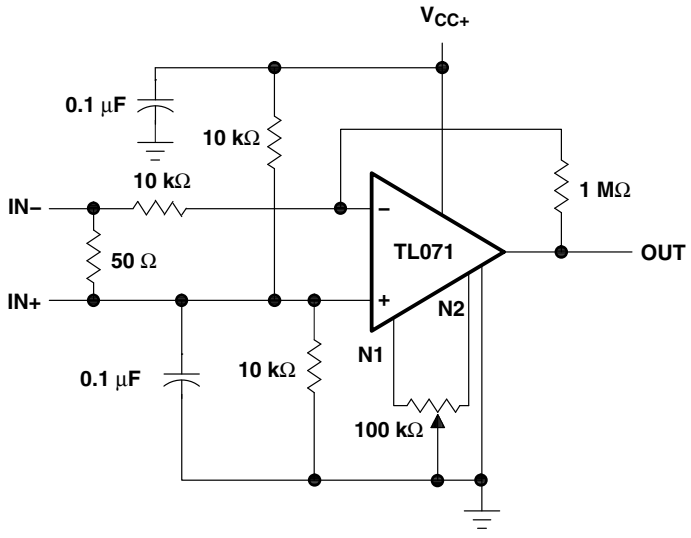


Figure 27. AC Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8102304HA	OBSOLETE			10		TBD	Call TI	Call TI	-55 to 125		
81023052A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
8102305HA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
8102305PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
81023062A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
8102306CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
8102306DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
JM38510/11906BCA	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
M38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
TL071-W	ACTIVE	WAFERSALE	YS	0		TBD	Call TI	Call TI			Samples
TL071ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071ACP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL071ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071ACP	Samples
TL071BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071BCP	Samples
TL071BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071BCP	Samples
TL071CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples
TL071CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples
TL071CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T071	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL071CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T071	Samples
TL071CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T071	Samples
TL071CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TL071ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-40 to 85		
TL071IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL071IP	Samples
TL071IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL071IP	Samples
TL071MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL071MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL071MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL072ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	0 to 70		
TL072ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072ACPSR	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70	T072A	
TL072ACPSRE4	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		
TL072ACPSRG4	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		
TL072BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	Samples
TL072BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	Samples
TL072CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		
TL072CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples
TL072IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
TL072MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL072MJG	Samples
TL072MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
TL072MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
TL074ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		
TL074ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A	Samples
TL074ACNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A	Samples
TL074ACNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A	Samples
TL074BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074BCDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples
TL074CNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples
TL074CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples
TL074CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70		
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-40 to 85		
TL074IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL074IN	Samples
TL074INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL074IN	Samples
TL074MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	TL074MFK	Samples
TL074MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
TL074MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL074MJ	Samples
TL074MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples
TL081-W	ACTIVE	WAFERSALE	YS	0		TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :

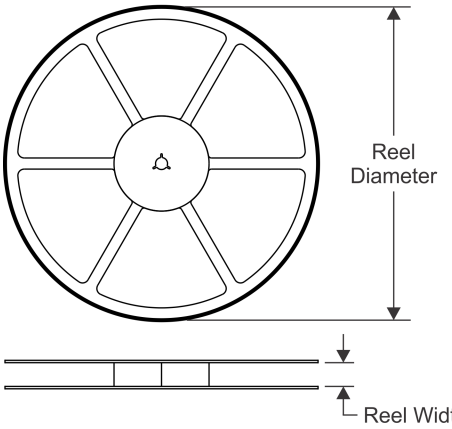
- Catalog: TL072, TL074
- Enhanced Product: TL072-EP, TL072-EP, TL074-EP, TL074-EP
- Military: TL072M, TL074M

NOTE: Qualified Version Definitions:

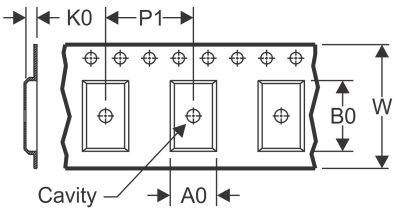
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

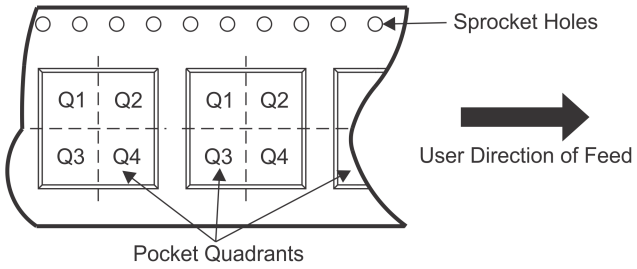


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

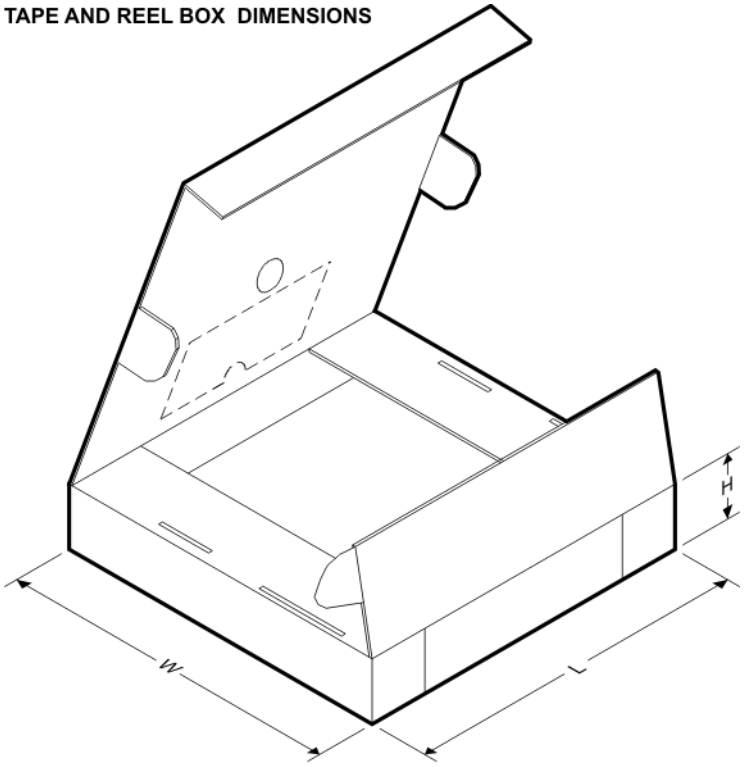
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

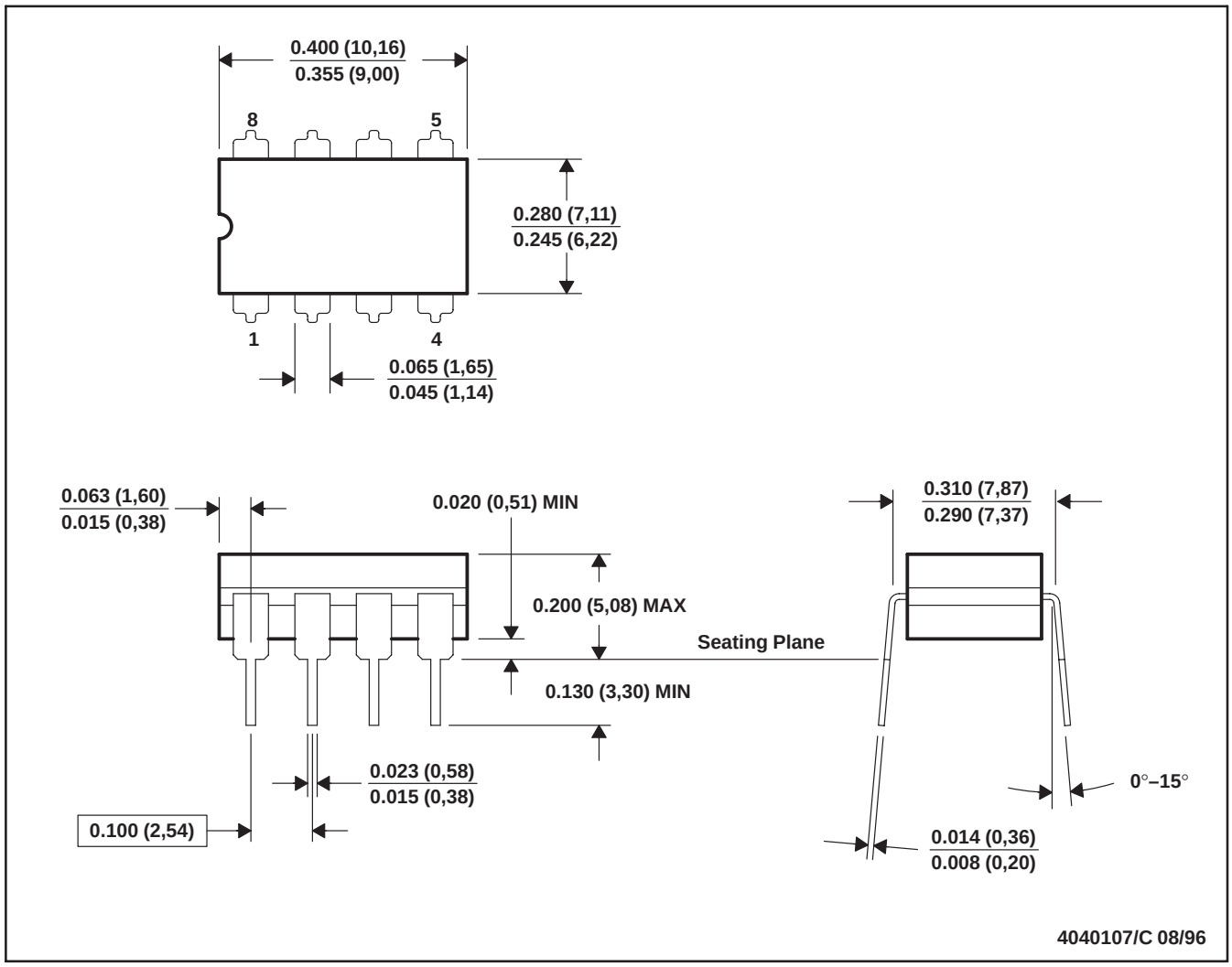


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL071CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL071IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL072CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL072IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL074ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074ACNSR	SO	NS	14	2000	367.0	367.0	38.0
TL074BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074CDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074CDRG4	SOIC	D	14	2500	333.2	345.9	28.6
TL074CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL074IDR	SOIC	D	14	2500	333.2	345.9	28.6

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

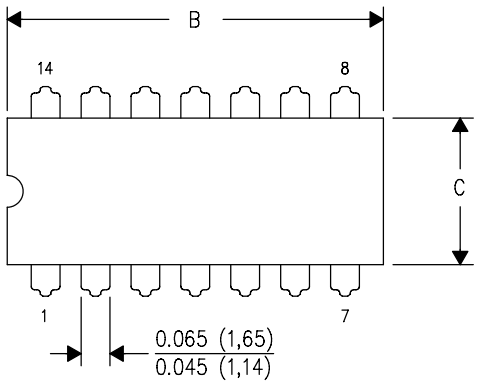


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

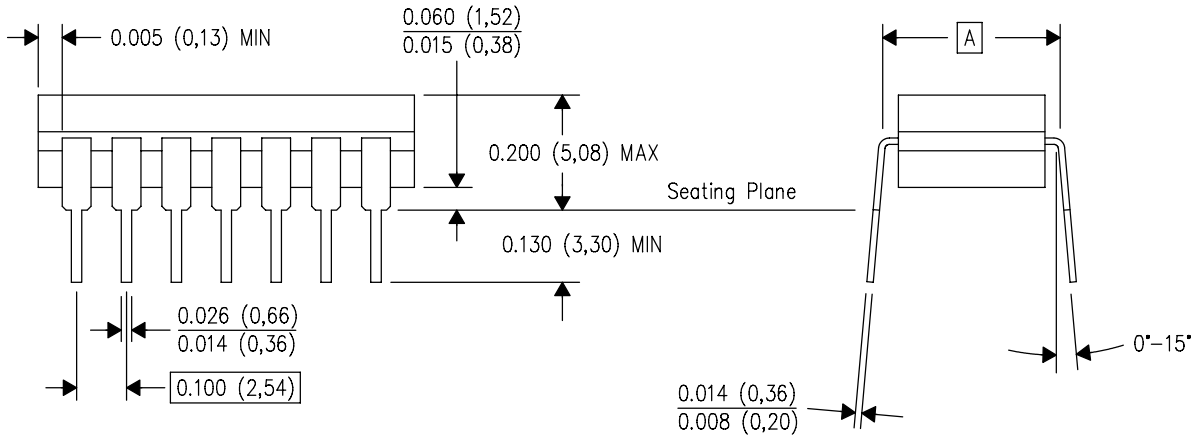
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



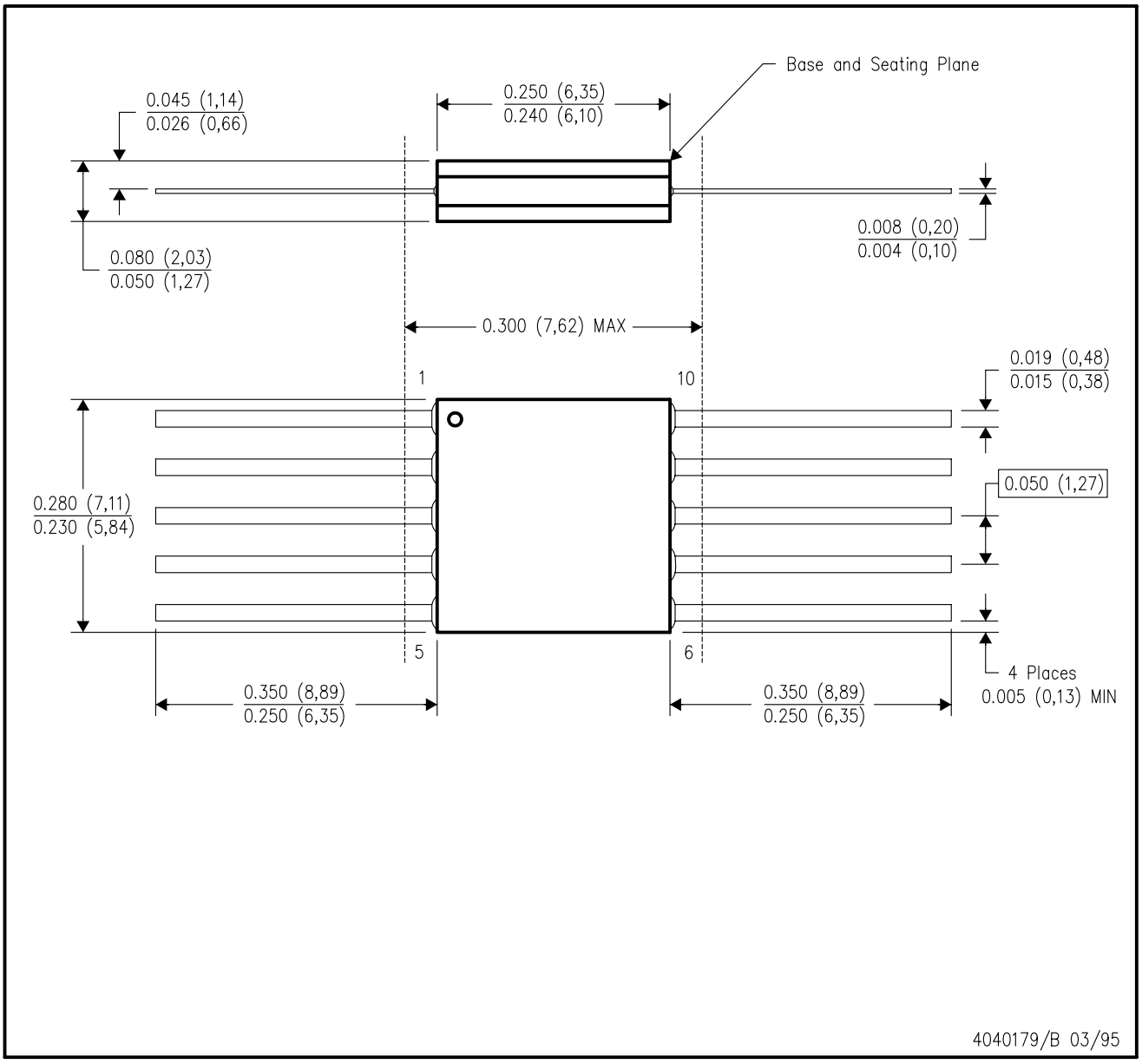
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

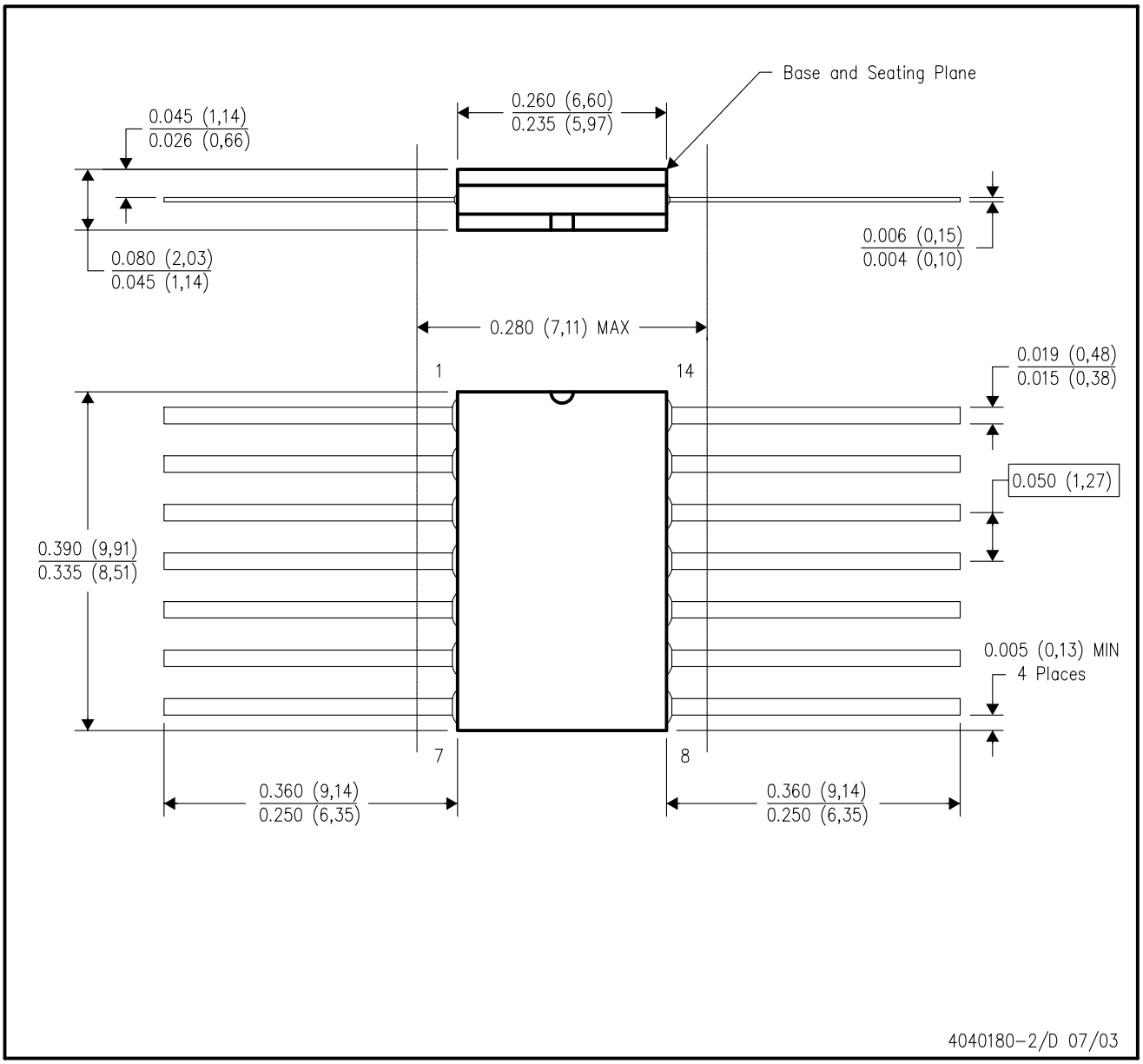
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

U (S–GDFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

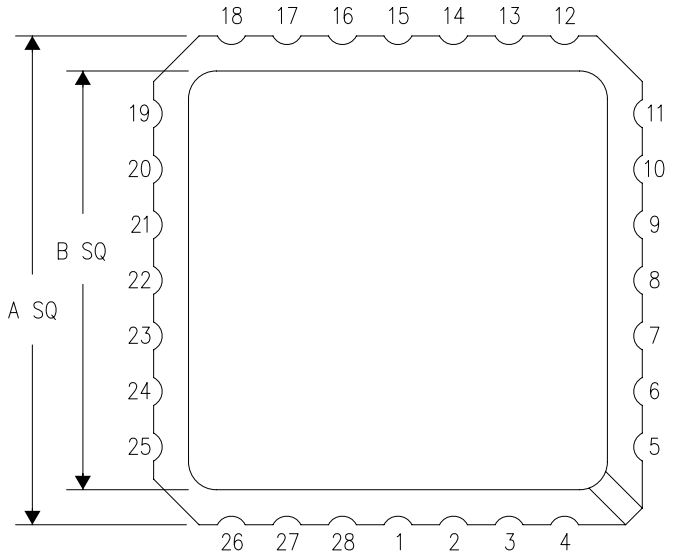
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



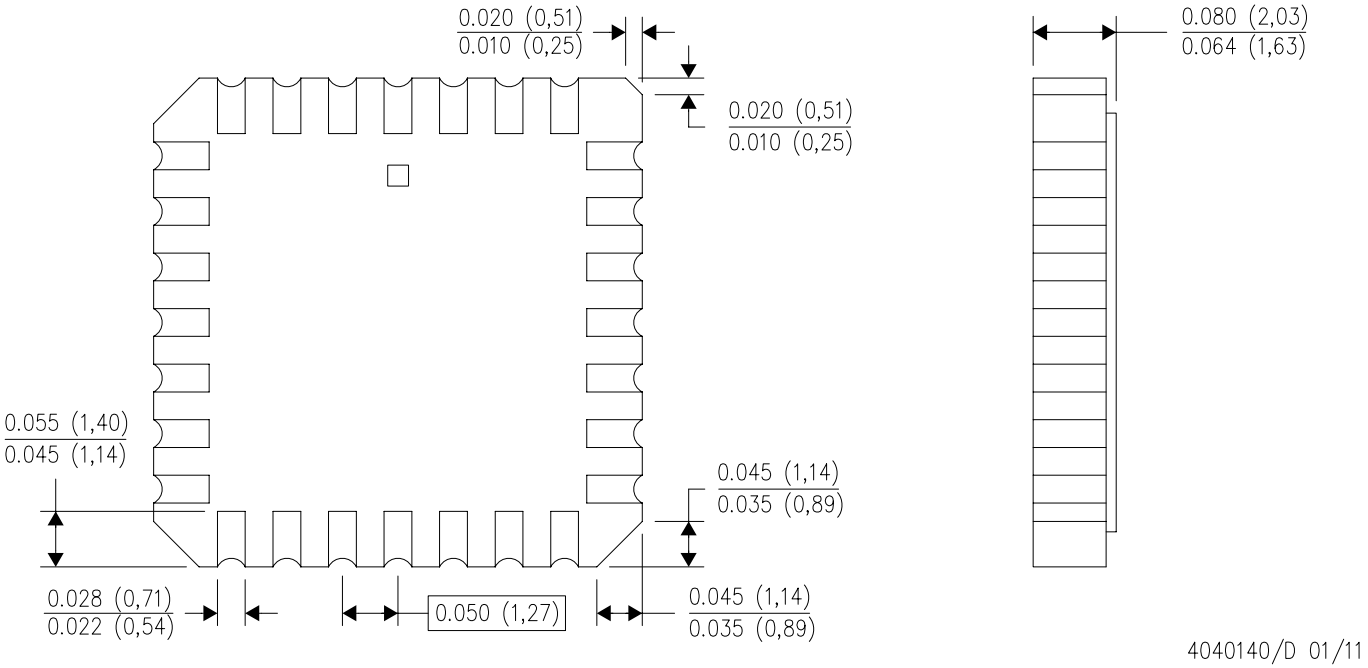
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



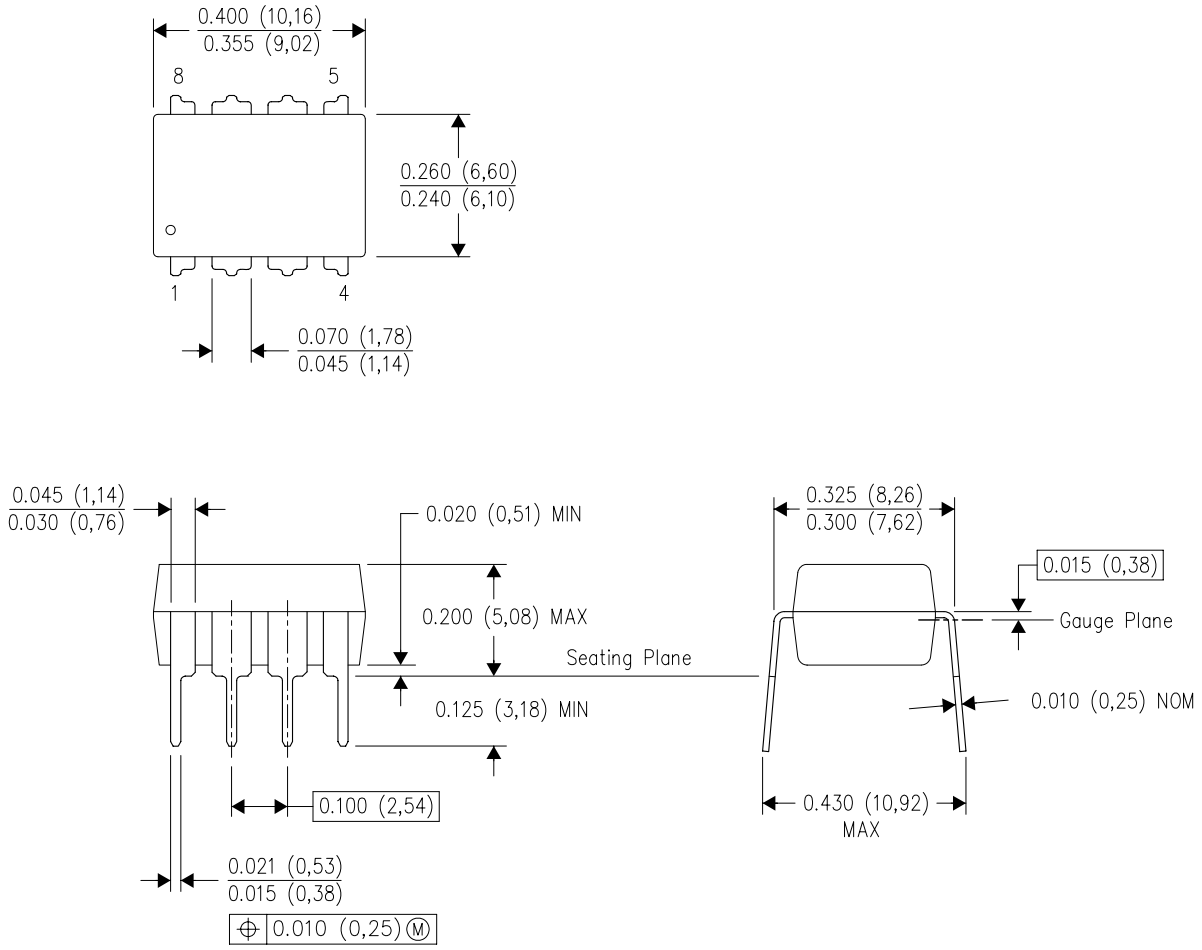
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

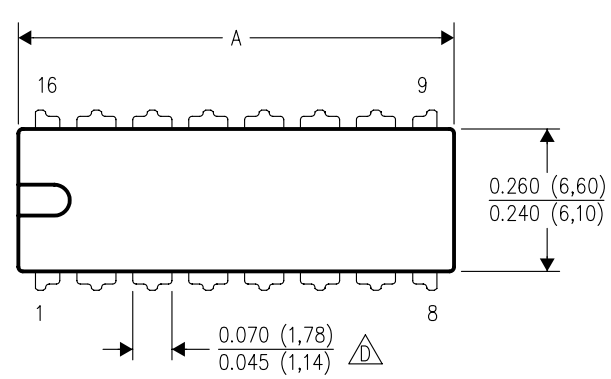


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

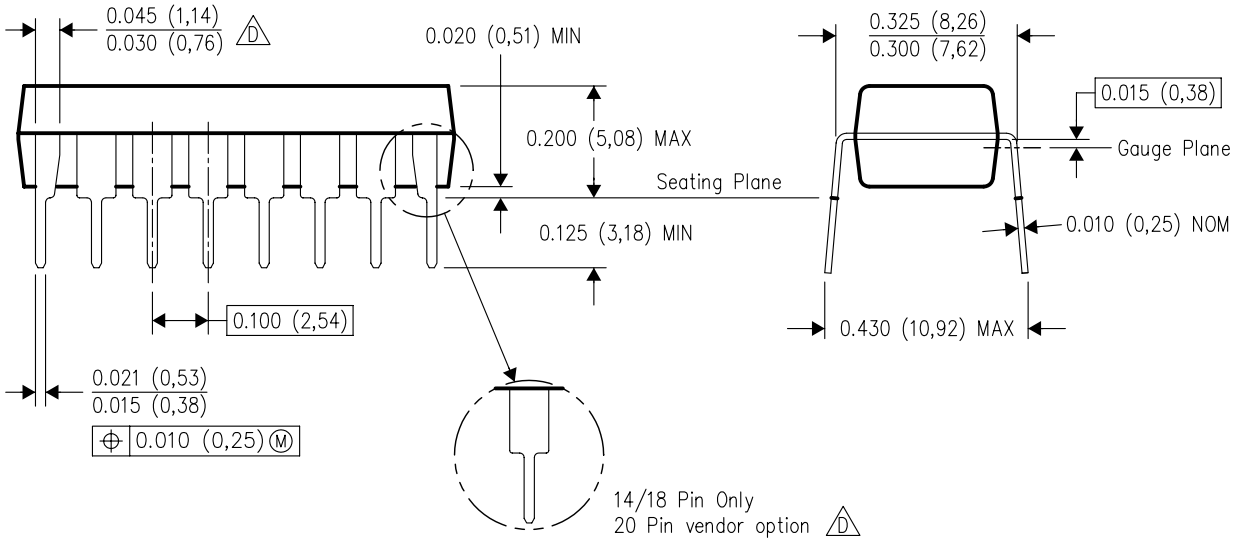
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



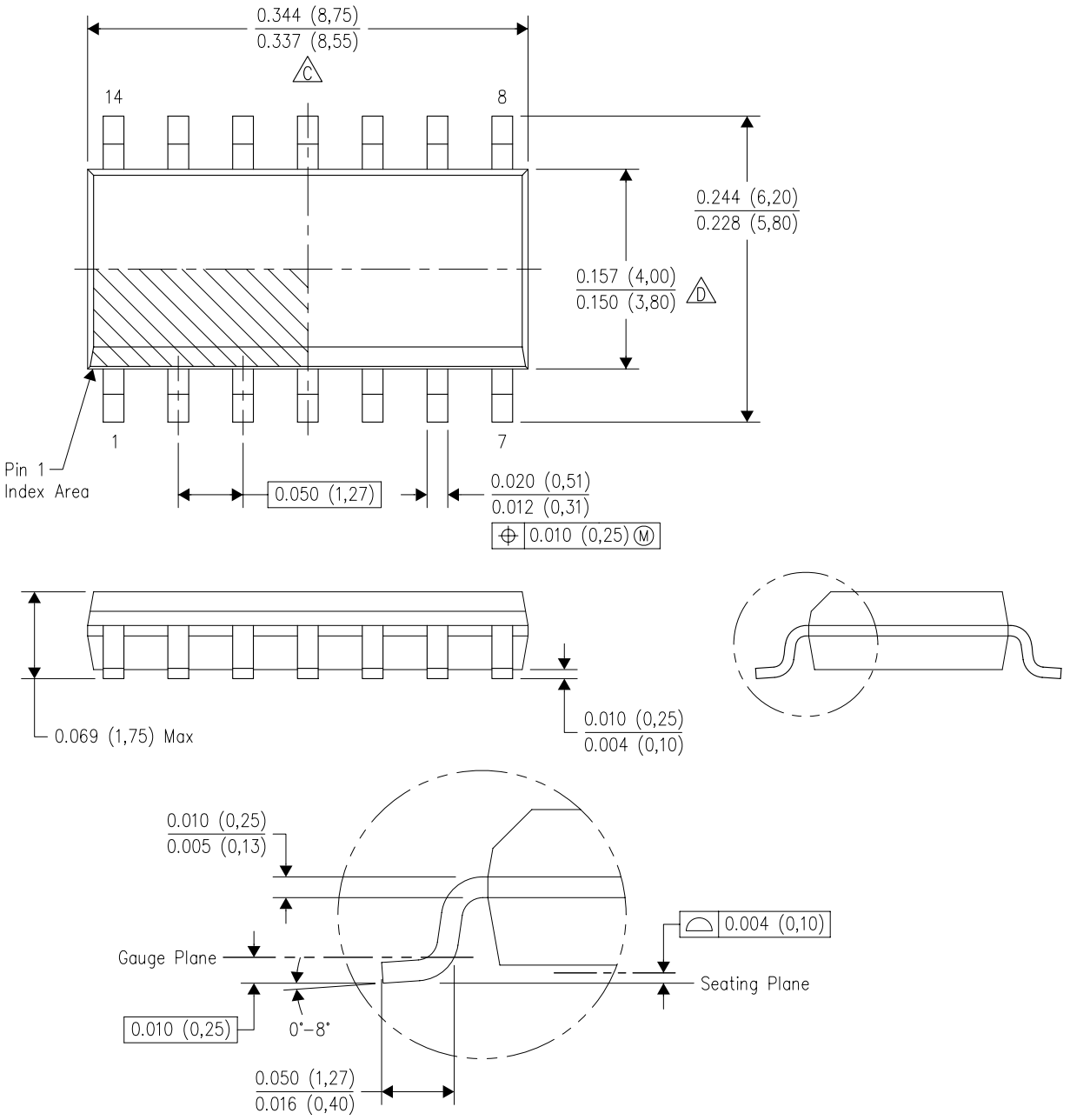
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

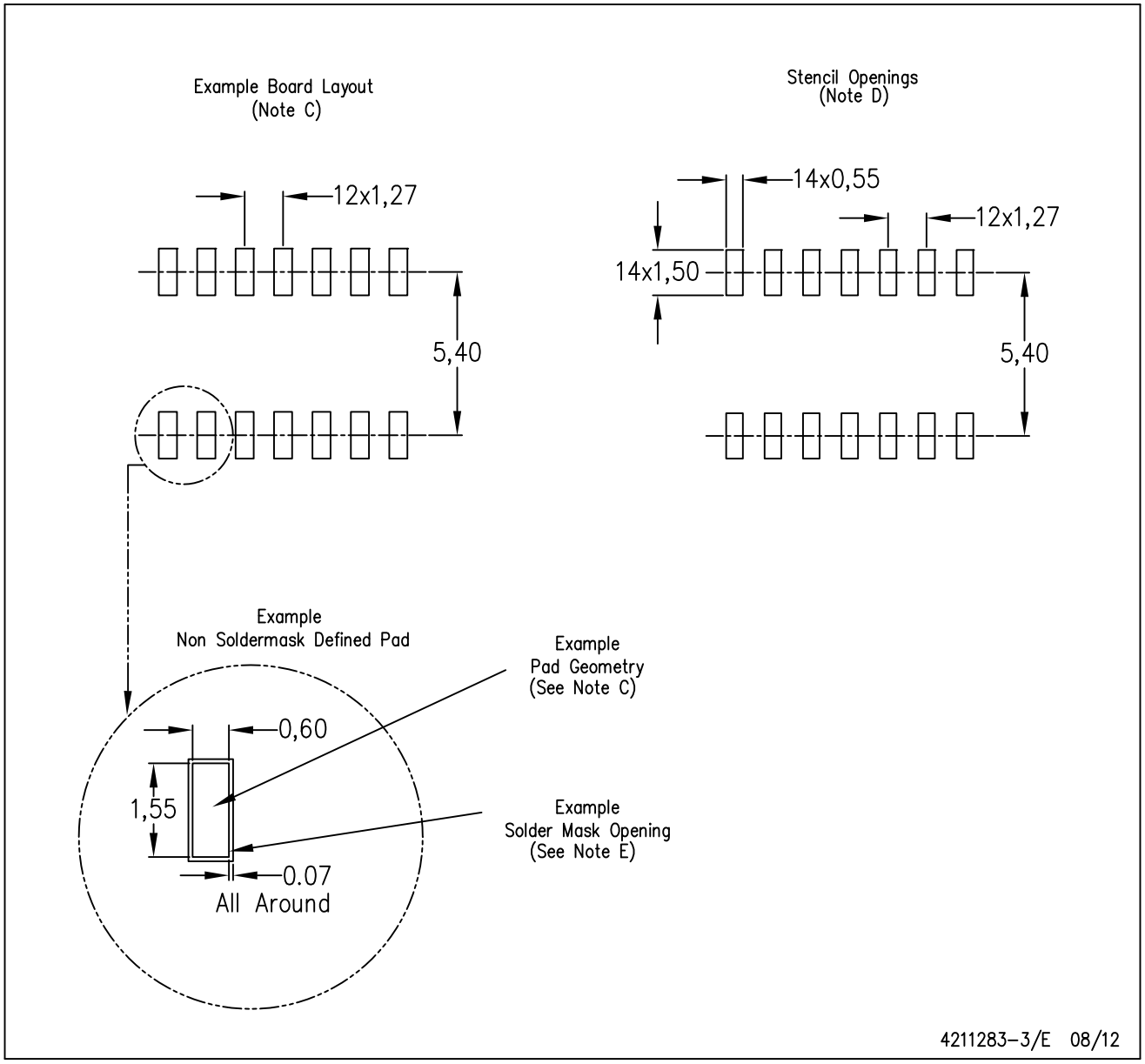
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

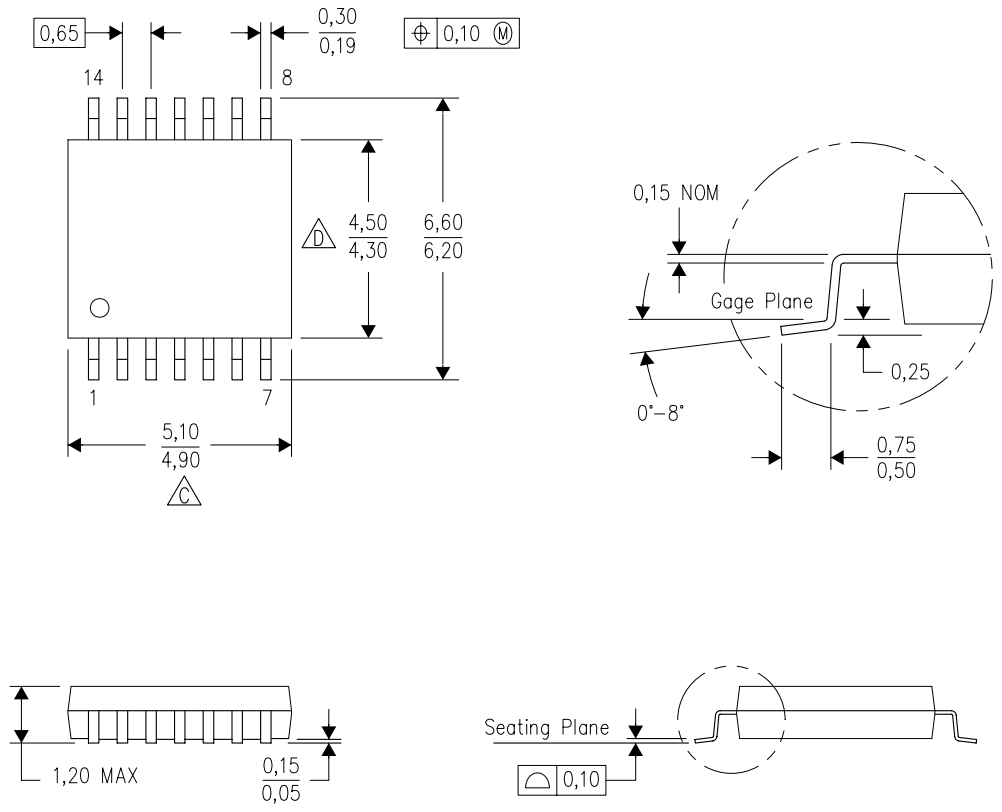
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

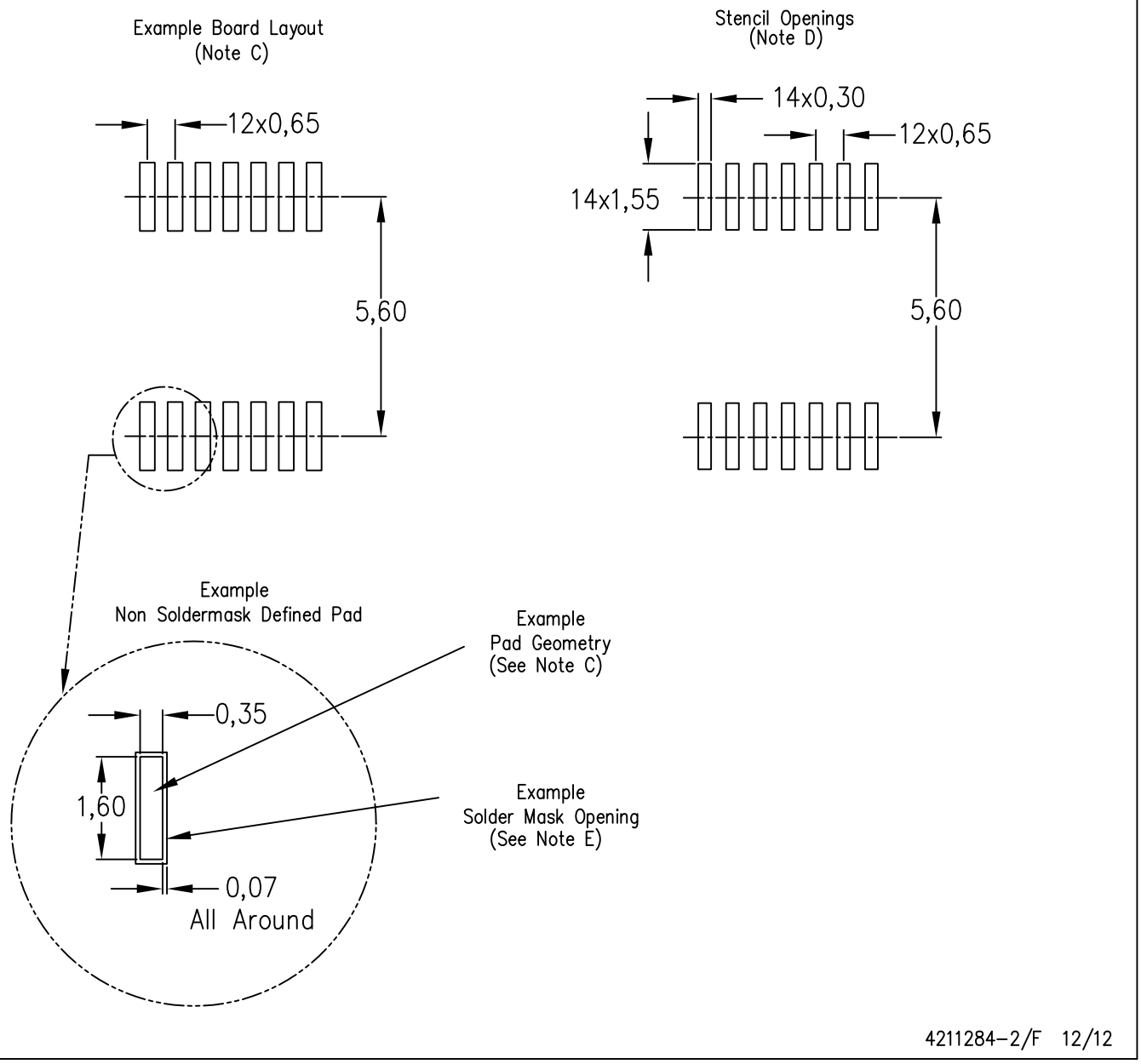
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

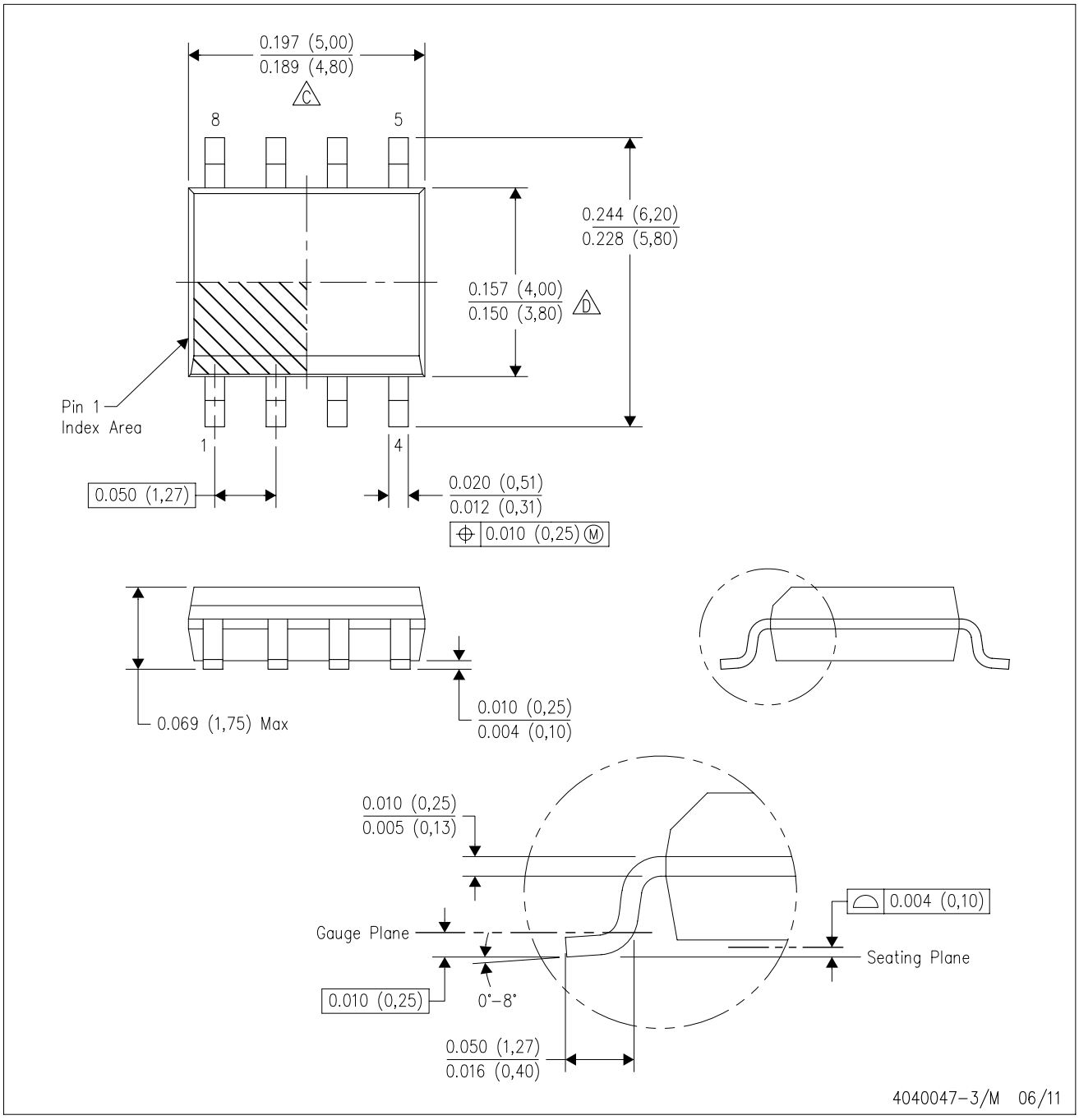
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



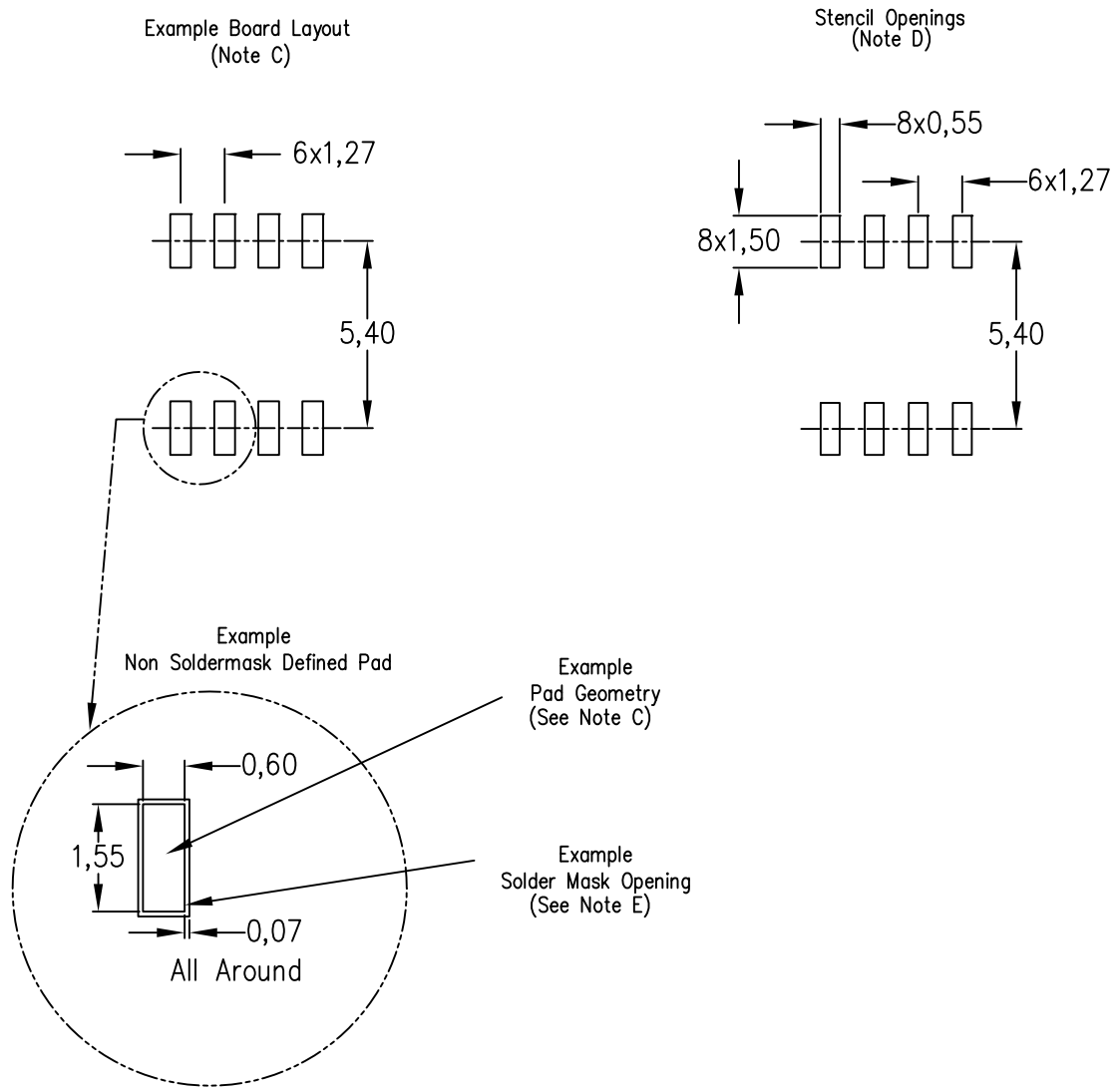
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

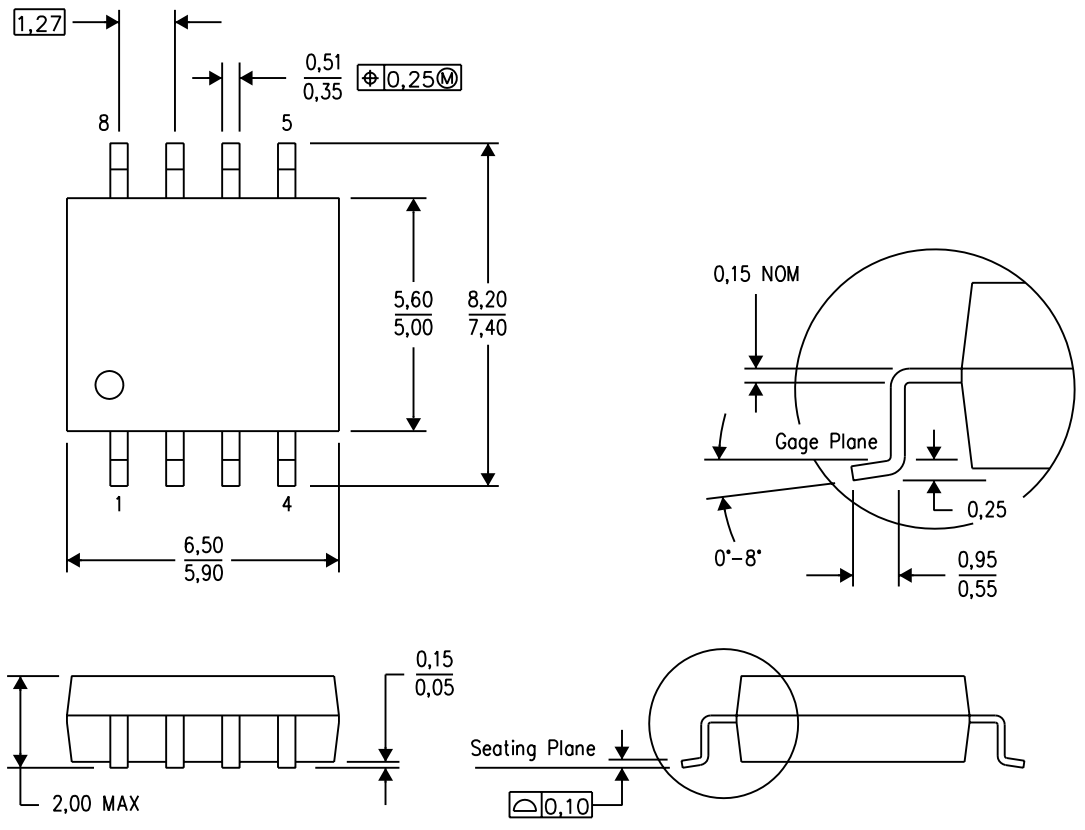
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

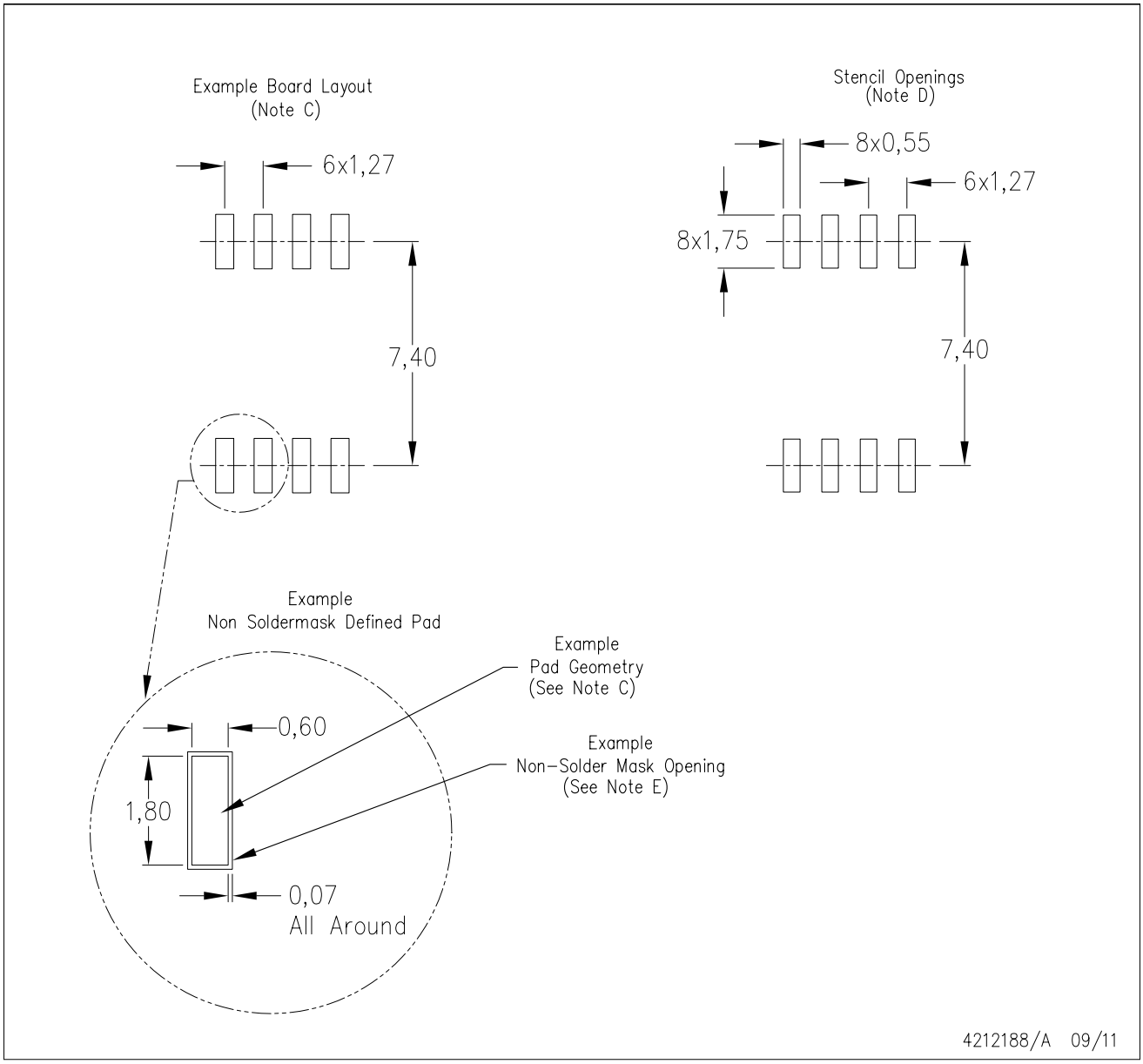
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE

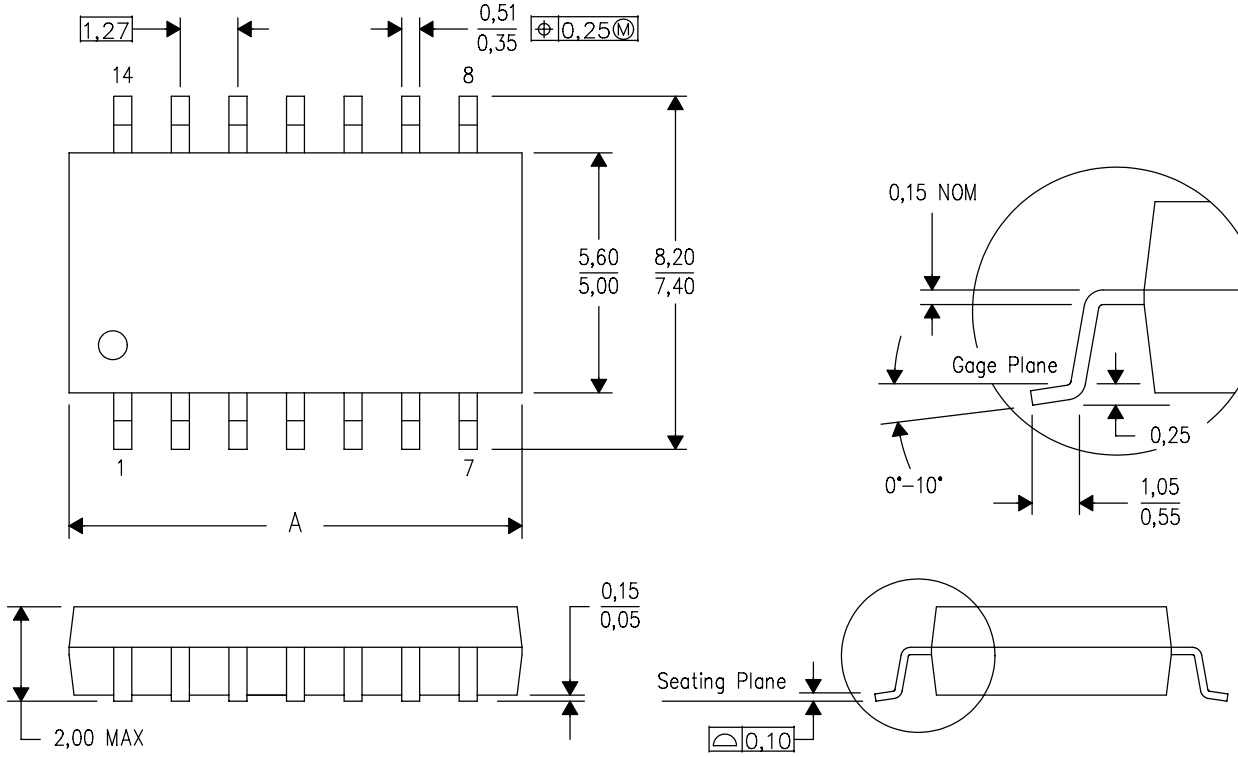


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

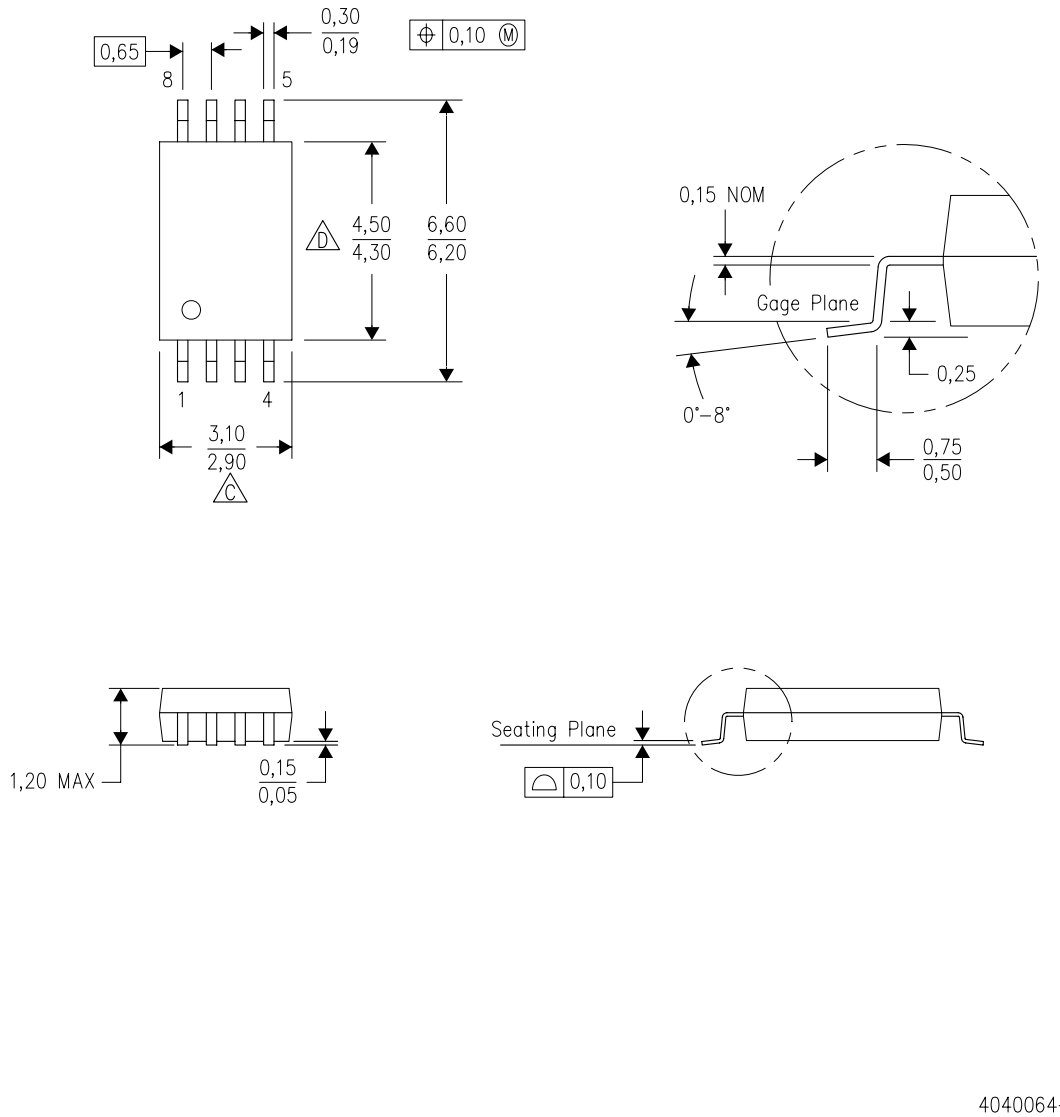


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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