

POWER MONITORING AND SWITCHING CONTROLLER FOR 3.3-V SRAM

FEATURES

- Power Monitoring and Switching for Non-Volatile Control of SRAMs
- Input Decoder Allows Control of 1 or 2 Banks of SRAM
- Write-Protect Control
- 3-V Primary Cell Input
- 3.3-V Operation
- Reset Output for System Power-On Reset
- Less than 20-ns Chip Enable Propagation Delay
- Small 16-Lead TSSOP Package

APPLICATIONS

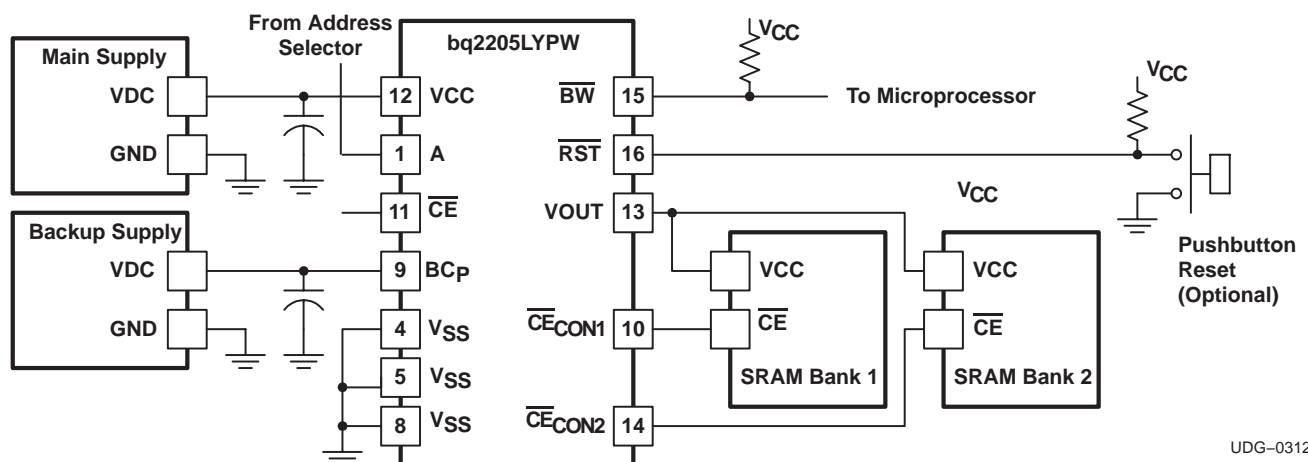
- NVSRAM Modules
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DESCRIPTION

The CMOS bq2205 SRAM non-volatile controller with reset provides all the necessary functions for converting one or two banks of standard CMOS SRAM into non-volatile read/write memory.

A precision comparator monitors the 3.3-V VCC input for an out-of-tolerance condition. When out-of-tolerance is detected, the two conditioned chip-enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs, VOUT, is switched from the VCC supply to the battery-backup supply as VCC decays. On a subsequent power-up, the VOUT supply is automatically switched from the backup supply to the VCC supply. The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system. During power-valid operation, the input decoder, A, selects one of two banks of SRAM.



UDG-03129



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

| T_A | OPERATION | PART NUMBER ⁽¹⁾ | SYMBOL |
|---------------|-----------|----------------------------|----------|
| -20°C to 70°C | 3.3 V | bq2205LYPW | bq2205LY |

(1) The PW package is available taped and reeled. Add an R suffix to the device type (i.e. bq2205LYPWR) to order quantities of 2,000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽²⁾

| | bq2205LY | UNIT |
|--|---------------------------------|------------------------|
| Input voltage range | V_{CC} , (wrt V_{SS}) | -0.3 to 6.0 |
| | BC_P , (wrt V_{SS}) | -0.3 to 4.5 |
| | all other pins, (wrt V_{SS}) | -0.3 to $V_{CC} + 0.3$ |
| Operating temperature range, T_A | -20 to 70 | °C |
| Storage temperature, T_{stg} | -55 to 125 | |
| Temperature under bias, T_{Jbias} | -40 to 85 | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 300 | |

(2) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | MIN | MAX | UNIT |
|---|------------|----------------|-------------|
| Supply voltage, V_{CC} | 3.0 | 3.6 | V |
| Supply voltage from backup cell, V_{BC} | 2.0 | 4.0 | |
| Low-level input voltage, V_{IL} | -0.3 | 0.8 | |
| High-level input voltage, V_{IH} | 2.2 | $V_{CC} + 0.3$ | |
| \overline{RST} low-level input voltage, V_{IL} | -0.3 | 0.4 | |
| \overline{RST} high-level input voltage, V_{IH} | 2.2 | $V_{CC} + 0.3$ | |
| Operating temperature range, T_A | -20 | 70 | °C |

ELECTRICAL CHARACTERISTICS(T_A = 25°C, V_{CC}(min) ≤ V_{CC} ≤ V_{CC}(max) unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|----------------------|------------------|-----------------------|------|
| VCC supply current, I _{CC} (VCC) | V _{BC} > V _{CC} (MIN) CE = low CECONX = 0 mA | | 210 | 500 | μA |
| Backup Battery Supply Current, I _{CC} (BC) | V _{BC} > V _{BC} (MIN), V _{CC} = 0 V CE = low CECONX = 0 mA | | 50 | 150 | nA |
| Output voltage (VOUT) | I(VOUT) = 80 mA, V _{CC} > V(SO) | V _{CC} -0.3 | | | V |
| | I(VOUT) = 100 μA, V _{CC} < V(SO) | V _{BC} -0.3 | | | |
| Power fail detect voltage, V _{PFD} | | 2.85 | 2.9 | 2.95 | |
| Supply switch-over voltage, V _{SO} | V _{BC} > V(PFD) | | V _{PFD} | | |
| | V _{BC} < V(PFD) | | V _{BC} | | |
| RST output voltage | I(RST) = 1 mA | | | 0.4 | V |
| BW output voltage | I(BW) = 1 mA | | | 0.4 | |
| Input leakage current on A and CE pins | | -1 | | 1 | |
| V _{oh} CE _{con1,2} | I _{oh} = 0.5 mA | | 2.4 | | V |
| V _{ol} CE _{con1,2} | I _{ol} = 2.0 mA | | 0.4 | | |
| Battery warning level V _{BW} | (1) | | | 0.677xV _{CC} | |
| Capacitance | | | | | |
| Output capacitance | VOUT = 0 V | | | 7 | pF |
| Input capacitance | VOUT = 0 V | | | 5 | |
| Power-Down and Power-Up Timing, Refer to Figure 1 through 3 | | | | | |
| VCC slew rate fall time, t _F | 3.0 V to 0.0 V | 300 | | | μs |
| VCC slew rate rise time, t _R | V _{SO} to V _{PFD} (max) | 100 | | | |
| V _{PFD} to RST active, t _{RST} (reset active timeout period) | | 30 | | 85 | ms |
| Chip-enable recovery time, t _{CER} | (2) | 30 | | 85 | |
| Chip-enable propagation delay time to external SRAM, t _{CED} | See Figure 2 | | 15 | 25 | ns |
| Push-button low time, t _{PBL} | RST pin | | 1 | | μs |

(1) Battery warning level is detected on power up and the BW pin is latched at t_{CER} time after V_{CC} passes through V_{PFD} on power up.(2) Time during which external SRAM is write protected after V_{CC} passes through V_{PFD} on power up.

AC TEST CONDITIONS, INPUT PULSE LEVELS $0\text{ V} \leq V_{IN} \leq 3\text{ V}$, $t_R = t_F = 5\text{ NS}$

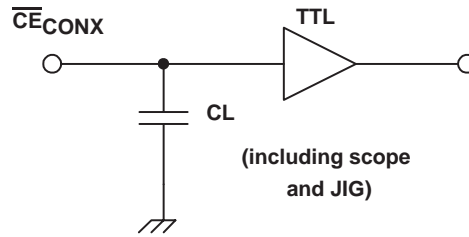


Figure 1. Output Load

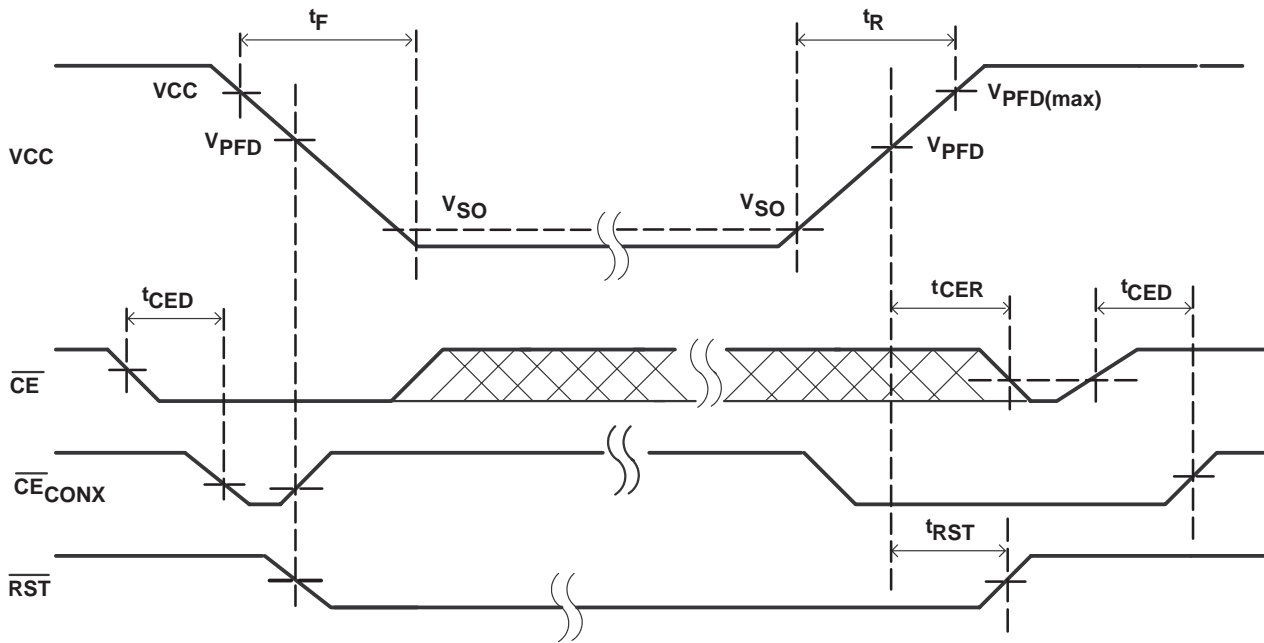


Figure 2. Power-Down/Power-Up Timing Diagram

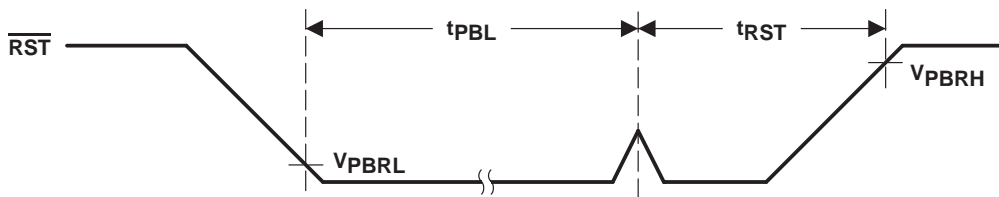
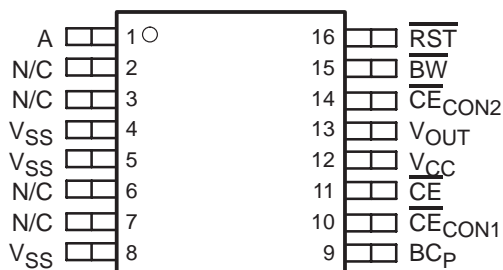


Figure 3. Push-Button Reset Timing

TERMINAL FUNCTIONS

| NAME | TERMINAL | I/O | DESCRIPTION |
|----------------------------|------------|-----|--|
| | bq2205LY | | |
| A | 1 | I | SRAM bank select input |
| BC _P | 9 | I | Backup supply input |
| $\overline{\text{BW}}$ | 15 | O | Battery warning output (open-drain) |
| $\overline{\text{CE}}$ | 11 | I | Chip enable input (active low) |
| $\overline{\text{CECON1}}$ | 10 | O | Conditioned chip enable output 1 |
| $\overline{\text{CECON2}}$ | 14 | O | Conditioned chip enable output 2 |
| N/C | 2, 3, 6, 7 | – | No connect. These pins must be left floating. |
| $\overline{\text{RST}}$ | 16 | O | Power-up reset to system CPU output (open-drain) |
| V _{CC} | 12 | I | Main supply input |
| V _{OUT} | 13 | O | SRAM supply output |
| V _{SS} | 4, 5, 8 | – | Ground input |

PW PACKAGE
(TOP VIEW)

N/C no connection

FUNCTIONAL DESCRIPTION

Two banks of CMOS static RAM can be battery-backed using the VOUT and conditioned chip-enable output pins from the bq2205. As the voltage input VCC slews down during a power failure, the two-conditioned chip enable outputs, \overline{CE}_{CON1} and \overline{CE}_{CON2} , are forced inactive independent of the chip enable input, \overline{CE} . This activity unconditionally write-protects the external SRAM as VCC falls to an out-of-tolerance threshold V_{PFD} . As the supply continues to fall past V_{PFD} , an internal switching device forces VOUT to the backup energy source. \overline{CE}_{CON1} and \overline{CE}_{CON2} are held high by the VOUT energy source.

During power-up, VOUT is switched back to the 3.3-V supply as VCC rises above the backup cell input voltage sourcing VOUT. Outputs \overline{CE}_{CON1} and \overline{CE}_{CON2} are held inactive for time t_{CER} after the power supply has reached V_{PFD} , independent of the \overline{CE} input, to allow for processor stabilization.

During power-valid operation, the \overline{CE} input is passed through to one of the two \overline{CE}_{CONx} outputs with a propagation delay of less than t_{CED} . The \overline{CE} input is output on one of the two \overline{CE}_{CONx} output pins; depending on the level of bank select input A. See truth table below.

Table 1. Truth Table

| INPUT | | OUTPUT | |
|-----------------|---|------------------------|------------------------|
| \overline{CE} | A | \overline{CE}_{CON1} | \overline{CE}_{CON2} |
| H | x | H | H |
| L | L | L | H |
| L | H | H | L |

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Non-volatility and decoding are achieved by hardware hookup as shown in the application diagram.

The \overline{RST} output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when \overline{RST} returns inactive.

BATTERY BACKUP INPUT

Backup energy source, BC_P input is provided on the bq2205 for use with an external primary cell. The primary cell input is designed to accept any 3-V primary battery (non-rechargeable), typically some type of lithium chemistry.

Power-Down and Power-Up Cycle

The bq2205 continuously monitors VCC for out-of-tolerance. During a power failure, when VCC falls below V_{PFD} , the bq2205 write-protects the external SRAM. The power source is switched to BC_P when V_{CC} is less than V_{PFD} and BC_P is greater than V_{PFD} , or when V_{CC} is less than BC_P and BC_P is less than V_{PFD} . When VCC is above V_{PFD} , the power source is V_{CC} . Write-protection continues for t_{CER} time after VCC rises above V_{PFD} .

An external CMOS static RAM is battery-backed using the VOUT and chip enable output pins from the bq2205. As the voltage input V_{CC} slews down during a power failure, the chip enable output, \overline{CE}_{CONx} , is forced inactive independent of the chip enable input \overline{CE} .

As the supply continues to fall past V_{PFD} , an internal switching device forces VOUT to the external backup energy source. \overline{CE}_{CONx} is held high by the VOUT energy source.

FUNCTIONAL DESCRIPTION

During power up, VOUT is switched back to the main supply as VCC rises above the backup cell input voltage sourcing VOUT. If $V_{PFD} < BC_P$ on the bq2205 the switch to the main supply occurs at V_{PFD} . \overline{CE}_{CONx} is held inactive for time t_{CER} after the power supply has reached V_{PFD} , independent of the \overline{CE} input, to allow for processor stabilization.

Power-On Reset

The bq2205 provides a power-on reset, which pulls the \overline{RST} pin low on power down and remains low on power up for t_{RST} after V_{CC} passes V_{PFD} . With valid battery voltage on BC_P , \overline{RST} remains valid for $V_{CC} = V_{SS}$. The pull-up resistor on this pin should not exceed 10 k Ω if a push button reset is used.

Battery Low Warning

The bq2205 checks the battery voltage on power-up. The threshold for the battery warning comparator is V_{BW} , and a low level is sensed after power valid on each power up and latched after t_{CER} time. The latched value is presented at \overline{BW} pin where a low indicates a low battery.

APPLICATION INFORMATION

PCB LAYOUT INFORMATION

It is important to pay special attention to the PCB layout. The following provides some guidelines:

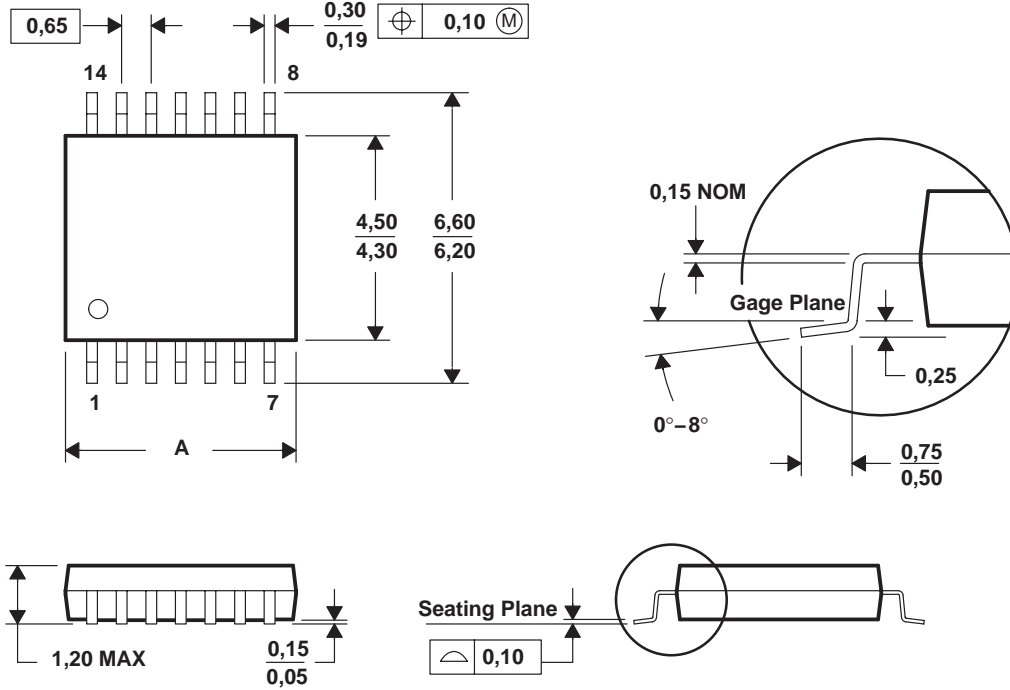
- To obtain optimal performance, the decoupling capacitor from input terminals to V_{SS} should be placed as close as possible to the bq2205, with short trace runs to both signal and V_{SS} pins.
- All low-current V_{SS} connections should be kept separate from the high-current paths from the inputs supplies. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.

MECHANICAL DATA

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---------------|------|------|------|------|------|------|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| BQ2205LYPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2205LYPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2205LYPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2205LYPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ2205LYPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



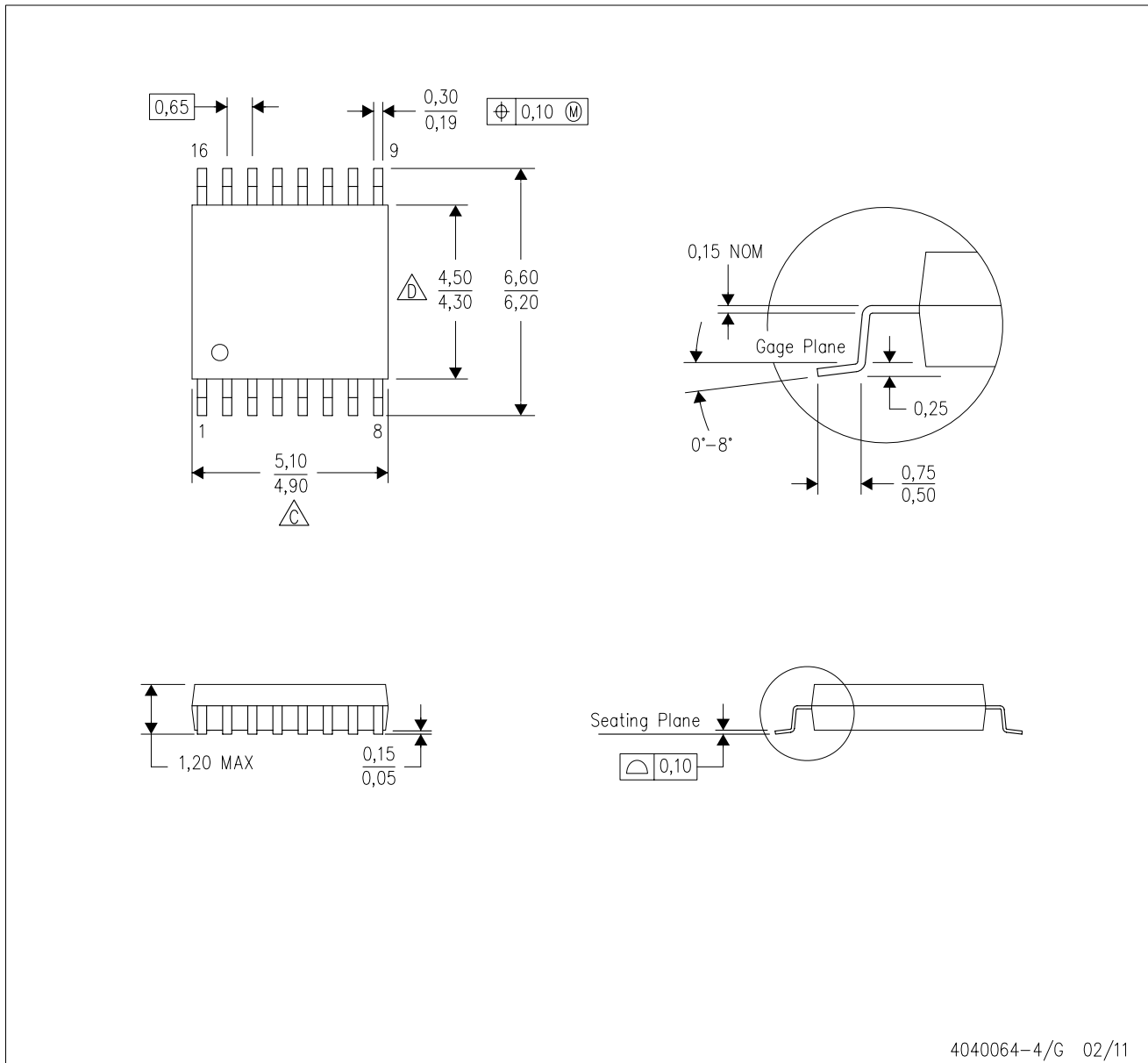
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ2205LYPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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