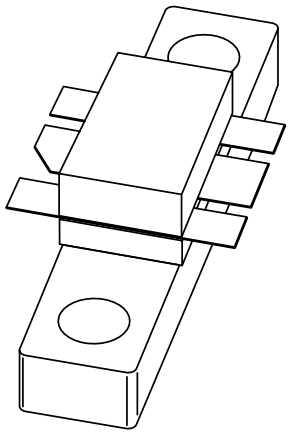
DATA SHEET



BLF544
UHF power MOS transistor

Product specification
Supersedes data of 1998 Jan 21

2003 Sep 18

Philips
Semiconductors

PHILIPS

UHF power MOS transistor BLF544

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

APPLICATIONS

- Communication transmitters in the UHF frequency range.

DESCRIPTION

N-channel enhancement mode vertical D-MOS power transistor encapsulated in a 6-lead, SOT171A flange package with a ceramic cap. All leads are isolated from the flange.
A marking code showing gate-source voltage (V_{GS}) information is provided for matched pair applications.

PINNING - SOT171A

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

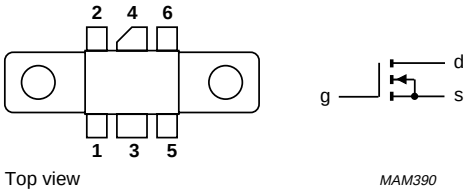


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	20	>11	>50
CW, class-B	960	28	20	typ. 7	typ. 50

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

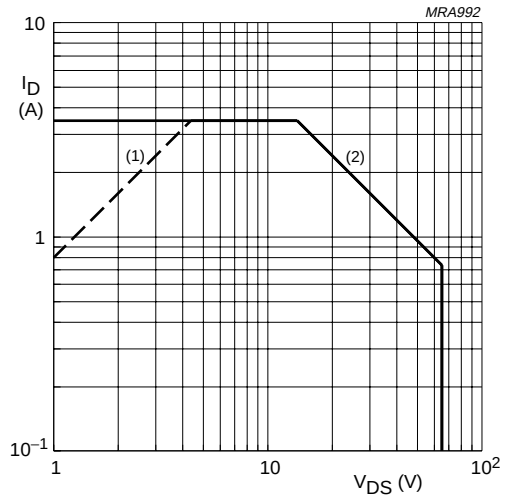
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	3.5	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	48	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

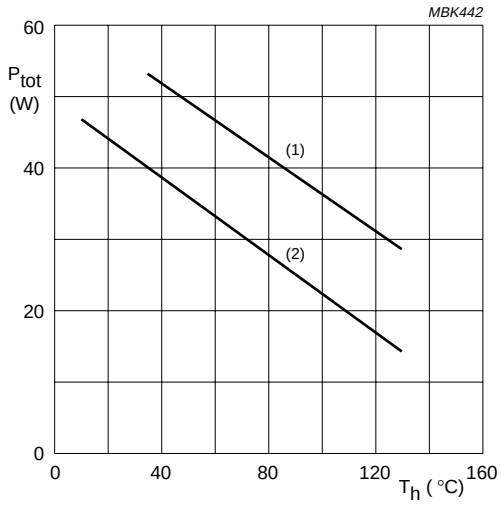
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	3.7	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4	K/W



(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power derating curves.

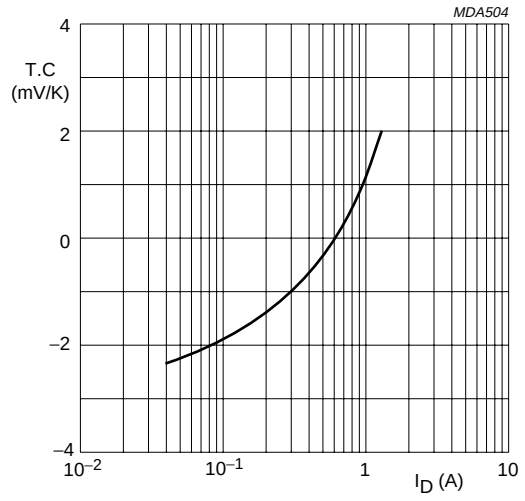
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	µA
V_{GSth}	gate-source threshold voltage	I_D = 40 mA; V_{DS} = 10 V	1	–	4	V
ΔV_{GSth}	gate-source voltage difference of matched pairs	I_D = 40 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.2 A; V_{DS} = 10 V	600	900	–	mS
R_{DSon}	drain-source on-state resistance	I_D = 1.2 A; V_{GS} = 10 V	–	0.85	1.25	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	4.8	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	32	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	24	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	6.4	–	pF

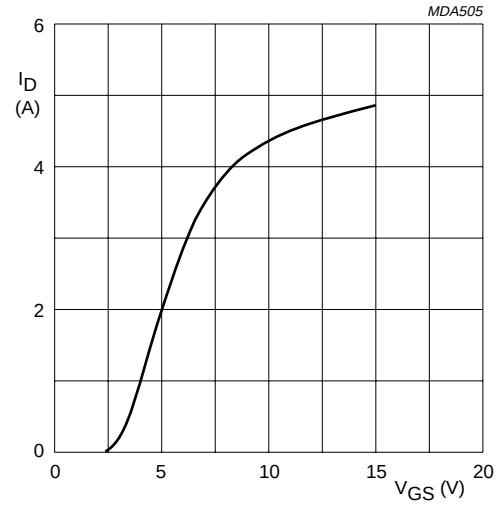
V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			



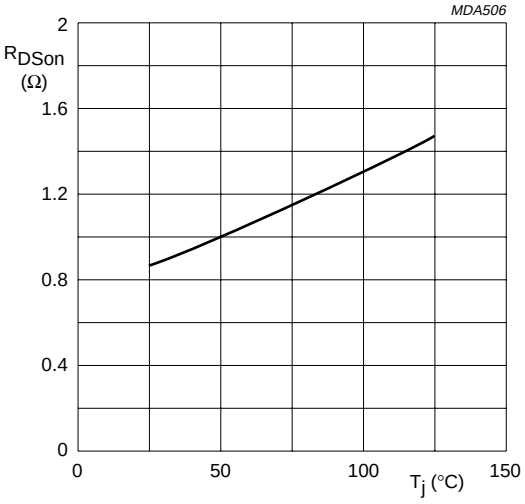
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



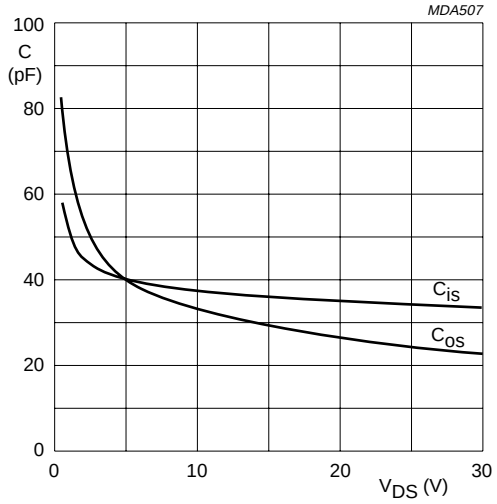
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values.



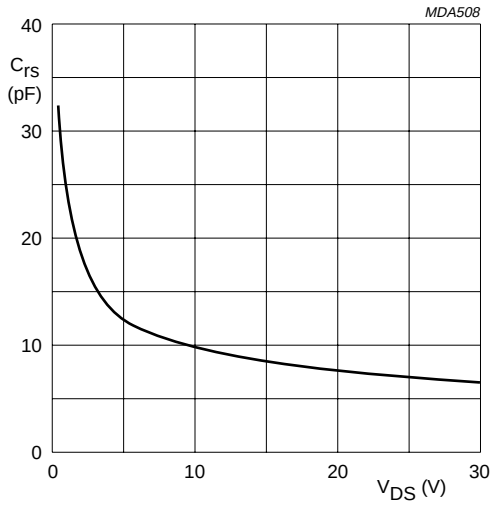
I_D = 1.2 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

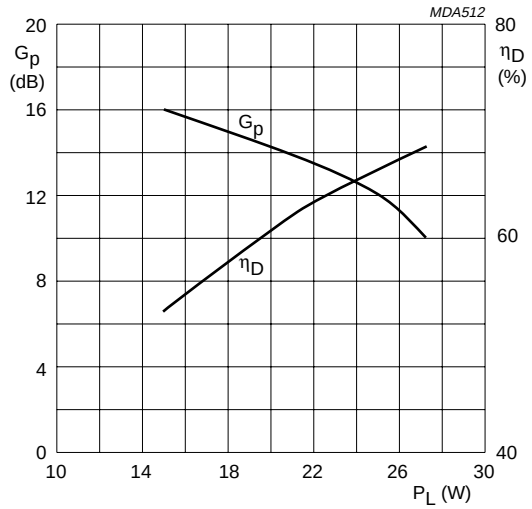
APPLICATION INFORMATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W unless otherwise specified.
RF performance in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	40	20	>11 typ. 14	>50 typ. 60
CW, class-B	960	28	40	20	typ. 7	typ. 50
CW, class-B	960	24	40	15	typ. 7	typ. 50

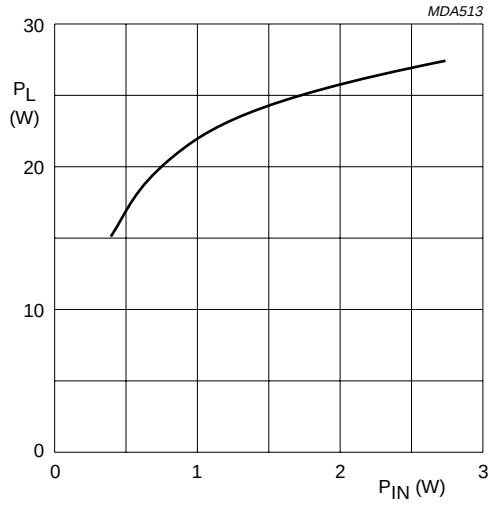
Ruggedness in class-B operation

The BLF544 is capable of withstanding a full load mismatch corresponding to VSWR = 50 : 1 through all phases under the following conditions: V_{DS} = 28 V; f = 500 MHz at rated output power.



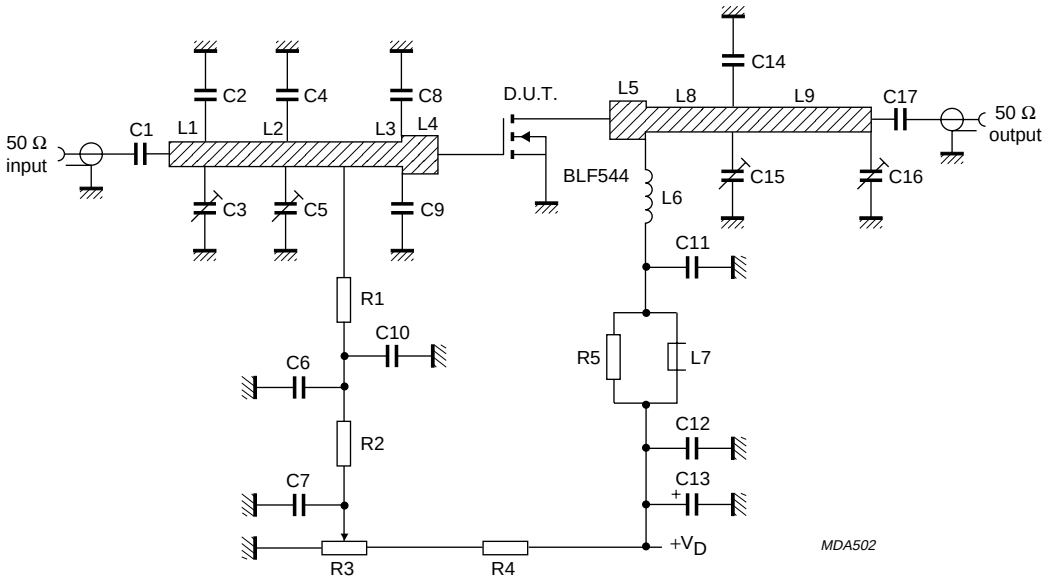
Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA;
Z_L = 4.3 + j6.3 Ω; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power; typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA;
Z_L = 4.3 + j6.3 Ω; f = 500 MHz.

Fig.10 Load power as a function of input power; typical values.



f = 500 MHz.

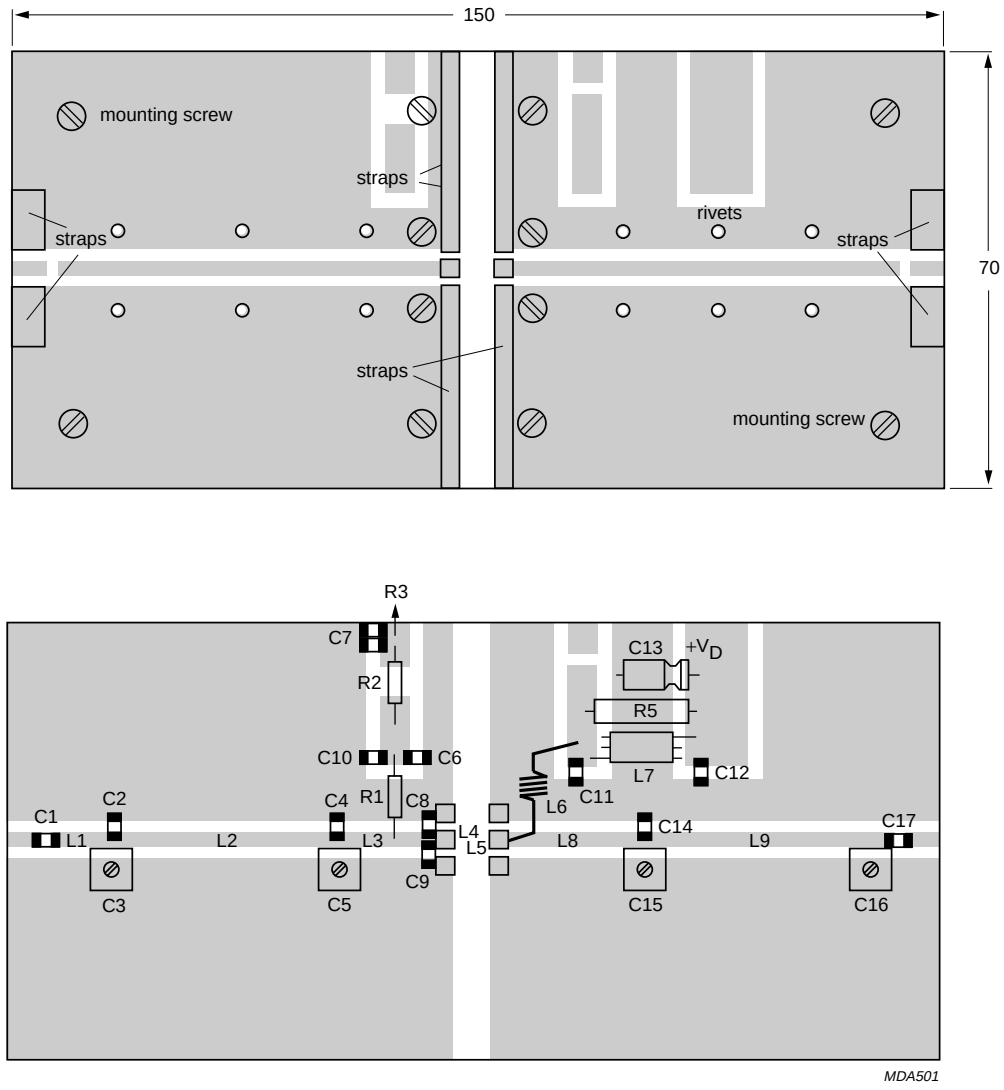
Fig.11 Test circuit for class-B operation.

List of components (see Figs 11 and 12**).**

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C11, C17	multilayer ceramic chip capacitor; note 1	390 pF; 500 V		
C2	multilayer ceramic chip capacitor; note 2	16 pF; 50 V		
C3, C5	film dielectric trimmer	2 to 9 pF		2222 809 09002
C4	multilayer ceramic chip capacitor; note 2	27 pF; 50 V		
C7	multilayer ceramic chip capacitor	2 × 100 nF in parallel; 50 V		2222 852 47104
C8, C9	multilayer ceramic chip capacitor; note 2	39 pF		
C10, C12	multilayer ceramic chip capacitor	100 nF; 50 V		2222 852 47104
C13	electrolytic capacitor	4.7 μF; 63 V		2222 030 38478
C14	multilayer ceramic chip capacitor; note 1	20 pF; 500 V		
C15, C16	film dielectric trimmer	2 to 18 pF		2222 809 09003
L1	stripline note 3	50 Ω	9.5 × 2.5 mm	
L2	stripline note 3	50 Ω	34.5 × 2.5 mm	
L3	stripline note 3	50 Ω	17.5 × 2.5 mm	
L4, L5	stripline note 3	42 Ω	3 × 3 mm	
L6	4 turns enamelled 0.8 mm copper wire	31 nH	length 7.5 mm int. dia. 3 mm leads 2 × 5 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L8	stripline note 3	50 Ω	22 × 2.5 mm	
L9	stripline note 3	50 Ω	39.5 × 2.5 mm	
R1, R2	0.4 W metal film resistor	1 kΩ		2322 151 11002
R3	10 turns cermet potentiometer	50 kΩ		
R4	0.4 W metal film resistor	140 kΩ		2322 151 11404
R5	1 W metal film resistor	10 Ω		2322 153 51009

Notes

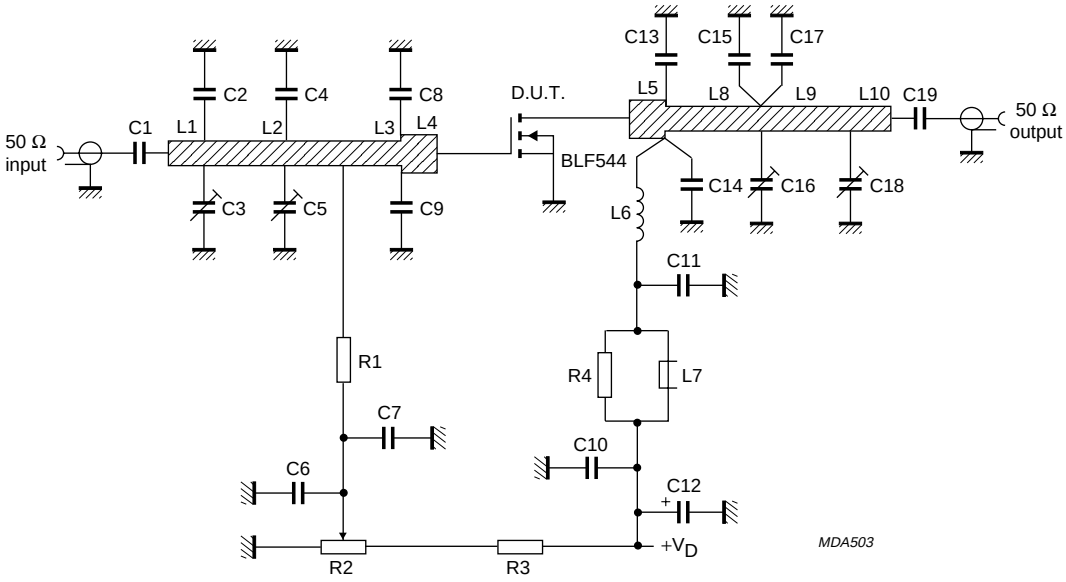
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE (ε_r = 2.2); thickness $^1/_{32}$ inch.



Dimensions in mm.

The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.



f = 960 MHz.

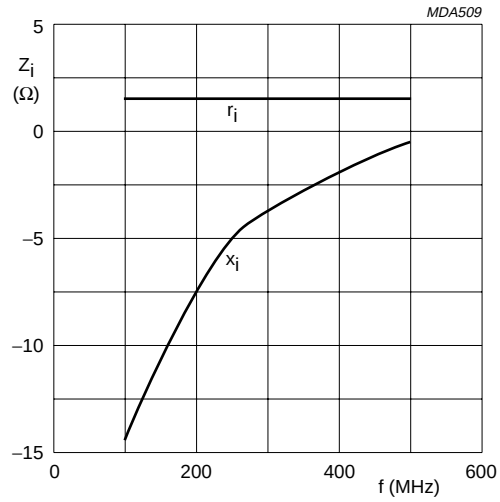
Fig.13 Test circuit for class-B operation.

List of components (see Figs 12 and 13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	multilayer ceramic chip capacitor; note 1	68 pF; 500 V		
C2	multilayer ceramic chip capacitor; note 2	1.6 pF; 50 V		
C3, C5, C16, C18	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C4	multilayer ceramic chip capacitor; note 2	1 pF; 50 V		
C6	multilayer ceramic chip capacitor	10 nF; 50 V		2222 852 47103
C7, C11	multilayer ceramic chip capacitor; note 1	56 μF; 500 V		
C8, C9, C15, C17	multilayer ceramic chip capacitor; note 2	6.8 μF; 50 V		
C10	multilayer ceramic chip capacitor	100 nF; 50 V		2222 852 47104
C12	electrolytic capacitor	4.7 μF; 63 V		2222 030 38478
C13	multilayer ceramic chip capacitor; note 2	16 pF; 50 V		
C14	multilayer ceramic chip capacitor; note 2	18 pF; 50 V		
C19	multilayer ceramic chip capacitor; note 1	62 pF; 500 V		
L1, L8	stripline; note 3	50 Ω	6 × 2.5 mm	
L2	stripline; note 3	50 Ω	38 × 2.5 mm	
L3	stripline; note 3	50 Ω	17.5 × 2.5 mm	
L4, L5	stripline; note 3	42 Ω	3 × 3 mm	
L6	2 turns enamelled 1 mm copper wire	16 nH	length 3.4 mm int. dia. 3 mm leads 2 × 5 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L9	stripline; note 3	50 Ω	21 × 2.5 mm	
L10	stripline; note 3	50 Ω	34.5 × 2.5 mm	
R1	0.4 W metal film resistor	15 kΩ		2322 151 11473
R2	10 turns potentiometer	50 kΩ		
R3	0.4 W metal film resistor	140 kΩ		2322 151 11404
R4	0.4 W metal film resistor	10 Ω		2322 153 51009

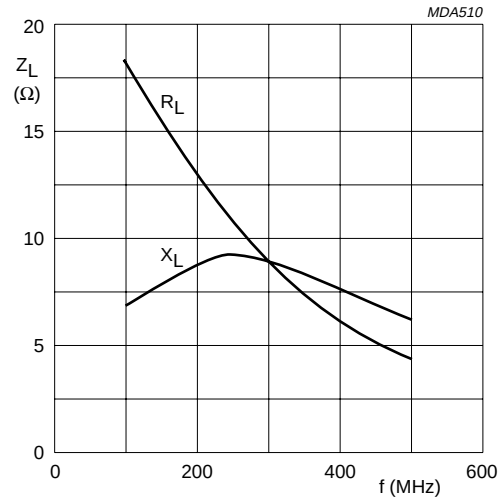
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed-circuit board with glass microfibre reinforced PTFE (ε_r = 2.2); thickness $^1/_{32}$ inch.



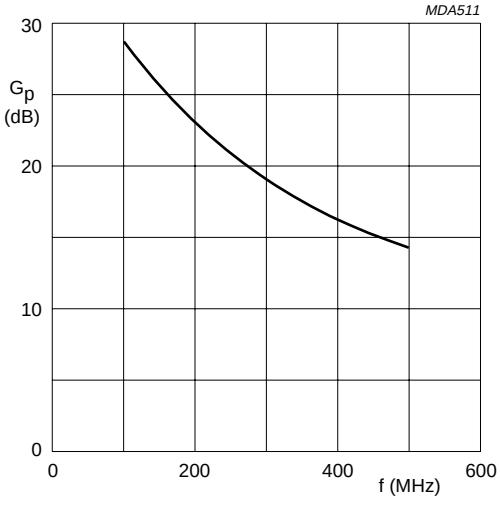
Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA; P_L = 20 W.

Fig.14 Input impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA; P_L = 20 W.

Fig.15 Load impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA; P_L = 20 W.

Fig.16 Power gain as a function of frequency; typical values.

Optimum input and load impedances

Optimum input impedance: 1.2 + j4.8 Ω.
Optimum load impedance: 2.6 – j3.1 Ω.
Conditions: class-B operation; V_{DS} = 24 V;
I_{DQ} = 40 mA; f = 960 MHz; P_L = 15 W; typical values.

BLF544 scattering parameters

V_{DS} = 28 V; I_D = 40 mA; note 1

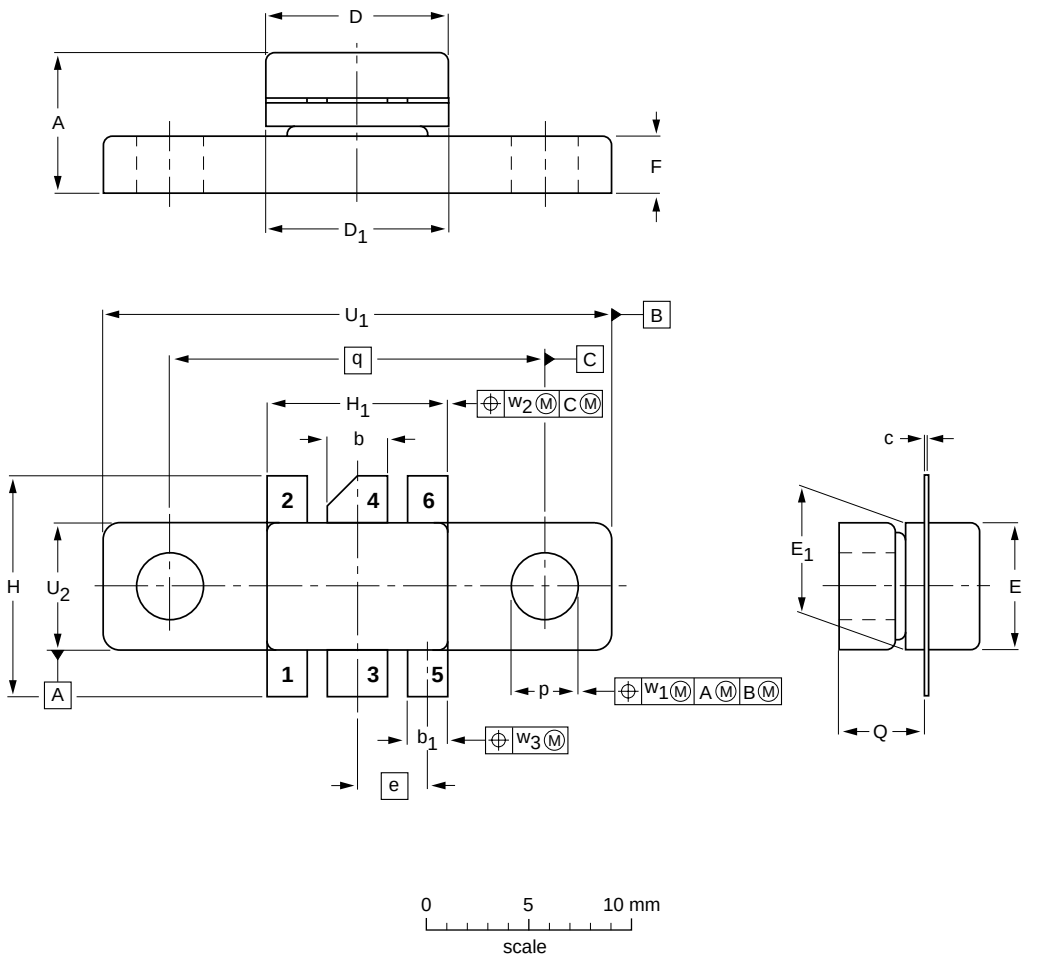
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	$\|s_{11}\|$	$\angle\Phi$	$\|s_{21}\|$	$\angle\Phi$	$\|s_{12}\|$	$\angle\Phi$	$\|s_{22}\|$	$\angle\Phi$
5	0.99	–14.0	13.60	171.0	0.02	81.0	0.89	–12.8
10	0.98	–27.6	13.20	162.0	0.04	72.4	0.87	–25.3
20	0.93	–52.0	11.90	146.0	0.07	57.1	0.82	–48.0
30	0.88	–72.0	10.30	134.0	0.09	44.8	0.77	–66.6
40	0.84	–87.7	8.93	124.0	0.10	35.2	0.72	–81.3
50	0.81	–100.0	7.75	116.0	0.11	27.7	0.68	–93.0
60	0.79	–110.0	6.78	110.0	0.12	21.6	0.66	–102.0
70	0.77	–118.0	6.00	104.0	0.12	16.7	0.64	–109.0
80	0.76	–124.0	5.36	99.8	0.12	12.5	0.63	–115.0
90	0.75	–129.0	4.82	95.9	0.12	8.9	0.62	–120.0
100	0.75	–133.0	4.37	92.3	0.13	5.7	0.61	–124.0
125	0.74	–141.0	3.53	84.7	0.13	–1.1	0.61	–131.0
150	0.74	–147.0	2.94	78.3	0.13	–6.6	0.61	–137.0
175	0.74	–151.0	2.50	72.6	0.12	–11.5	0.62	–140.0
200	0.75	–154.0	2.16	67.5	0.12	–15.8	0.64	–143.0
250	0.77	–159.0	1.67	58.4	0.12	–23.3	0.67	–148.0
300	0.78	–163.0	1.33	50.4	0.11	–29.7	0.70	–151.0
350	0.80	–167.0	1.09	43.1	0.10	–35.3	0.73	–154.0
400	0.82	–169.0	0.91	36.6	0.10	–40.3	0.75	–157.0
450	0.84	–172.0	0.77	30.6	0.09	–44.7	0.78	–160.0
500	0.85	–175.0	0.66	25.1	0.08	–48.6	0.80	–162.0
600	0.89	–179.0	0.50	15.6	0.07	–55.2	0.84	–167.0
700	0.90	177.0	0.39	7.5	0.06	–60.4	0.88	–170.0
800	0.92	173.0	0.32	0.6	0.05	–64.3	0.90	–174.0
900	0.93	169.0	0.26	–5.4	0.04	–67.3	0.92	–177.0
1000	0.94	166.0	0.22	–10.8	0.04	–69.2	0.93	–179.0

Note

1. For more extensive s-parameters see internet:
   http://www.semiconductors.philips.com/markets/communications/wirelesscommunication/broadcast.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 6 leads **SOT171A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.81 6.07	3.18 2.92	2.13 1.88	0.16 0.07	9.25 9.04	9.27 9.02	5.95 5.74	5.97 5.72	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	5.97 5.72	0.25	0.51	0.25
inches	0.268 0.239	0.125 0.115	0.084 0.074	0.006 0.003	0.364 0.356	0.365 0.355	0.234 0.226	0.235 0.225	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.235 0.225	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT171A						99-03-29

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
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