



# F100324

## Low Power Hex TTL-to-ECL Translator

### General Description

The F100324 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. The output levels are voltage compensated over the full  $-4.2V$  to  $-5.7V$  range.

When the circuit is used in the differential mode, the F100324, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The  $V_{EE}$  and  $V_{TTL}$  power may be applied in either order.

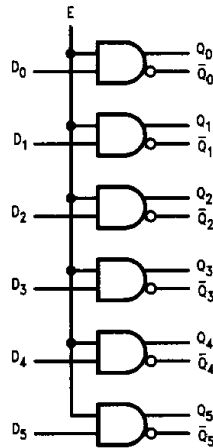
The F100324 is pin and function compatible with the F100124 with similar AC performance, but features power dissipation roughly half of the F100124 to ease system cooling requirements.

### Features

- Pin/function compatible with F100124
- Meets F100124 AC specifications
- 50% power reduction of the F100124
- Differential outputs
- 2000V ESD protection
- $-4.2V$  to  $-5.7V$  operating range

**Ordering Code:** See Section 8

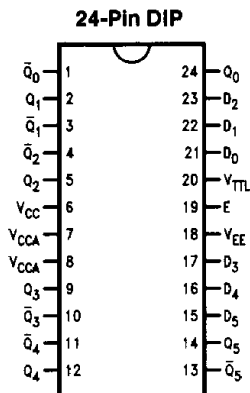
### Logic Diagram



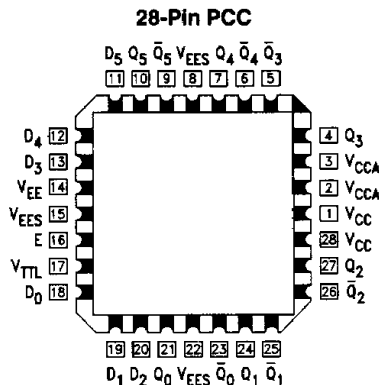
TL/F/9878-4

Pin Names	Description
$D_0-D_5$	Data Inputs
E	Enable Input
$Q_0-Q_5$	Data Outputs
$\bar{Q}_0-\bar{Q}_5$	Complementary Data Outputs

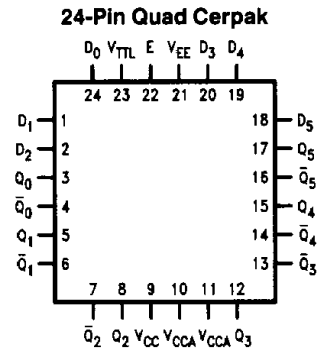
### Connection Diagrams



TL/F/9878-1



TL/F/9878-3



TL/F/9878-2

## Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	
Ceramic	+175°C
Plastic	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
$V_{TTL}$ Pin Potential to Ground Pin	+6.0V to -0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

## Recommended Operating Conditions

Case Temperature ( $T_C$ )	
Commercial	0°C to +85°C
Military	-55°C to +125°C
Supply Voltage ( $V_{EE}$ )	
Commercial	-5.7V to -4.2V
Military	-5.7V to -4.2V

## DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0°C$  to  $+85°C$  (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620		
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage			-1610		
$V_{IH}$	Input HIGH Voltage	2.0		5.0	V	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	0		0.8	V	Guaranteed LOW Signal for All Inputs
$V_{CD}$	Input Clamp Diode Voltage	-1.2			V	$I_{IN} = -18$ mA
$I_{IH}$	Input HIGH Current Data Enable			20 120	μA	$V_{IN} = +2.4V$ , All Other Inputs $V_{IN} = GND$
	Input HIGH Current Breakdown Test, All Inputs			1.0	mA	$V_{IN} = +5.5V$ , All Other Inputs = GND
$I_{IL}$	Input LOW Current Data	-0.9			mA	$V_{IN} = +0.4V$ , All Other Inputs $V_{IN} = V_{IH}$
	Enable	-5.4				
$I_{EE}$	$V_{EE}$ Power Supply Current	-70	-45	-22	mA	All Inputs $V_{IN} = +4.0V$
$I_{TTL}$	$V_{TTL}$ Power Supply Current		25	38	mA	All Inputs $V_{IN} = GND$

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## Ceramic Dual-In-Line Package AC Electric Characteristics

 $V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V \text{ to } +5.5V$ 

Symbol	Parameter	$T_C = 0^\circ\text{C}$		$T_C = +25^\circ\text{C}$		$T_C = +85^\circ\text{C}$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data and Enable to Output	0.50	3.00	0.50	2.90	0.50	3.00	ns	Figures 1 and 2
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

## PCC and Cerpak AC Electrical Characteristics

 $V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V \text{ to } +5.5V$ 

Symbol	Parameter	$T_C = 0^\circ\text{C}$		$T_C = +25^\circ\text{C}$		$T_C = +85^\circ\text{C}$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data and Enable to Output	0.50	2.80	0.50	2.70	0.50	2.80	ns	Figures 1 and 2
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	
$t_{S\ G-G}$	Skew, Gate to Gate	TBD		TBD		TBD		ps	PCC Only (Note 1)

**Note 1:** Gate to gate skew is defined as the difference in the propagation delays between each of the outputs.

## Military Version—Preliminary

### DC Electrical Characteristics

 $V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55^\circ\text{C} \text{ to } +125^\circ\text{C}, V_{TTL} = +4.5V \text{ to } +5.5V$ 

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes	
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ\text{C} \text{ to } +125^\circ\text{C}$	$V_{IN} = V_{IH} \text{ (Max)}$ or $V_{IL} \text{ (Min)}$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3
		-1085	-870	mV	$-55^\circ\text{C}$			
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ\text{C} \text{ to } +125^\circ\text{C}$	OE or DIR Low		
		-1830	-1555	mV	$-55^\circ\text{C}$			
	Cutoff Voltage		-1950	mV	$0^\circ\text{C} \text{ to } +125^\circ\text{C}$			
			-1915	mV	$-55^\circ\text{C}$			
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^\circ\text{C} \text{ to } +125^\circ\text{C}$	$V_{IN} = V_{IH} \text{ (Max)}$ or $V_{IL} \text{ (Min)}$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3
		-1085		mV	$-55^\circ\text{C}$			
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^\circ\text{C} \text{ to } +125^\circ\text{C}$			
			-1555	mV	$-55^\circ\text{C}$			
$V_{IH}$	Input HIGH Voltage	2.0	5.0	V	$-55^\circ\text{C} \text{ to } +125^\circ\text{C}$	Over $V_{TTL}, V_{EE}, T_C$ Range	1, 2, 3, 4	
$V_{IL}$	Input LOW Voltage	0.0	0.8	V	$-55^\circ\text{C} \text{ to } +125^\circ\text{C}$	Over $V_{TTL}, V_{EE}, T_C$ Range	1, 2, 3, 4	
$I_{IH}$	Input HIGH Current		20	$\mu\text{A}$	$-55^\circ\text{C} \text{ to } +125^\circ\text{C}$	$V_{IN} = +2.7V$	1, 2, 3	
	Breakdown Test		100	$\mu\text{A}$	$-55^\circ\text{C} \text{ to } +125^\circ\text{C}$	$V_{IN} = +5.5V$		

**Military Version—Preliminary** (Continued)**DC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$  (Continued)

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes
$I_{IL}$	Input LOW Current Data Enable	-0.9 -5.4		mA	$-55^\circ C$ to $+125^\circ C$	$V_{IN} = +0.5V$	1, 2, 3
$V_{FCD}$	Input Clamp Diode Voltage		-1.2	V	$-55^\circ C$ to $+125^\circ C$	$I_{IN} = -18$ mA	1, 2, 3
$I_{EE}$	$V_{EE}$ Power Supply Current	-70	-22	mA	$-55^\circ C$ to $+125^\circ C$	All Inputs $V_{IN} = +4.0V$	1, 2, 3
$I_{TTL}$	$V_{TTL}$ Power Supply Current		38	mA	$-55^\circ C$ to $+125^\circ C$	All Inputs $V_{IN} = GND$	1, 2, 3

**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 2:** Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups 1, 2, 3, 7, and 8.

**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups A1, 2, 3, 7, and 8.

**Note 4:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

**Ceramic Dual-In-Line Package AC Electric Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data and Enable to Output	0.50	3.00	0.50	2.90	0.30	3.30	ns	Figures 1 and 2	1, 2, 3,
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.35	1.80	0.45	1.80	0.45	1.80	ns		4

**Cerpak AC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data and Enable to Output	0.50	3.00	0.50	2.90	0.30	3.30	ns	Figures 1 and 2	1, 2, 3
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.35	1.80	0.45	1.80	0.45	1.80	ns		4

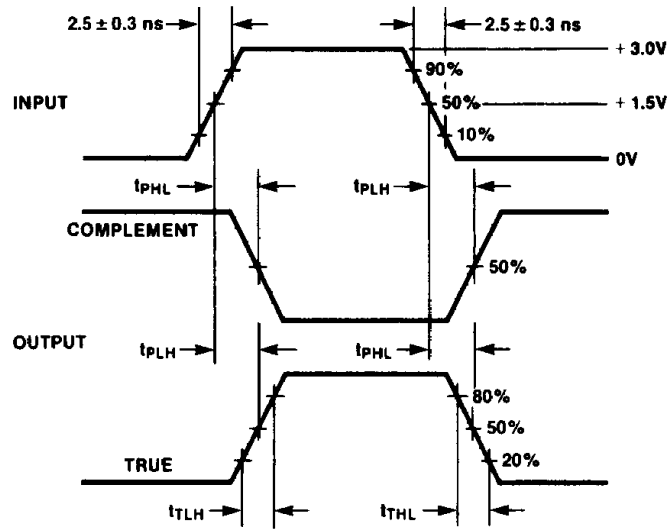
**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 2:** Screen tested 100% on each device at  $+25^\circ C$  temperature only, Subgroup A9.

**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$  and  $-55^\circ C$  temperatures, Subgroups A10 and A11.

**Note 4:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$ , and  $-55^\circ C$  temperature (design characterization data).

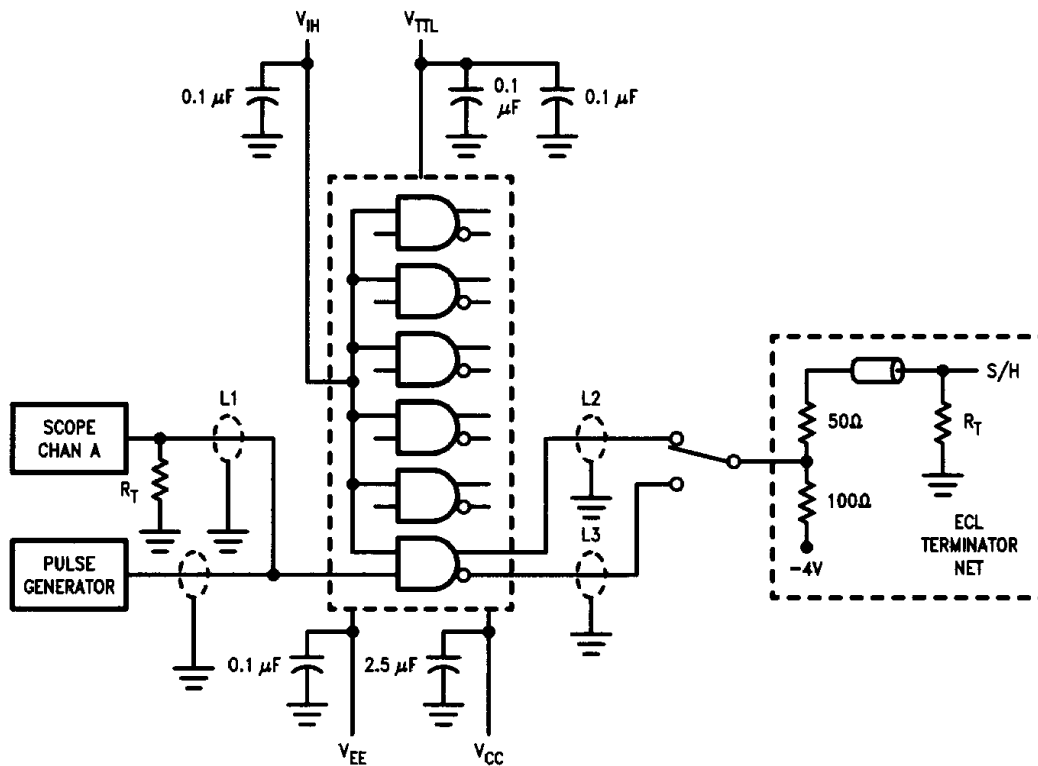
## Switching Waveform



TL/F/9878-6

FIGURE 1. Propagation Delay and Transition Times

## Test Circuit



TL/F/9878-5

FIGURE 2. AC Test Circuit

### Notes:

$V_{CC}, V_{CCA} = 0V, V_{EE} = -4.5V, V_{TTL} = +5.0V, V_{IH} = +3.0V$

L1, L2 and L3 = equal length 50Ω impedance lines

$R_T = 50\Omega$  terminator internal to scope

Decoupling 0.1 μF from GND to  $V_{CC}, V_{EE}$  and  $V_{TTL}$

All unused outputs are loaded with 50Ω to GND

$C_L$  = Fixture and stray capacitance  $\leq 3$  pF



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