# CD54HC40105, CD74HC40105, CD54HCT40105, CD74HCT40105

Data sheet acquired from Harris Semiconductor
SCHS222C

## High-Speed CMOS Logic 4-Bit x 16-Word FIFO Register

February 1998 - Revised October 2003

### Features

- **Independent Asynchronous Inputs and Outputs**
- **Expandable in Either Direction**
- **Reset Capability**
- **Status Indicators on Inputs and Outputs**
- **Three-State Outputs**
- **Shift-Out Independent of Three-State Control**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^{O}$C to 125$^{O}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

### Applications

- **Bit-Rate Smoothing**
- **CPU/Terminal Buffering**
- **Data Communications**
- **Peripheral Buffering**
- **Line Printer Input Buffers**
- **Auto-Dialers**
- **CRT Buffer Memories**
- **Radar Data Acquisition**

### Description

The ’HC40105 and ’HCT40105 are high-speed silicon-gate CMOS devices that are compatible, except for “shift-out” circuitry, with the CD40105B. They are low-power first-in-out (FIFO) “elastic” storage registers that can store 16 four-bit words. The 40105 is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems.

Each work position in the register is clocked by a control flip-flop, which stores a marker bit. A “1” signifies that the position’s data is filled and a “0” denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the “0” state and sees a “1” in the preceeding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to “0”. The first and last control flip-flops have buffered outputs. Since all empty locations “bubble” automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

### Ordering Information

| PART NUMBER | TEMP. RANGE ($^{O}$C) | PACKAGE |
|---|---|---|
| CD54HC40105F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT40105F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC40105E | -55 to 125 | 16 Ld PDIP |
| CD74HC40105M | -55 to 125 | 16 Ld SOIC |
| CD74HC40105MT | -55 to 125 | 16 Ld SOIC |
| CD74HC40105M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT40105E | -55 to 125 | 16 Ld PDIP |
| CD74HCT40105M | -55 to 125 | 16 Ld SOIC |
| CD74HCT40105MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT40105M96 | -55 to 125 | 16 Ld SOIC |

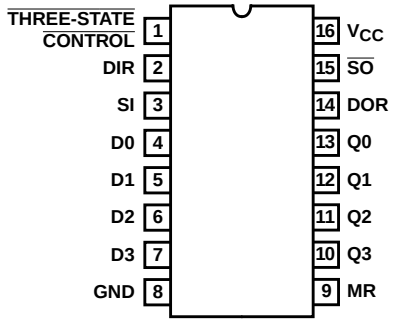
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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## Pinout

**CD54HC40105, CD54HCT40105**
**(CERDIP)**
**CD74HC40105, CD74HCT40105**
**(PDIP, SOIC)**
TOP VIEW




### Loading Data

Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

### Unloading Data

As soon as the first word has rippled to the output, the data-out ready output (DOR) goes HIGH and data of the first word is available on the outputs. Data of other words can be removed by a negative-going transition on the shift-out input ($\overline{SO}$). This negative-going transition causes the DOR signal to go LOW while the next word moves to the output. As long as valid data is available in the FIFO, the DOR signal will go high again, signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain LOW, and any further commands will be ignored until a “1” marker ripples down to the last control register and DOR goes HIGH. If during unloading SI is HIGH, (FIFO is full) data on the data input of the FIFO is entered in the first location.

### Master Reset

A high on the MASTER RESET (MR) sets all the control logic marker bits to “0”. DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded. Thus, MR does not clear data within the register but only the control logic. If the shift-in flag (SI) is HIGH during the master reset pulse, data present at the input (D0 to D3) are immediately moved into the first location upon completion of the reset process.

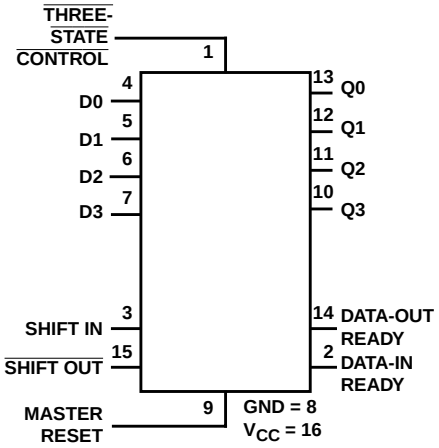
### Three-State Outputs

In order to facilitate data busing, three-state outputs (Q0 to Q3) are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output. A HIGH on the three-state control flag (output enable input OE) forces the outputs into the high-impedance OFF-state mode. Note that the shift-out signal, unlike that in the CD40105B, is independent of the three-state output control. In the CD40105B, the three-state control must not be shifted from High to Low when the shift-out signal is Low (data loss would occur). In the high-speed CMOS version this restriction has been eliminated.

### Cascading

The 40105 can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than four bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions (see Figures 12 and 13).

## Functional Diagram



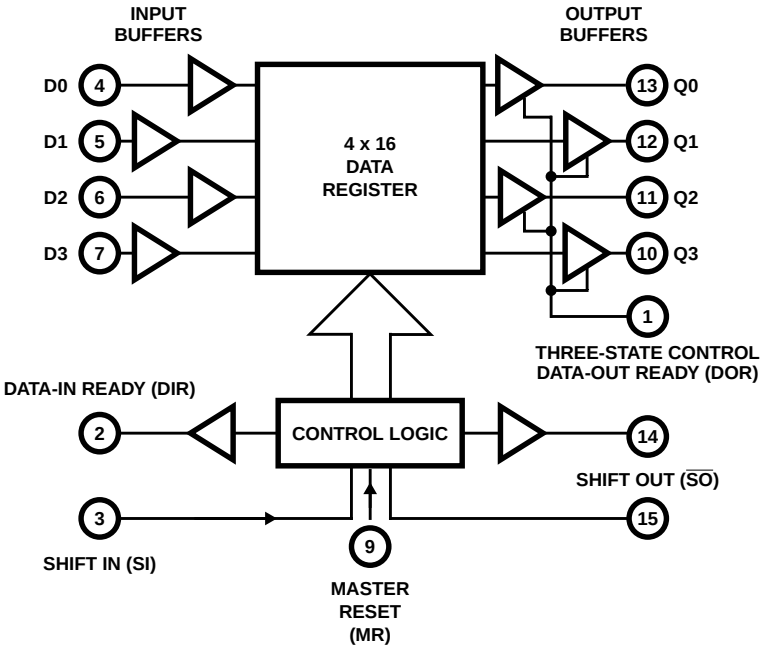
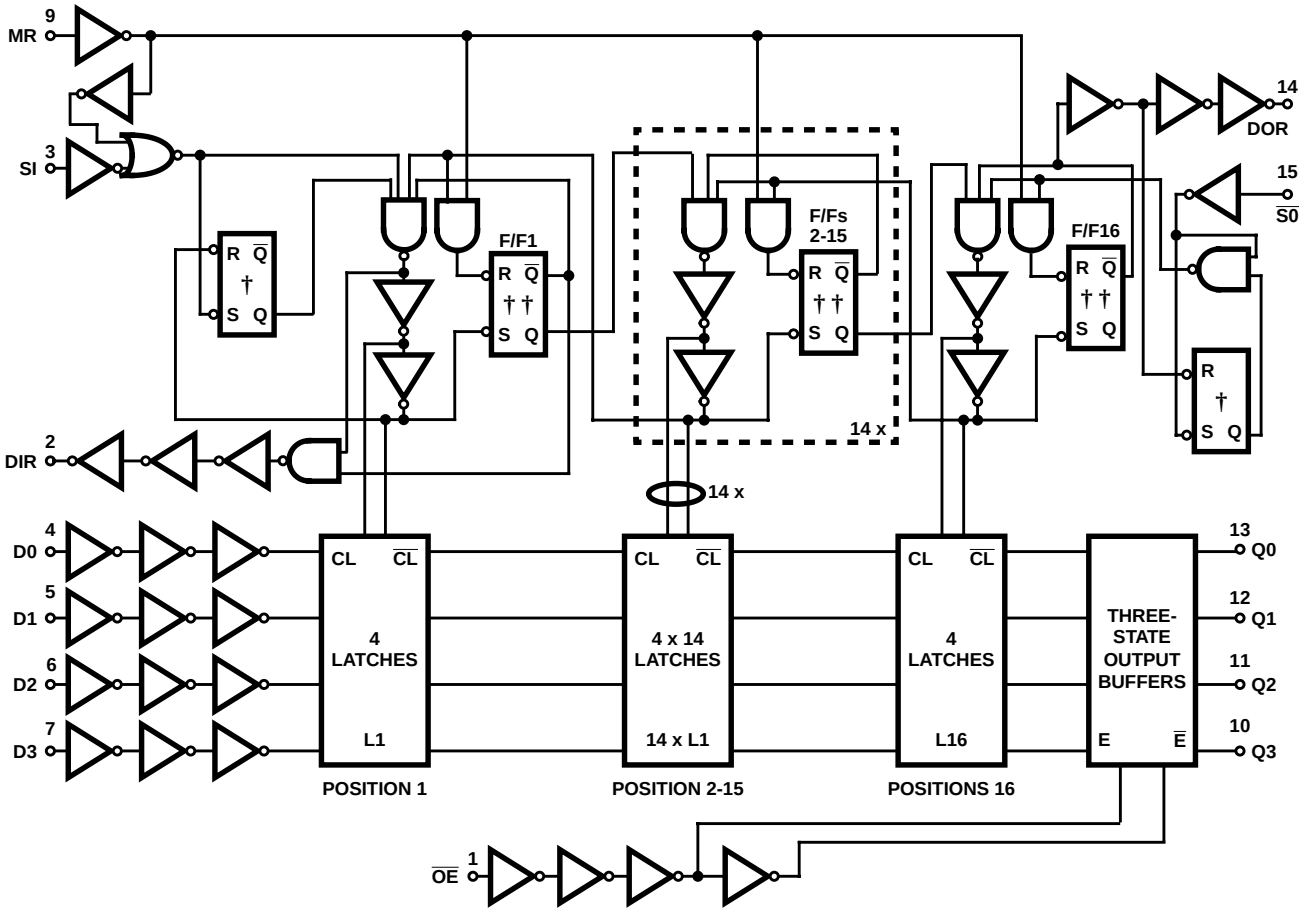



**FIGURE 1. FUNCTIONAL BLOCK DIAGRAM**




† "S" overrides "R".
†† "R" overrides "S".

**FIGURE 2. LOGIC DIAGRAM**

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| E (PDIP) Package | 67 |
| M (SOIC) Package | 73 |

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Three-State Leakage Current | $I_{OZ}$ | $V_{IL}$ or $V_{IH}$ | $V_O$ = $V_{CC}$ or GND | 6 | - | - | ±0.5 | - | ±5 | - | ±10 | µA |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ and GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Three-State Leakage Current | $I_{OZ}$ | $V_{IL}$ or $V_{IH}$ | $V_O$ = $V_{CC}$ or GND | 5.5 | - | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| $\overline{OE}$ | 0.75 |
| SI, $\overline{SO}$ | 0.4 |
| Dn | 0.3 |
| MR | 1.5 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

**Prerequisite for Switching Specifications**

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | |
| SI Pulse Width HIGH or LOW | $t_W$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| $\overline{SO}$ Pulse Width HIGH or LOW | $t_W$ | 2 | 120 | - | 150 | - | 180 | - | ns |
| | | 4.5 | 24 | - | 30 | - | 36 | - | ns |
| | | 6 | 20 | - | 26 | - | 31 | - | ns |
| DIR Pulse Width HIGH or LOW | $t_W$ | 2 | 200 | - | 250 | - | 300 | - | ns |
| | | 4.5 | 40 | - | 50 | - | 60 | - | ns |
| | | 6 | 34 | - | 43 | - | 51 | - | ns |
| DOR Pulse Width HIGH or LOW | $t_W$ | 2 | 200 | - | 250 | - | 300 | - | ns |
| | | 4.5 | 40 | - | 50 | - | 60 | - | ns |
| | | 6 | 34 | - | 43 | - | 51 | - | ns |
| MR Pulse Width HIGH | $t_W$ | 2 | 120 | - | 150 | - | 180 | - | ns |
| | | 4.5 | 24 | - | 30 | - | 36 | - | ns |
| | | 6 | 20 | - | 26 | - | 31 | - | ns |
| Removal Time MR to SI | $t_{REM}$ | 2 | 50 | - | 65 | - | 75 | - | ns |
| | | 4.5 | 10 | - | 13 | - | 15 | - | ns |
| | | 6 | 9 | - | 11 | - | 13 | - | ns |
| Set-Up Time Dn to SI | $t_{SU}$ | 2 | 5 | - | 5 | - | 5 | - | ns |
| | | 4.5 | 5 | - | 5 | - | 5 | - | ns |
| | | 6 | 5 | - | 5 | - | 5 | - | ns |
| Hold Time Dn to SI | $t_H$ | 2 | 125 | - | 155 | - | 190 | - | ns |
| | | 4.5 | 25 | - | 31 | - | 38 | - | ns |
| | | 6 | 21 | - | 26 | - | 32 | - | ns |
| Maximum Pulse Frequency SI, $\overline{SO}$ | $f_{MAX}$ | 2 | 3 | - | 2 | - | 2 | - | MHz |
| | | 4.5 | 15 | - | 12 | - | 10 | - | MHz |
| | | 6 | 18 | - | 14 | - | 12 | - | MHz |
| **HCT TYPES** | | | | | | | | | |
| SI Pulse Width HIGH or LOW | $t_W$ | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| $\overline{SO}$ Pulse Width HIGH or LOW | $t_W$ | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| DIR Pulse Width HIGH or LOW | $t_W$ | 4.5 | 40 | - | 50 | - | 60 | - | ns |
| DOR Pulse Width HIGH or LOW | $t_W$ | 4.5 | 40 | - | 50 | - | 60 | - | ns |
| MR Pulse Width HIGH | $t_W$ | 4.5 | 24 | - | 30 | - | 36 | - | ns |
| Removal Time MR to SI | $t_{REM}$ | 4.5 | 15 | - | 19 | - | 22 | - | ns |
| Set-Up Time Dn to SI | $t_{SU}$ | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| Hold Time Dn to SI | $t_H$ | 4.5 | 25 | - | 31 | - | 38 | - | ns |
| Maximum Pulse Frequency SI, $\overline{SO}$ | $f_{MAX}$ | 4.5 | 15 | - | 12 | - | 10 | - | MHz |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 175 | - | 220 | - | 265 | ns |
| MR to DIR, DOR | | $C_L$ = 50pF | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | $C_L$ = 15pF | 5 | - | 15 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 30 | - | 37 | - | 45 | ns |
| SI to DIR | $t_{PHL}$, $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 210 | - | 265 | - | 315 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| | | $C_L$ = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 36 | - | 45 | - | 54 | ns |
| $\overline{SO}$ to DOR | $t_{PHL}$, $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 210 | - | 265 | - | 315 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| | | $C_L$ = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 36 | - | 45 | - | 54 | ns |
| $\overline{SO}$ to Qn | $t_{PHL}$, $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 400 | - | 500 | - | 600 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 80 | - | 100 | - | 120 | ns |
| | | $C_L$ = 15pF | 5 | - | 35 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 68 | - | 85 | - | 102 | ns |
| Propagation Delay/Ripple thru Delay SI to DOR | $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 2000 | - | 2500 | - | 3000 | ns |
| | | | 4.5 | - | - | 400 | - | 500 | - | 600 | ns |
| | | | 6 | - | - | 340 | - | 425 | - | 510 | ns |
| Propagation Delay/Ripple thru Delay $\overline{SO}$ to DIR | $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 2500 | - | 3125 | - | 3750 | ns |
| | | | 4.5 | - | - | 500 | - | 625 | - | 750 | ns |
| | | | 6 | - | - | 425 | - | 532 | - | 638 | ns |
| Propagation Delay/Ripple thru Delay SI to Qn | $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 1500 | - | 1900 | - | 2250 | ns |
| | | | 4.5 | - | - | 300 | - | 380 | - | 450 | ns |
| | | | 6 | - | - | 260 | - | 330 | - | 380 | ns |
| Three-State Output Enable $\overline{OE}$ to $Q_n$ | $t_{PZH}$, $t_{PZL}$ | $C_L$ = 50pF | 2 | - | - | 150 | - | 190 | - | 225 | ns |
| | | | 4.5 | - | - | 30 | - | 38 | - | 45 | ns |
| | | | 6 | - | - | 26 | - | 33 | - | 38 | ns |
| Three-State Output Disable $\overline{OE}$ to Qn | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ = 50pF | 2 | - | - | 140 | - | 175 | - | 210 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 28 | - | 35 | - | 42 | ns |
| | | $C_L$ = 50pF | 6 | - | - | 24 | - | 30 | - | 36 | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Maximum SI, $\overline{SO}$ Frequency | $f_{MAX}$ | $C_L$ = 15pF | 5 | - | 32 | - | - | - | - | - | MHz |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | $C_L$ = 15pF | 5 | - | 83 | - | - | - | - | - | pF |

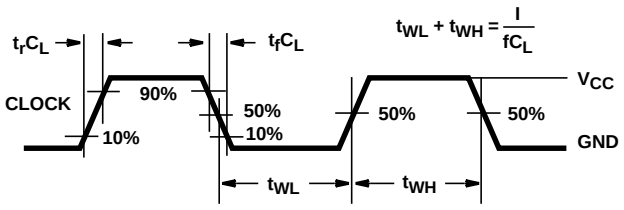
**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Three-State Output Capacitance | $C_O$ | $C_L$ = 50pF | - | - | - | 15 | - | 15 | - | 15 | pF |
| **HCT TYPES** | | | | | | | | | | | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 36 | - | 45 | - | 54 | ns |
| MR to DIR, DOR | | $C_L$ = 15pF | 5 | - | 15 | - | - | - | - | - | ns |
| SI to DIR | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| | | $C_L$ =15pF | 5 | - | 18 | - | - | - | - | - | ns |
| $\overline{SO}$ to DOR | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| | | $C_L$ =15pF | 5 | - | 18 | - | - | - | - | - | ns |
| $\overline{SO}$ to Qn | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 80 | - | 100 | - | 120 | ns |
| | | $C_L$ =15pF | 5 | - | 35 | - | - | - | - | - | ns |
| Propagation Delay/Ripple thru Delay SI to DOR | $t_{PLH}$ | $C_L$ = 50pF | 4.5 | - | - | 400 | - | 500 | - | 600 | ns |
| Propagation Delay/Ripple thru Delay $\overline{SO}$ to DIR | $t_{PLH}$ | $C_L$ = 50pF | 4.5 | - | - | 500 | - | 625 | - | 750 | ns |
| Propagation Delay/Ripple thru Delay SI to Qn | $t_{PLH}$ | $C_L$ = 50pF | 4.5 | - | - | 300 | - | 380 | - | 450 | ns |
| Three-State Output Enable $\overline{OE}$ to $Q_n$ | $t_{PZH}$, $t_{PZL}$ | $C_L$ = 50pF | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| Three-State Output Disable $\overline{OE}$ to Qn | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ = 50pF | 4.5 | - | - | 30 | - | 38 | - | 45 | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Maximum CP Frequency | $f_{MAX}$ | $C_L$ =15pF | 5 | - | 32 | - | - | - | - | - | MHz |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | $C_L$ =15pF | 5 | - | 83 | - | - | - | - | - | pF |
| Three-State Output Capacitance | $C_O$ | $C_L$ = 50pF | - | - | - | 15 | - | 15 | - | 15 | pF |

NOTES:

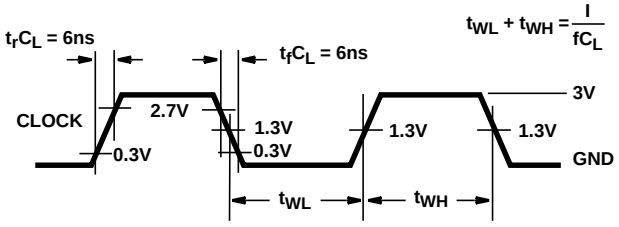
3. $C_{PD}$ is used to determine the dynamic power consumption, per package.
4. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where $f_i$ = Input Frequency, $f_o$ = Output Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## Test Circuits and Waveforms




NOTE: Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{MAX}$, input duty cycle = 50%.

**FIGURE 3. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**




NOTE: Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{MAX}$, input duty cycle = 50%.

**FIGURE 4. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

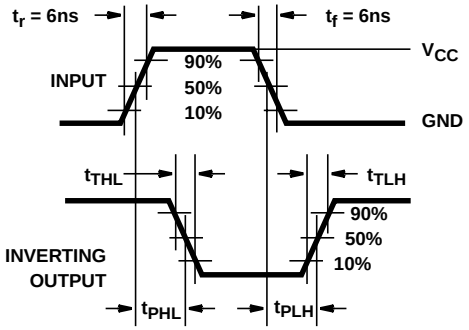



**FIGURE 5. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

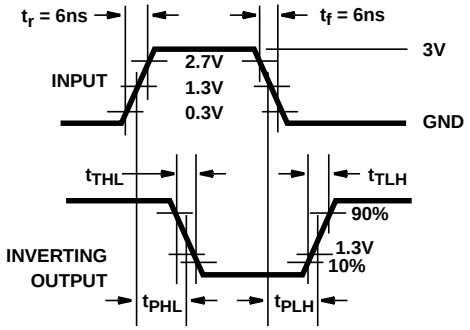



**FIGURE 6. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

## Test Circuits and Waveforms (Continued)

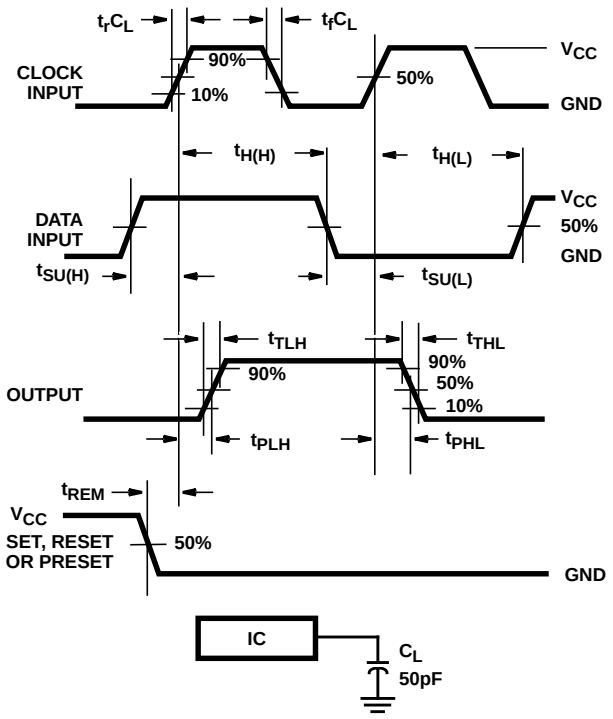



FIGURE 7. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

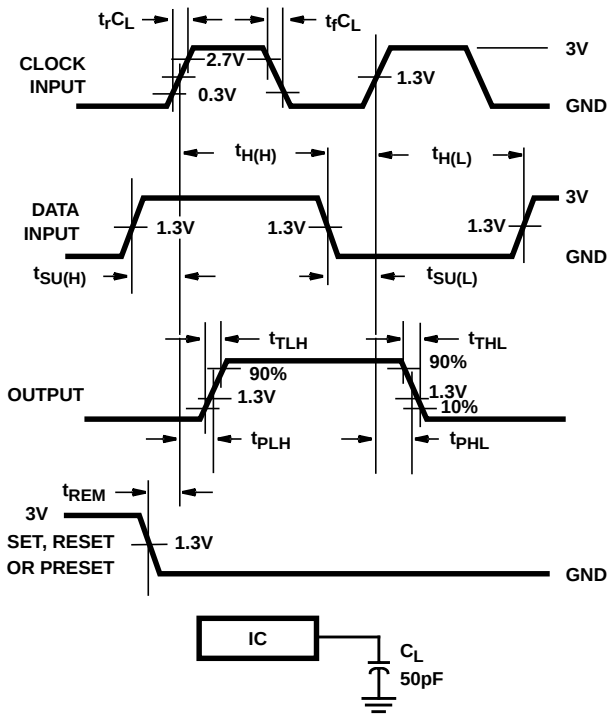



FIGURE 8. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

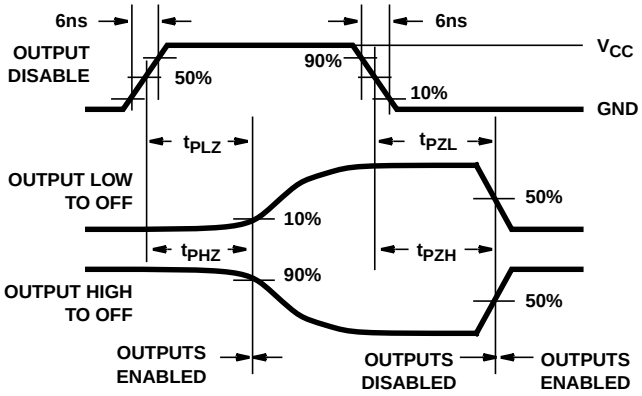



FIGURE 9. HC THREE-STATE PROPAGATION DELAY WAVEFORM

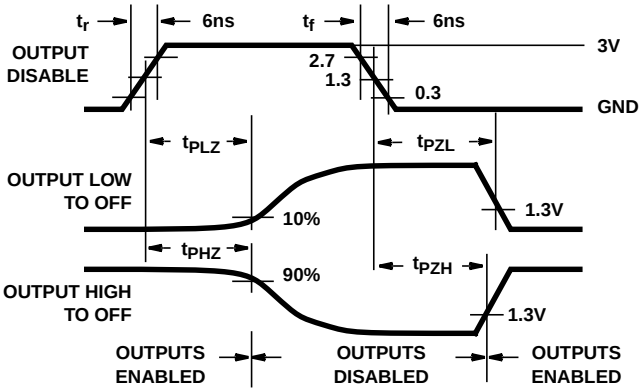
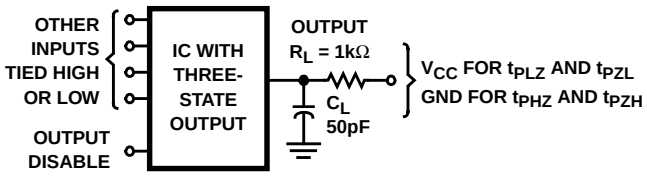
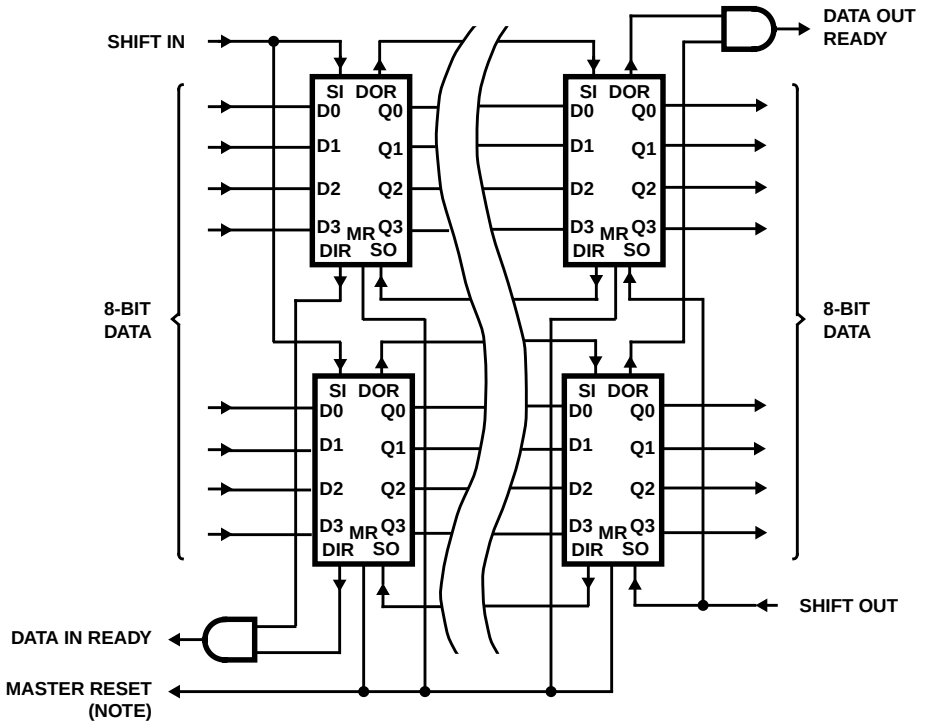



FIGURE 10. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



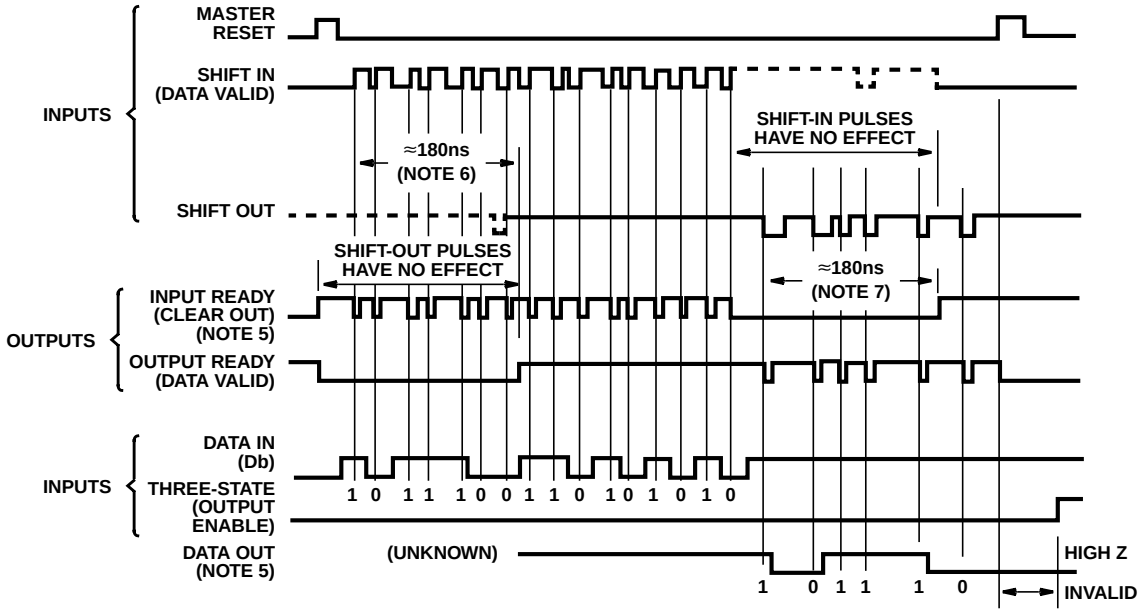

NOTE: Open drain waveforms $t_{PLZ}$ and $t_{PZL}$ are the same as those for three-state shown on the left. The test circuit is Output $R_L$ = 1kΩ to $V_{CC}$, $C_L$ = 50pF.

FIGURE 11. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT




NOTE: Pulse must be applied for cascading by 16 N bits.

**FIGURE 12. EXPANSION, 8-BITS WIDE BY 16 N-BITS LONG USING HC/HCT40105**




NOTES:

5. Data valid goes to high level in advance of the data out by a maximum of 38ns at $V_{CC}$ = 4.5V for $C_L$ = 50pF and $T_A$ = 25$^oC$.
6. At $V_{CC}$ = 4.5V, ripple time from position 1 to position 16.
7. At $V_{CC}$ = 4.5V, ripple time from position 16 to position 1.

**FIGURE 13. TIMING DIAGRAM FOR THE CD74HC/HCT40105**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| CD54HC40105F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| CD54HCT40105F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| CD74HC40105E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC40105EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC40105M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC40105M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC40105M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC40105M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC40105ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC40105MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC40105MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC40105MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC40105MTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT40105E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT40105EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT40105M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT40105M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT40105M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT40105M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT40105ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT40105MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT40105MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT40105MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT40105MTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

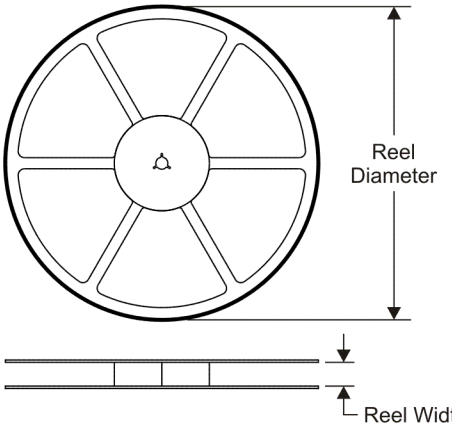
**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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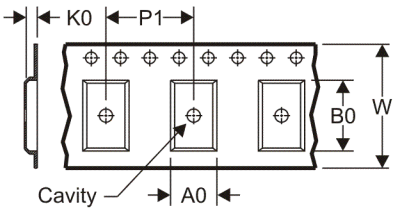
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

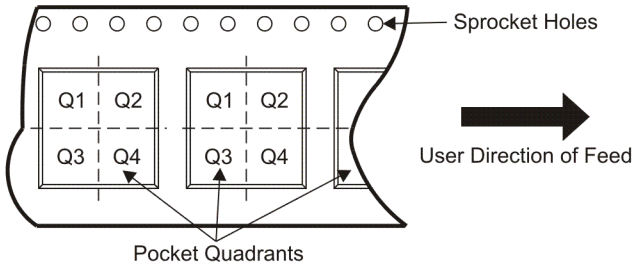



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

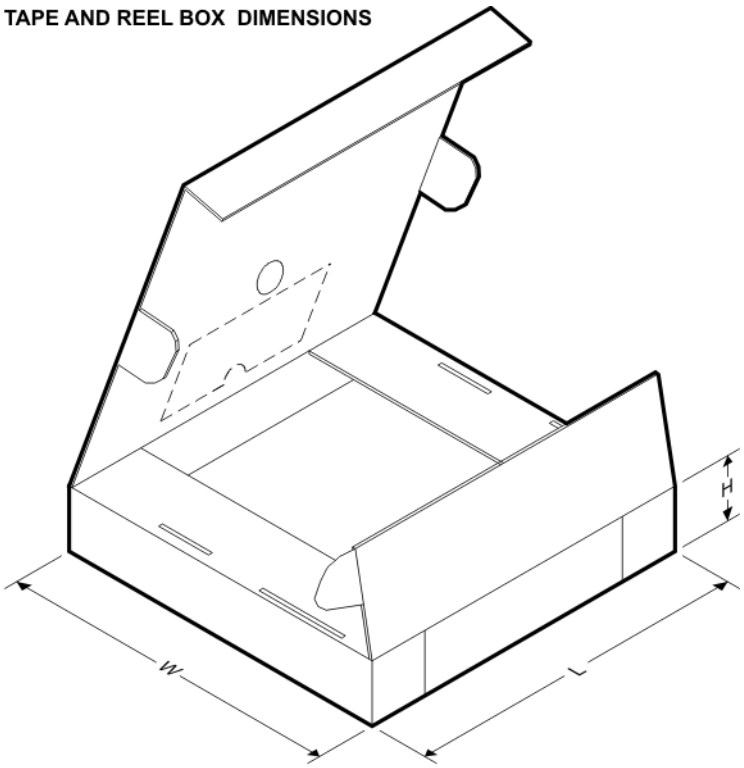
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC40105M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT40105M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



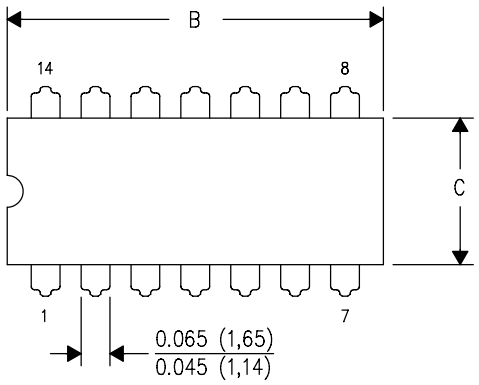

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC40105M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HCT40105M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

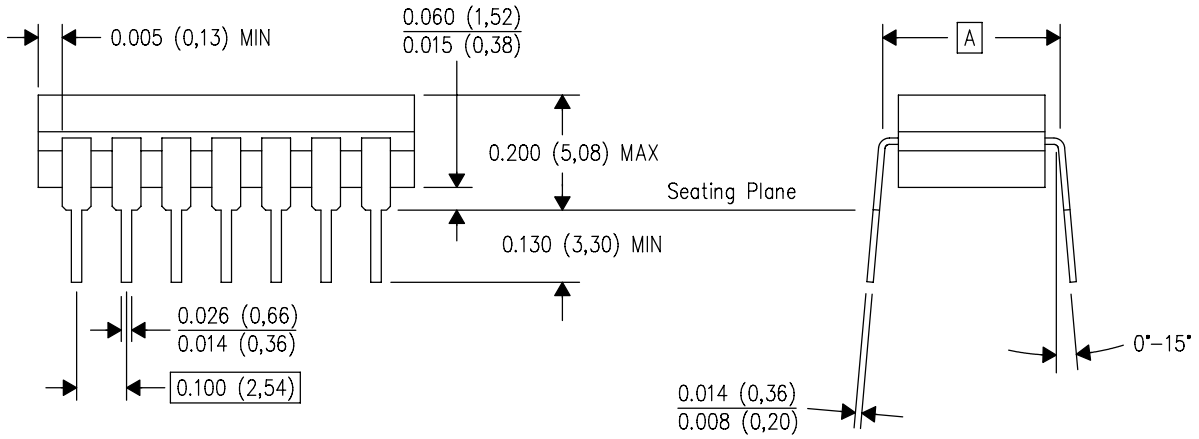
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



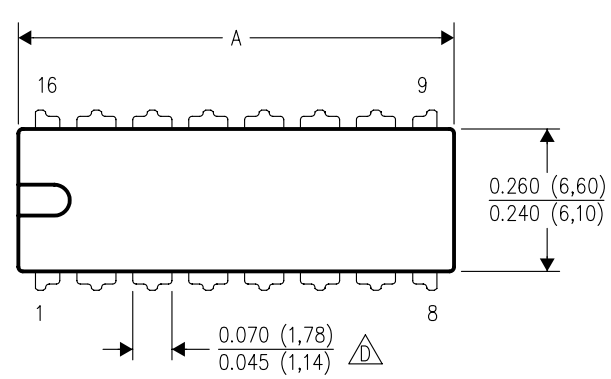

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

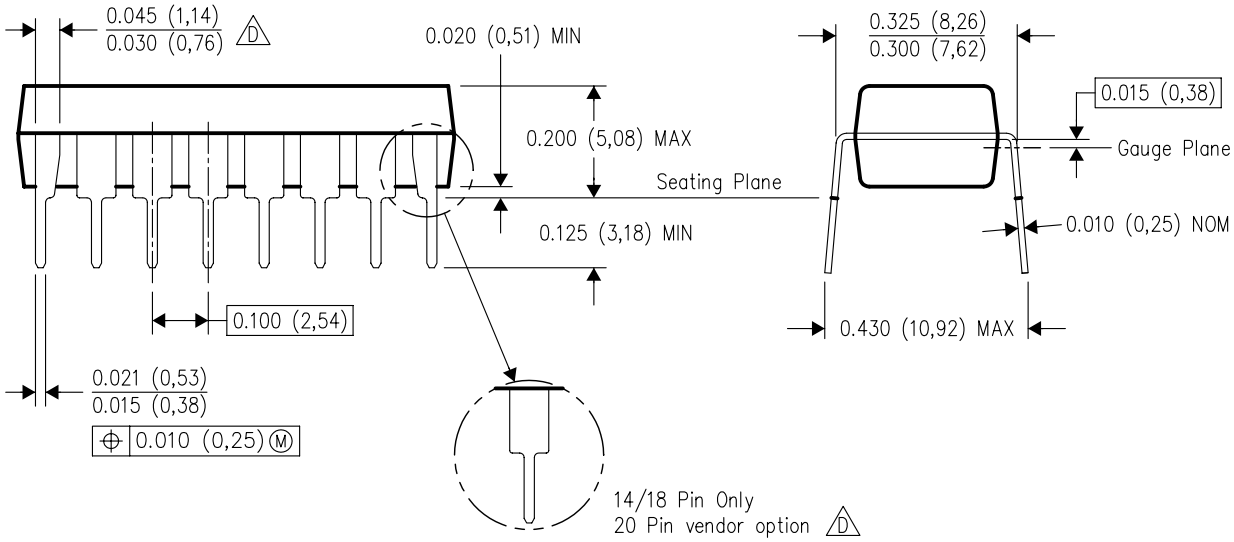
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



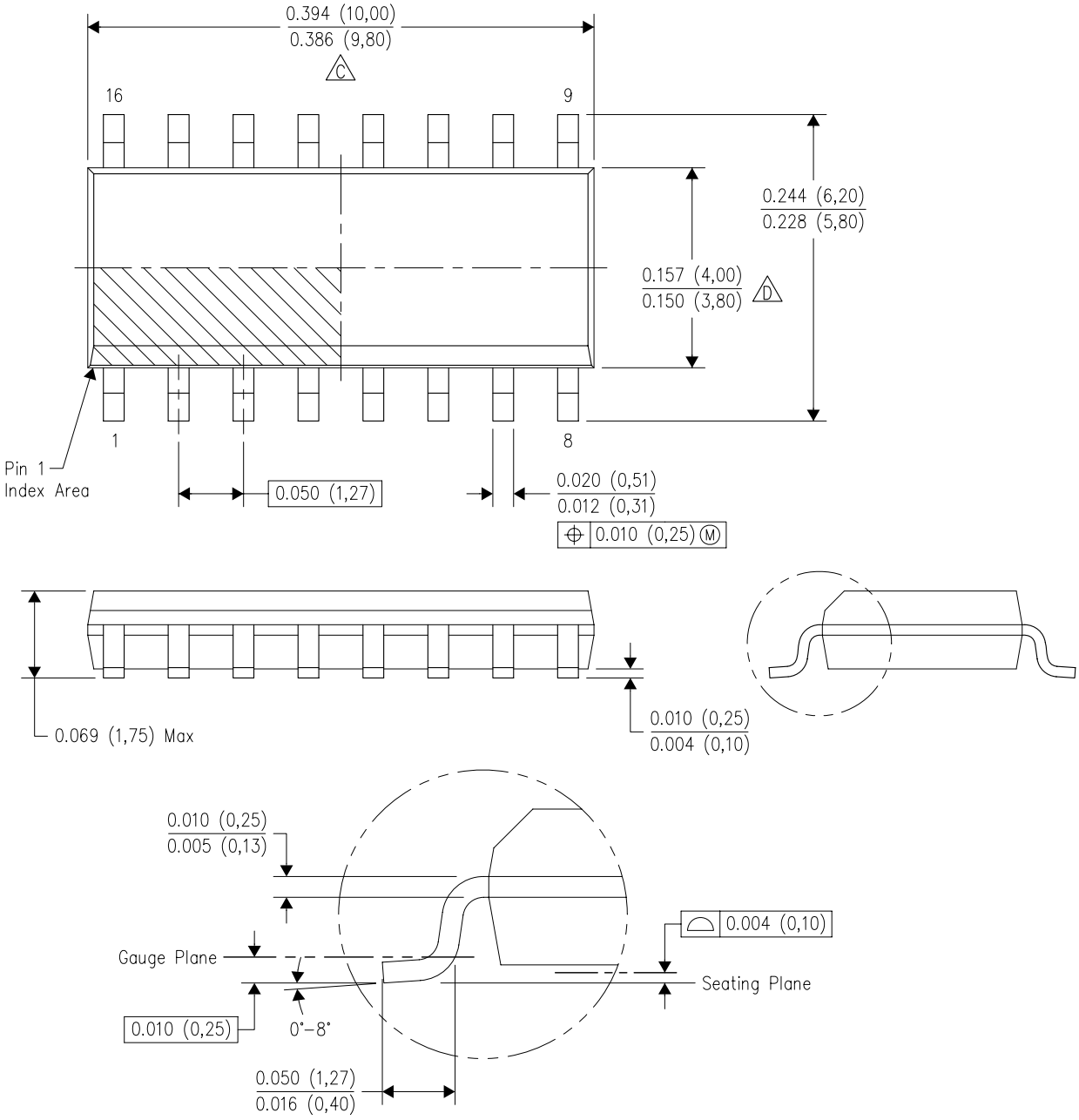

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

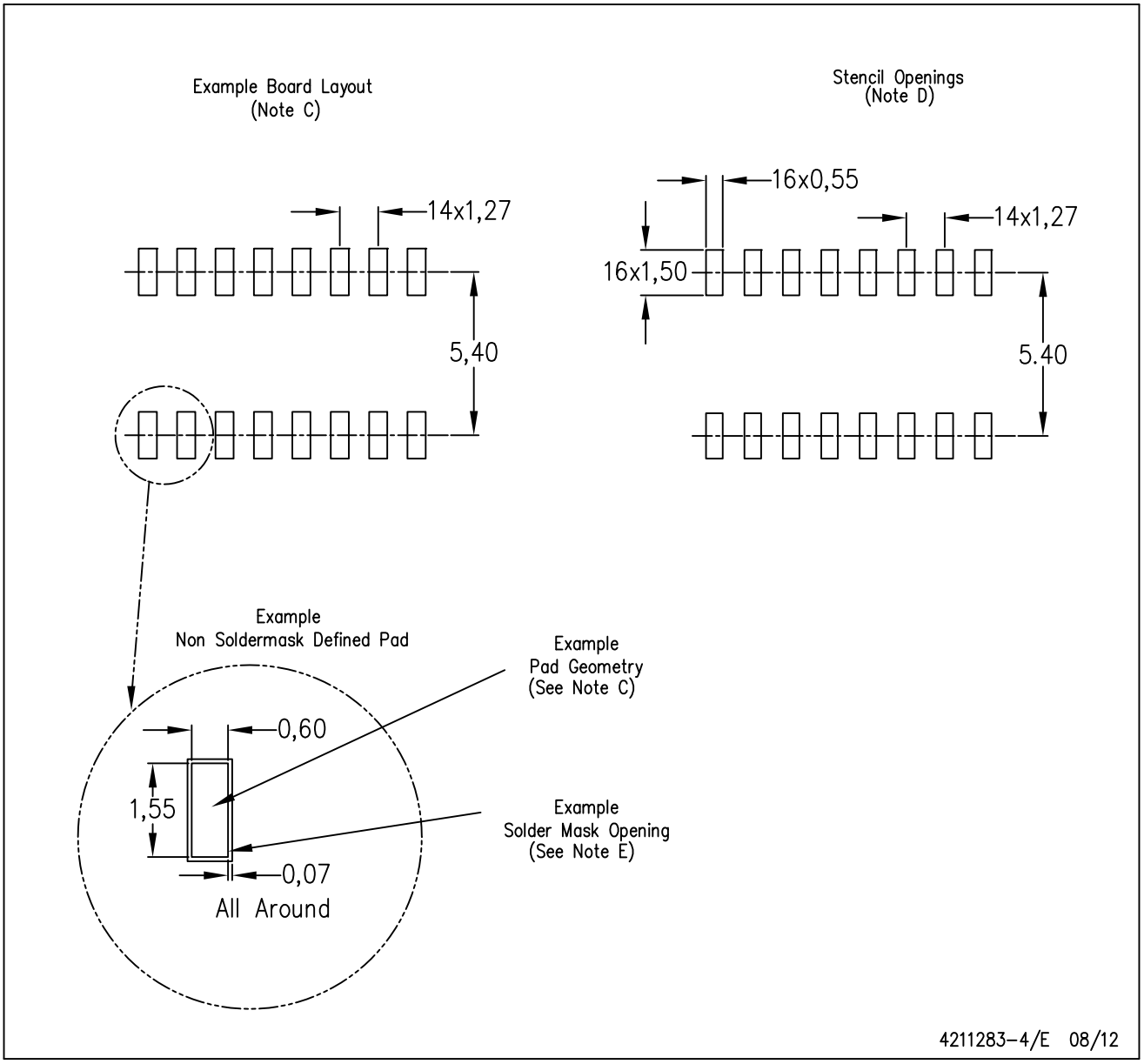
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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ИНН: 7735154786
ОГРН: 1167746717709