FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-13511-3E

Linear IC Converter

CMOS

D/A Converter for Digital Tuning

(12-channel, 8-bit, on-chip OP amp, low-voltage)

MB88346L

■ DESCRIPTION

The Fujitsu MB88346L is a 12-channel 8-bit D/A converter capable of low-voltage operation that has amplifiers built into each of the 12 analog output lines to deliver heavy-current drive capability.

The use of serial data input means that only three control lines are required, and enables cascade connection of multiple MB88346L chips.

The MB88346L is suitable for applications such as electronic volume controls and replacing trimmer potentiometers in tuning systems. In addition, the MB88346L is both function-compatible and pin-compatible the currently used MB88346B, making it easy to reduce the voltage level of a system by simply replacing the MB88346B with the MB88346L.

■ FEATURES

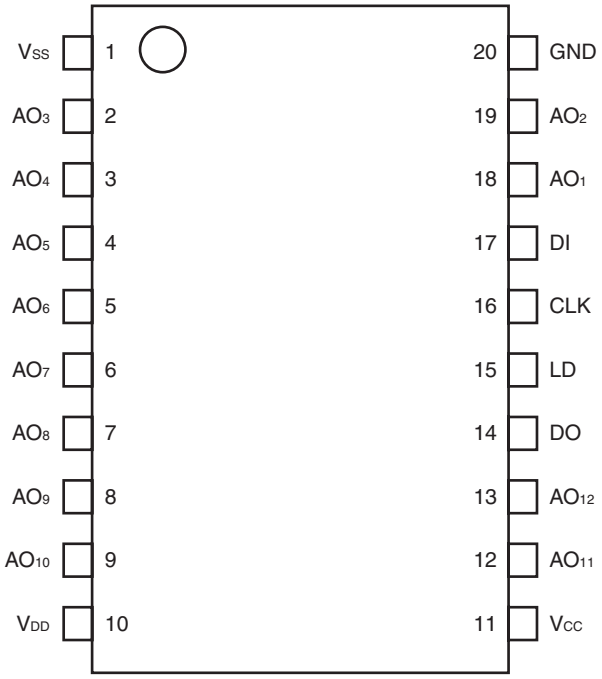
- Low voltage operation (V_{CC}/V_{DD} : 2.7 V to 3.6 V)
- Ultra-low power consumption (0.5 mW/ch at V_{CC} = 3 V)
- Ultra-compact space-saving package lineup (SSOP-20)
- Contains 12-channel R-2R type 8-bit D/A converter
- On-chip analog output amps (sink current max. 1.0 mA, source current max. 1.0 mA)
- Analog output range from 0 to V_{CC}
- Two separate power supply/ground lines for MCU interface block/operational amplifier output buffer block and D/A converter block
- Serial data input : maximum operating speed 2.5 MHz
  (maximum operating speed in cascade connection is 1.5 MHz)
- CMOS process
- Package lineup includes DIP 20-pin, SSOP 20-pin

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■ PIN ASSIGNMENT

(Top view)

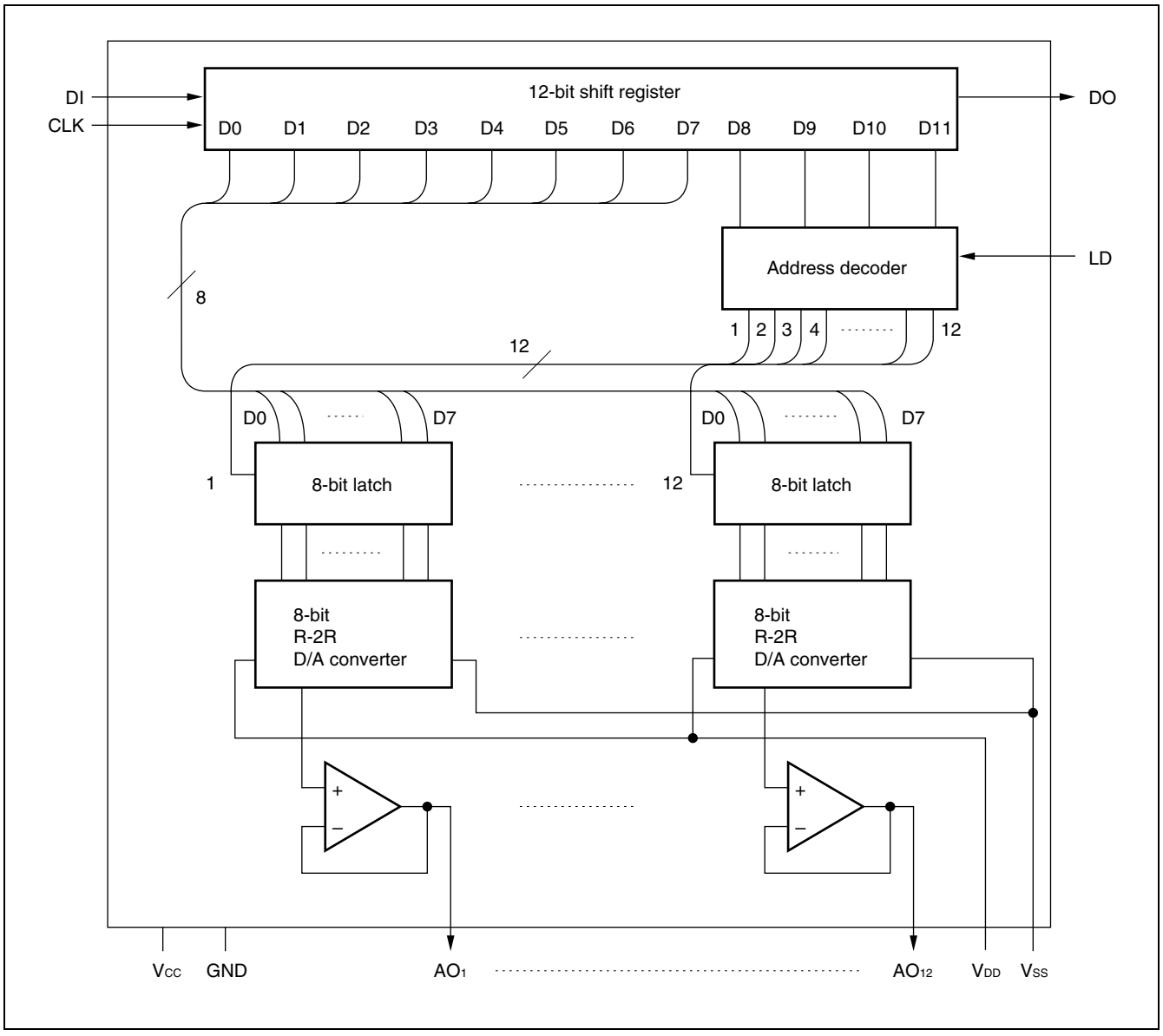


(DIP-20P-M02)
(FPT-20P-M03)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Function
17	DI	I	Serial address/data input to the internal 12-bit shift register : The address/data format is that upper 4 bits (D11 to D8) indicate an address and lower 8 bits (D7 to D0) indicate data. The D11 (MSB) is the first-in bit and D0 (LSB) is the last-in bit.
14	DO	O	Outputs MSB bit data from 12-bit shift register.
16	CLK	I	Shift clock input to the internal 12-bit shift register : At the rising edge of CLK data on the DI pin is shifted into the LSB of the shift register and contents of the shift register are shifted right (to the MSB) .
15	LD	I	Load strobe input for a 12-bit address/data : A high level on the LD pin latches a 4-bit address (upper 4 bits : D11 to D8) of the internal 12-bit shift register into the internal address decoder, and writes 8-bit data (lower 8 bits : D7 to D0) of the shift register into an internal data latch selected by the latched address.
18 19 2 3 4 5 6 7 8 9 12 13	AO_1 AO_2 AO_3 AO_4 AO_5 AO_6 AO_7 AO_8 AO_9 AO_{10} AO_{11} AO_{12}	O	8-bit D/A output pins with OP amps.
11	V_{CC}	—	MCU interface and OP amp power supply pin.
20	GND	—	MCU interface and OP amp ground pin.
10	V_{DD}	—	D/A converter power supply pin.
1	V_{SS}	—	D/A converter ground pin.

■ BLOCK DIAGRAM

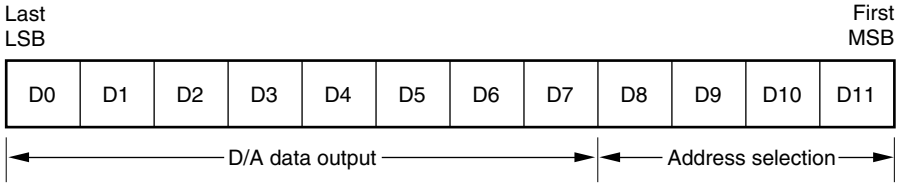


■ DATA CONFIGURATION

The MB88346L has a 12-bit shift register for controlling the chip. The data passed to the 12-bit shift register needs to be supplied in the following format.

The data structure consists of a total of 12 bits, four for address selection and eight for D/A data output.

1. Shift Register Control Data Configuration



2. D/A Converter Control Signals

D0	D1	D2	D3	D4	D5	D6	D7	D/A data output
0	0	0	0	0	0	0	0	≒ V_{SS}
1	0	0	0	0	0	0	0	≒ $V_{LB} + V_{SS}$
0	1	0	0	0	0	0	0	≒ $V_{LB} \times 2 + V_{SS}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	≒ $V_{LB} \times 254 + V_{SS}$
1	1	1	1	1	1	1	1	≒ V_{DD}

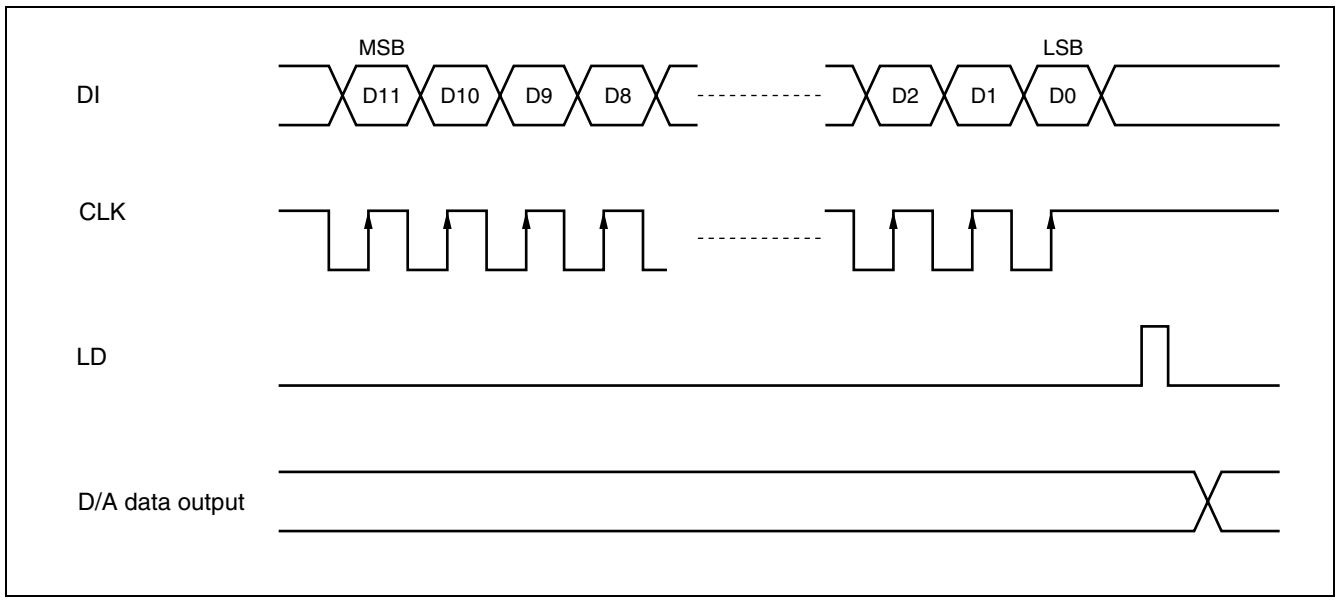
$V_{LB} = (V_{DD} - V_{SS}) /255$

3. Address Selection Signals

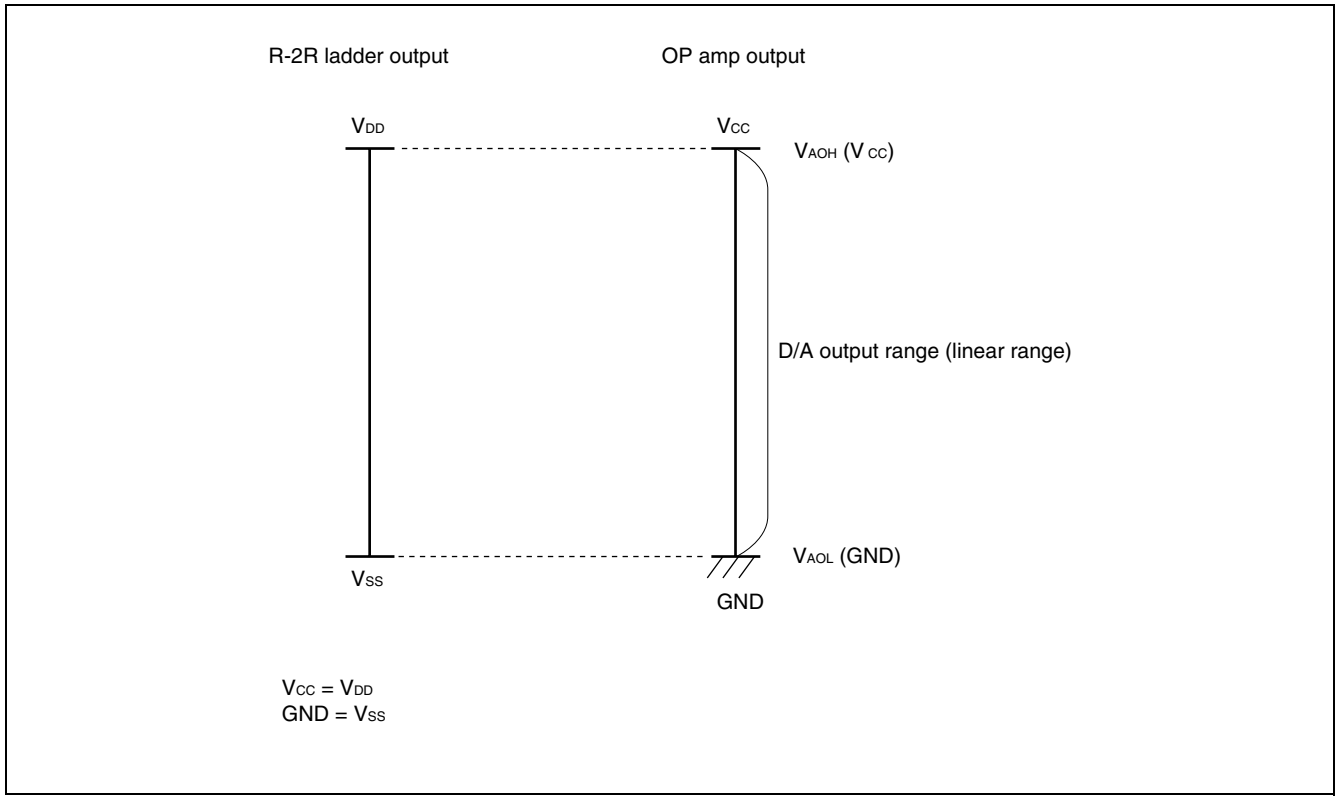
D8	D9	D10	D11	Address selection
0	0	0	0	Don't Care
0	0	0	1	AO_1 selection
0	0	1	0	AO_2 selection
0	0	1	1	AO_3 selection
0	1	0	0	AO_4 selection
0	1	0	1	AO_5 selection
0	1	1	0	AO_6 selection
0	1	1	1	AO_7 selection
1	0	0	0	AO_8 selection
1	0	0	1	AO_9 selection
1	0	1	0	AO_{10} selection
1	0	1	1	AO_{11} selection
1	1	0	0	AO_{12} selection
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

■ OPERATING DESCRIPTION

1. Timing Chart for Data Condition Setup



2. Analog Output Voltage Range



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	GND used as reference, Ta = + 25 °C	− 0.3	+ 7.0	V
	V_{DD}*		− 0.3	+ 7.0	V
Input voltage	V_{IN}		− 0.3	V_{CC} + 0.3	V
Output voltage	V_{OUT}		− 0.3	V_{CC} + 0.3	V
Power consumption	P_D	—	—	250	mW
Operating temperature	Ta	—	− 20	+ 85	°C
Storage temperature	Tstg	—	− 55	+ 150	°C

* : $V_{CC} \geq V_{DD}$

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage 1	V_{CC}	—	2.7	—	3.6	V
	GND	—	—	0	—	V
Power supply voltage 2	V_{DD}	$V_{DD} - V_{SS} \geq 2.0$ V	2.0	—	V_{CC}	V
	V_{SS}		GND	—	V_{CC} − 2.0	V
Analog output source current	I_{AL}	V_{CC} = 3.0 V	—	—	1.0	mA
Analog output sink current	I_{AH}	V_{CC} = 3.0 V	—	—	1.0	mA
Oscillator limiting output capacity	C_{AL}	—	—	—	0.1	µF
Digital data value range	—	—	#00	—	#FF	—
Operating temperature	Ta	—	− 20	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(1) Digital Block

(V_{DD}, V_{CC} = 2.7 V to 3.6 V ($V_{CC} \geq V_{DD}$) , GND = V_{SS} = 0 V, Ta = –20 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{CC}	V_{CC}	—	2.7	3.0	3.6	V
Power supply current 1	I_{CC}		Stationary (CLK signal stopped) , no load	—	1.2	3.0	mA
Input leak current	I_{ILK}	CLK, DI, LD	V_{IN} = 0 to V_{CC}	– 10	—	+ 10	µA
L level input voltage	V_{IL}		—	—	—	0.2 V_{CC}	V
H level input voltage	V_{IH}		—	0.8 V_{CC}	—	—	V
L level output voltage	V_{OL}	DO	I_{OL} = 2.5 mA	—	—	0.4	V
H level output voltage	V_{OH}		I_{OH} = – 400 µA	V_{CC} – 0.4	—	—	V

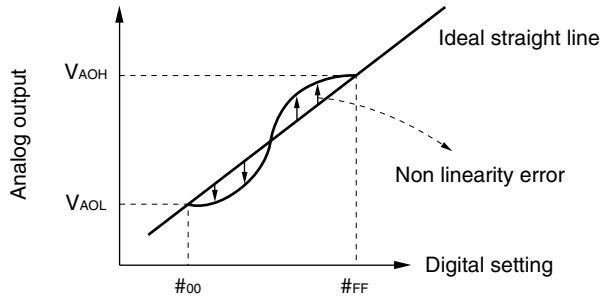
(2) Analog Block 1

(V_{DD}, V_{CC} = 2.7 V to 3.6 V ($V_{CC} \geq V_{DD}$) , GND = V_S = 0 V, Ta = –20 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Power consumption	I_{DD}	V_{DD}	Maximum setting value from #00 to #FF	—	0.6	1.5	mA
Analog voltage	V_{DD}	V_{DD}	$V_{DD} – V_{SS} \geq 2.0$	2.0	—	V_{CC}	V
	V_{SS}	V_{SS}		GND	—	V_{CC} – 2.0	V
Resolution	Res	AO_1 to AO_{12}	—	—	8	—	bit
Monotonic increase	Rem		$V_{DD} \leq V_{CC}$ – 0.1 V, $V_{SS} \geq$ 0.1 V, no load	—	8	—	bit
Nonlinearity error	LE			– 1.5	—	+ 1.5	LSB
Differential linearity error	D_{LE}			– 1.0	—	+ 1.0	LSB

Nonlinearity error : Deviation (error) in input/output curves with respect to an ideal straight line connecting output voltage at “00” and output voltage at “FF.”

Differential linearity error : Deviation (error) in amplification with respect to theoretical increase in amplification per 1-bit increase in digital value.



Note : The value of V_{AOH} and V_{DD}, and the value of V_{AOL} and V_{SS} are not necessarily equivalent.

(3) Analog Block 2

(V_{DD}, V_{CC} = 2.7 V to 3.6 V ($V_{CC} \geq V_{DD}$) , GND = V_{SS} = 0 V, Ta = –20 °C to +85 °C)

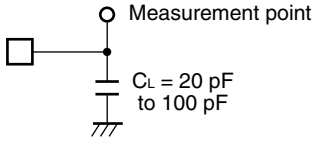
Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Output minimum voltage 1	V_{AOL1}	AO_1 to AO_{12}	V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AL} = 0 µA Digital data = #00	V_{SS}	—	V_{SS} + 0.1	V
Output minimum voltage 2	V_{AOL2}		V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AL} = 500 µA Digital data = #00	V_{SS} – 0.2	V_{SS}	V_{SS} + 0.2	V
Output minimum voltage 3	V_{AOL3}		V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AH} = 500 µA Digital data = #00	V_{SS}	—	V_{SS} + 0.2	V
Output minimum voltage 4	V_{AOL4}		V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AL} = 1.0 mA Digital data = #00	V_{SS} – 0.3	V_{SS}	V_{SS} + 0.3	V
Output minimum voltage 5	V_{AOL5}		V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AH} = 1.0 mA Digital data = #00	V_{SS}	—	V_{SS} + 0.3	V
Output maximum voltage 1	V_{AOH1}		V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AL} = 0 µA Digital data = #FF	V_{DD} – 0.1	—	V_{DD}	V
Output maximum voltage 2	V_{AOH2}		V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AL} = 500 µA Digital data = #FF	V_{DD} – 0.2	—	V_{DD}	V
Output maximum voltage 3	V_{AOH3}		V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AH} = 500 µA Digital data = #FF	V_{DD} – 0.2	V_{DD}	V_{DD} + 0.2	V
Output maximum voltage 4	V_{AOH4}		V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AL} = 1.0 mA Digital data = #FF	V_{DD} – 0.3	—	V_{DD}	V
Output maximum voltage 5	V_{AOH5}		V_{DD} = V_{CC} = 3.0 V, V_{SS} = GND = 0.0 V, I_{AH} = 1.0 mA Digital data = #FF	V_{DD} – 0.3	V_{DD}	V_{DD} + 0.3	V

2. AC Characteristics

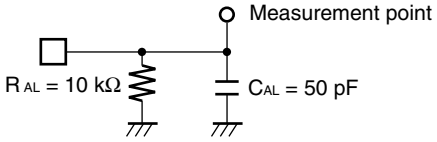
(V_{DD}, V_{CC} = 2.7 V to 3.6 V ($V_{CC} \geq V_{DD}$) , GND = V_{SS} = 0 V, Ta = − 20 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Clock L level pulse width	t_{CKL}	—	200	—	ns
Clock H level pulse width	t_{CKH}	—	200	—	ns
Clock rise time Clock fall time	t_{Cr} t_{Cf}	—	—	200	ns
Data setup time	t_{DCH}	—	30	—	ns
Data hold time	t_{CHD}	—	60	—	ns
Load setup time	t_{CHL}	—	200	—	ns
Load hold time	t_{LDC}	—	100	—	ns
Load H level pulse width	t_{LDH}	—	100	—	ns
Data output delay time	t_{DO}	Refer to "• Load condition 1"	70	600	ns
D/A output settling time	t_{LDD}	Refer to "• Load condition 2"	—	300	µs

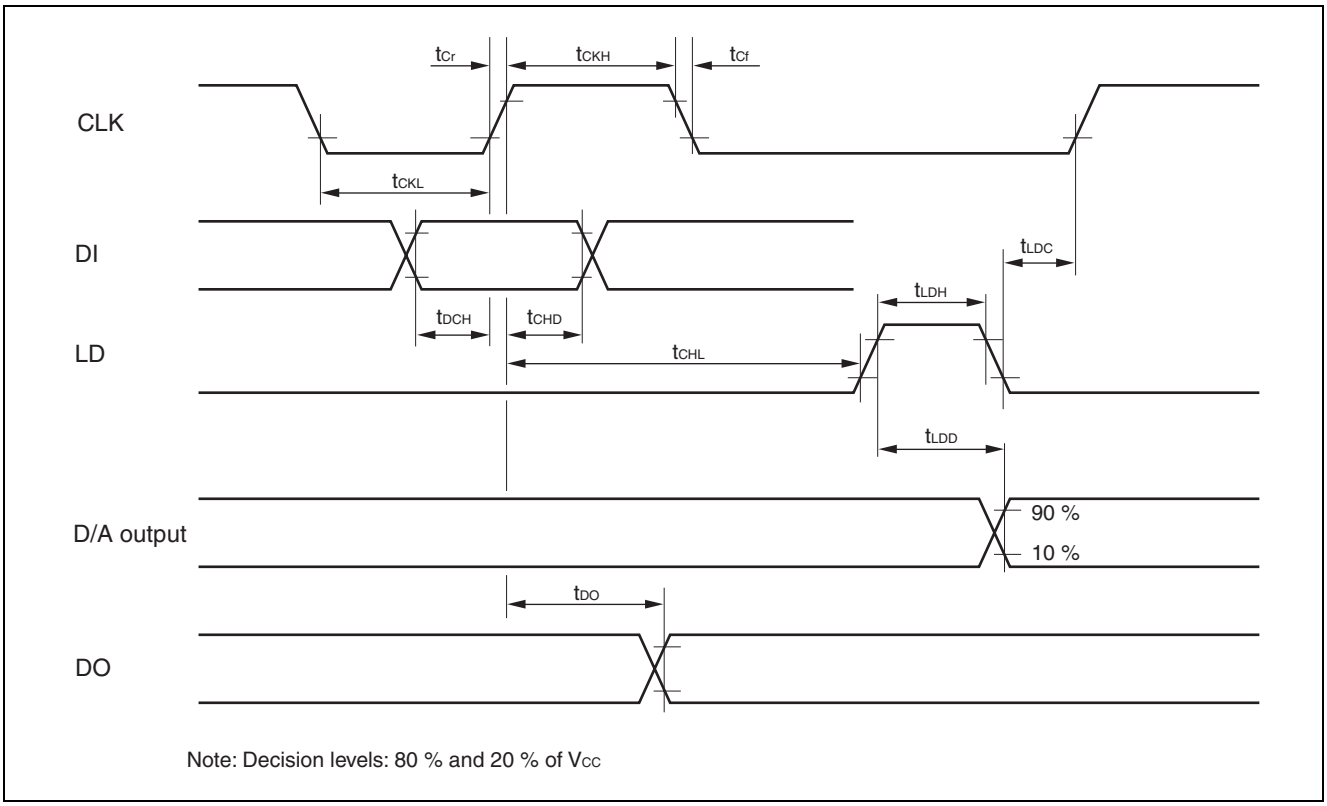
• Load condition 1



• Load condition 2

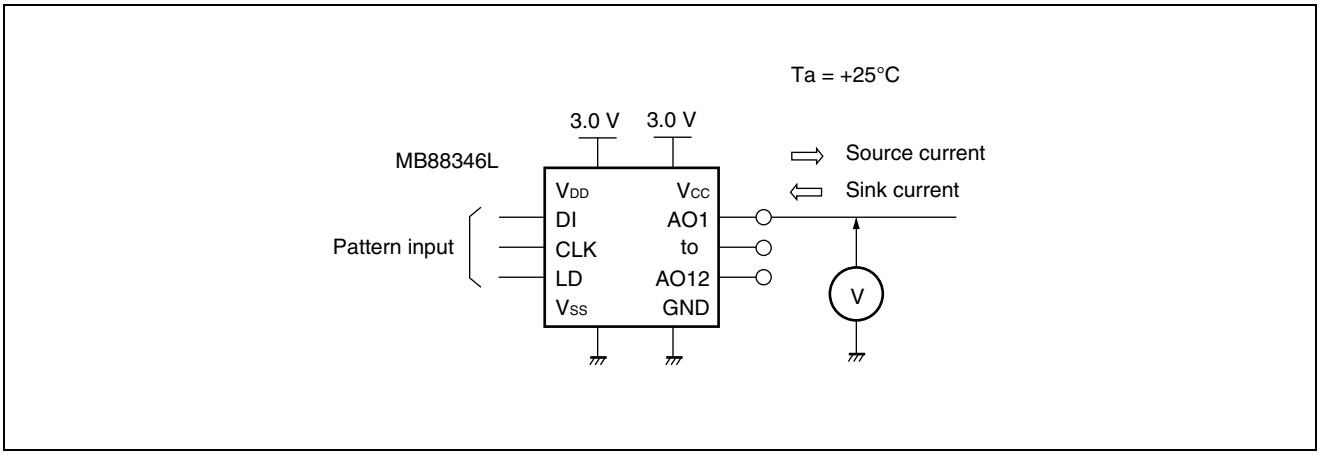


- **Input/output timing**



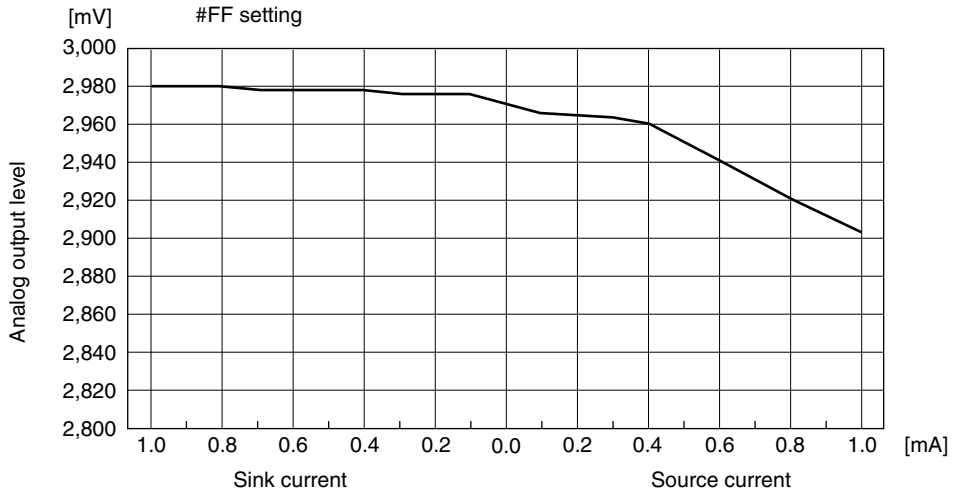
Note: Decision levels: 80 % and 20 % of V_{CC}

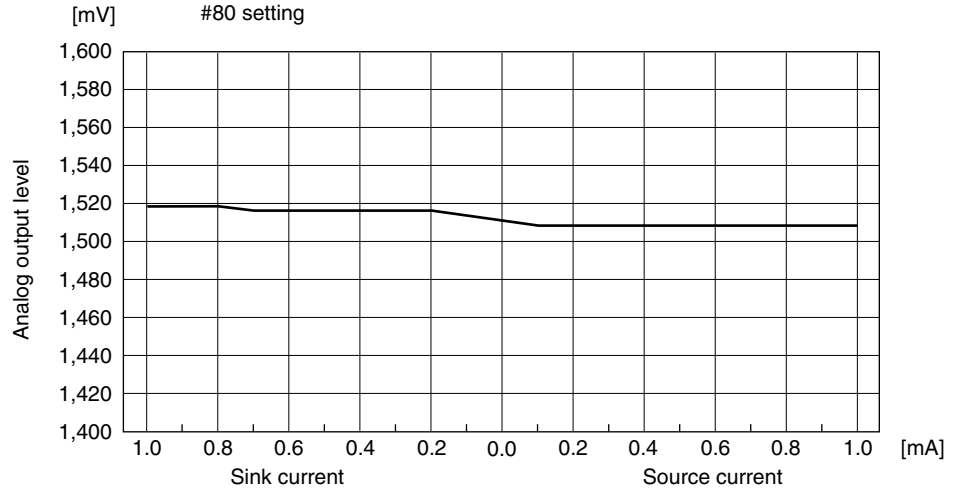
■ V_{AO} vs. I_{AO} CHARACTERISTICS : EXAMPLE

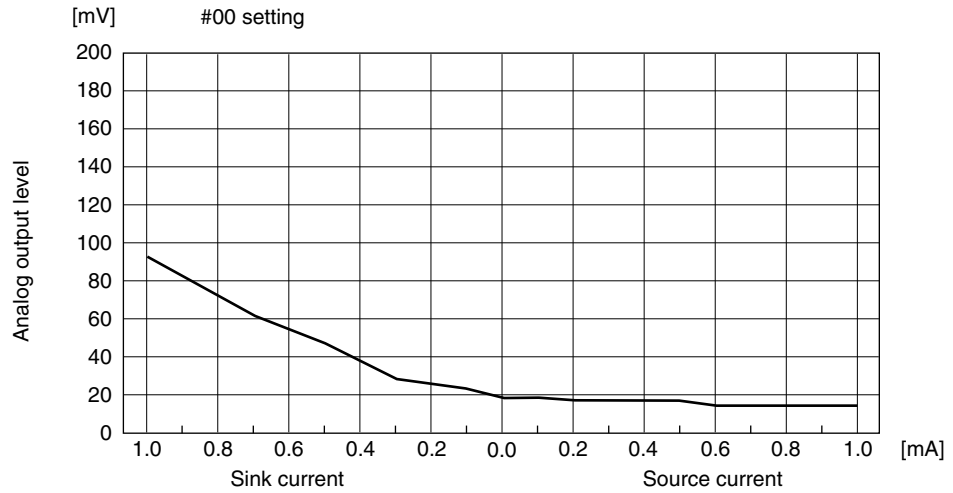


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[mV]
#FF setting
3,000
2,980
2,960
2,940
2,920
2,900
2,880
2,860
2,840
2,820
2,800
Analog output level
1.0 0.8 0.6 0.4 0.2 0.0 0.2 0.4 0.6 0.8 1.0
[mA]
Sink current
Source current

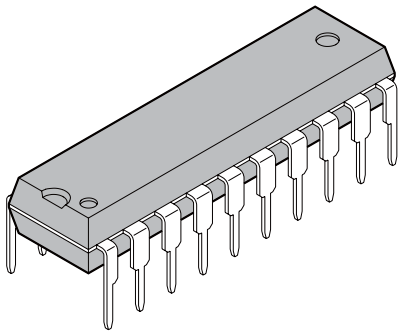

[mV]
#80 setting
1,600
1,580
1,560
1,540
1,520
1,500
1,480
1,460
1,440
1,420
1,400
Analog output level
1.0 0.8 0.6 0.4 0.2 0.0 0.2 0.4 0.6 0.8 1.0
[mA]
Sink current
Source current


[mV]
#00 setting
200
180
160
140
120
100
80
60
40
20
0
Analog output level
1.0 0.8 0.6 0.4 0.2 0.0 0.2 0.4 0.6 0.8 1.0
[mA]
Sink current
Source current

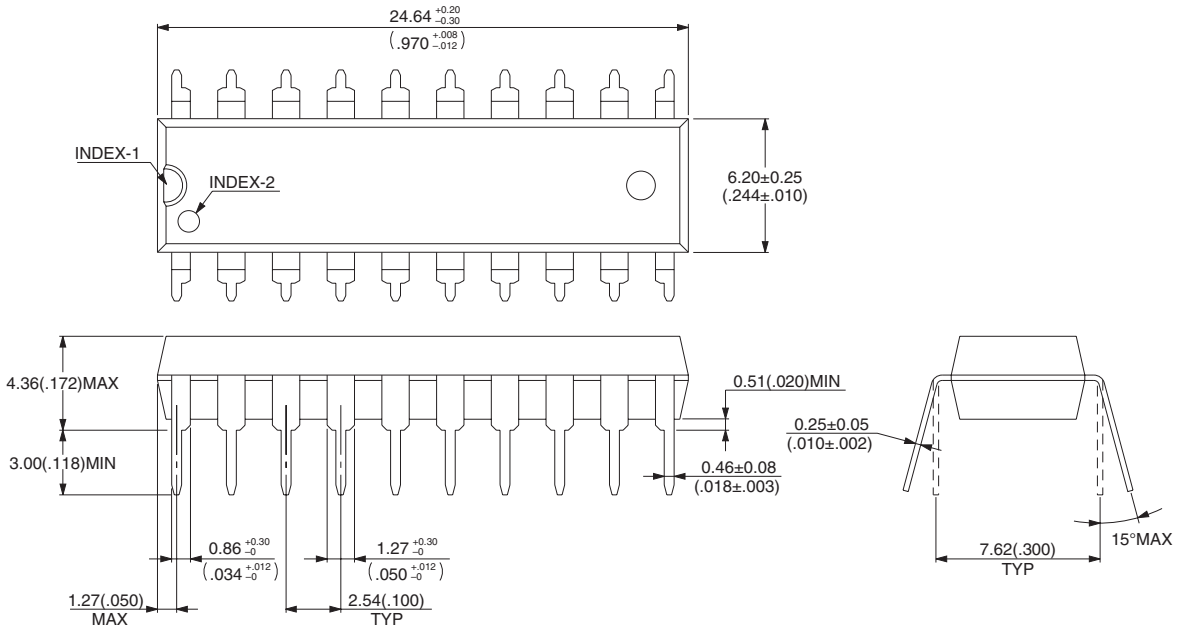
■ ORDERING INFORMATION

Part number	Package	Remarks
MB88346LP	20-pin plastic DIP (DIP-20P-M02)	
MB88346LPFV	20-pin plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSIONS

20-pin plastic DIP		
	Lead pitch	2.54mm(100mil)
	Row spacing	7.62mm(300mil)
	Sealing method	Plastic mold
(DIP-20P-M02)		

20-pin plastic DIP
(DIP-20P-M02)



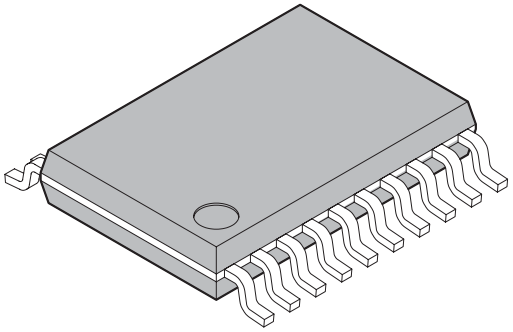
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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

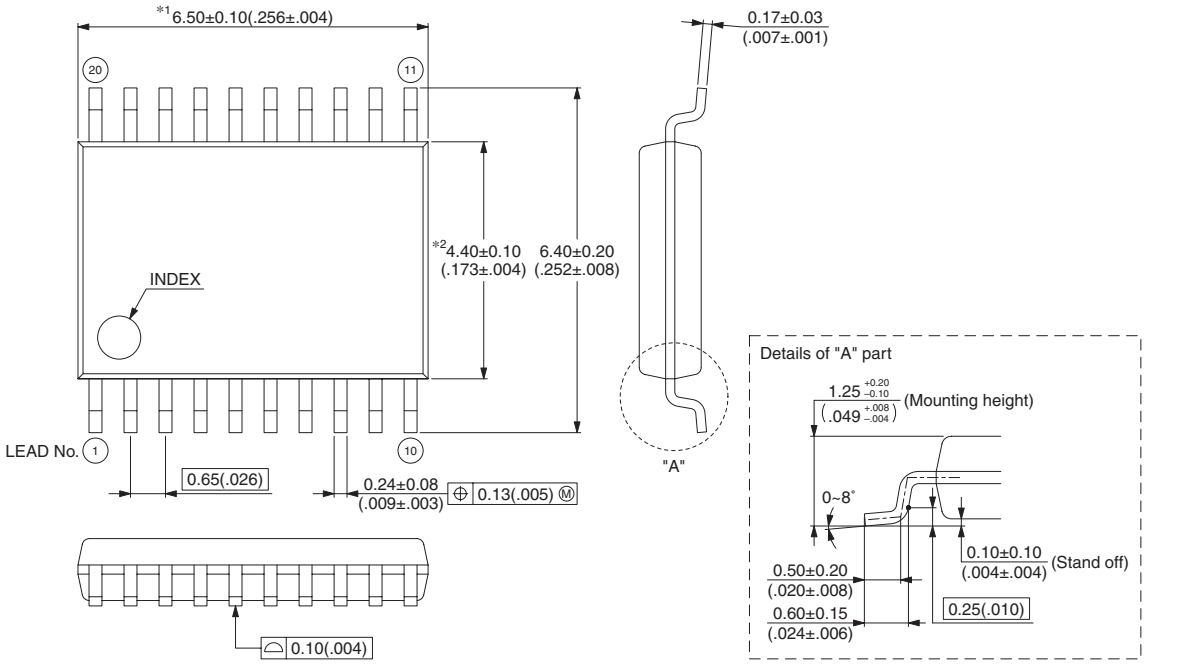
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20-pin plastic SSOP		
	Lead pitch	0.65 mm
	Package width × package length	4.40 × 6.50 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.45 mmMAX
	Weight	0.09g
(FPT-20P-M03)	Code (Reference)	P-SSOP20-4.4×6.5-0.65

20-pin plastic SSOP
(FPT-20P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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