19-5213; Rev 4; 4/10

Real-Time Clocks

DS12885/DS12887/DS12887A/DS12C887/DS12C887A

General Description

The DS12885, DS12887, and DS12C887 real-time clocks (RTCs) are designed to be direct replacements for the DS1285 and DS1287. The devices provide a real-time clock/calendar, one time-of-day alarm, three maskable interrupts with a common interrupt output, a programmable square wave, and 114 bytes of battery-backed static RAM (113 bytes in the DS12C887 and DS12C887A). The DS12887 integrates a quartz crystal and lithium energy source into a 24-pin encapsulated DIP package. The DS12C887 adds a century byte at address 32h. For all devices, the date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The devices also operate in either 24-hour or 12-hour format with an AM/PM indicator. A precision temperature-compensated circuit monitors the status of V_{CC}. If a primary power failure is detected, the device automatically switches to a backup supply. A lithium coin-cell battery can be connected to the V_{BAT} input pin on the DS12885 to maintain time and date operation when primary power is absent. The device is accessed through a multiplexed byte-wide interface, which supports both Intel and Motorola modes.

Applications

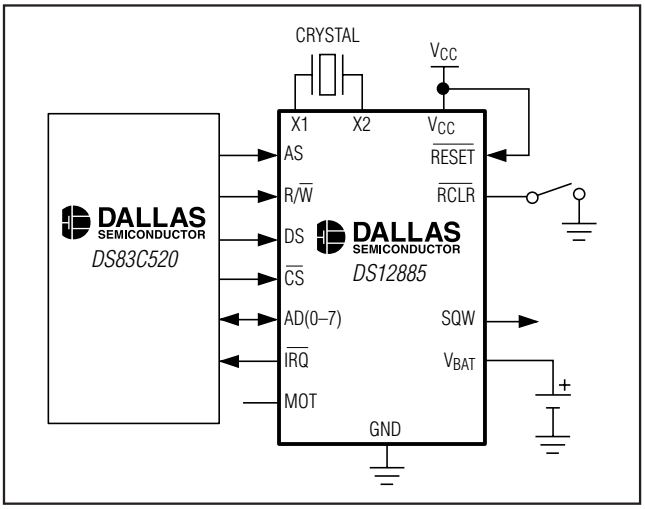
Embedded Systems

Utility Meters

Security Systems

Network Hubs, Bridges, and Routers

Typical Operating Circuit



Features

- Drop-In Replacement for IBM AT Computer Clock/Calendar
- RTC Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap Year Compensation Through 2099
- Binary or BCD Time Representation
- 12-Hour or 24-Hour Clock with AM and PM in 12-Hour Mode
- Daylight Saving Time Option
- Selectable Intel or Motorola Bus Timing
- Interfaced with Software as 128 RAM Locations
- 14 Bytes of Clock and Control Registers
- 114 Bytes of General-Purpose, Battery-Backed RAM (113 Bytes in the DS12C887 and DS12C887A)
- RAM Clear Function (DS12885, DS12887A, and DS12C887A)
- Interrupt Output with Three Independently Maskable Interrupt Flags
- Time-of-Day Alarm Once Per Second to Once Per Day
- Periodic Rates from 122µs to 500ms
- End-of-Clock Update Cycle Flag
- Programmable Square-Wave Output
- Automatic Power-Fail Detect and Switch Circuitry
- Optional 28-Pin PLCC Surface Mount Package or 32-Pin TQFP (DS12885)
- Optional Encapsulated DIP (EDIP) Package with Integrated Crystal and Battery (DS12887, DS12887A, DS12C887, DS12C887A)
- Optional Industrial Temperature Range Available
- Underwriters Laboratory (UL) Recognized

Pin Configurations and Ordering Information appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Real-Time Clocks

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Pin Relative to Ground .....-0.3V to +6.0V
Operating Temperature Range .....
Commercial (noncondensing) .....0°C to +70°C
Operating Temperature Range .....
Industrial (noncondensing).....-40°C to +85°C
Storage Temperature Range
EDIP .....-40°C to +85°C
PDIP, SO, PLCC, TQFP .....-55°C to +125°C

Lead Temperature (soldering, 10s) .....+260°C
(**Note:** EDIP is hand or wave-soldered only.)
Soldering Temperature (reflow)
PDIP, SO, PLCC.....+260°C
TQFP .....+245°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = +4.5V to +5.5V**, T_A = over the operating range, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 3)	4.5		5.5	V
V_{BAT} Input Voltage	V_{BAT}	(Note 3)	2.5		4.0	V
Input Logic 1	V_{IH}	(Note 3)	2.2		V_{CC} + 0.3	V
Input Logic 0	V_{IL}	(Note 3)	-0.3		+0.8	V
V_{CC} Power-Supply Current	I_{CC1}	(Note 4)			15	mA
V_{CC} Standby Current	I_{CCS}	(Note 5)				mA
Input Leakage	I_{IL}		-1.0		+1.0	µA
I/O Leakage	I_{OL}	(Note 6)	-1.0		+1.0	µA
Input Current	I_{MOT}	(Note 7)	-1.0		+500	µA
Output at 2.4V	I_{OH}	(Note 3)	-1.0			mA
Output at 0.4V	I_{OL}	(Note 3)			4.0	mA
Power-Fail Voltage	V_{PF}	(Note 3)	4.0	4.25	4.5	V
VRT Trip Point	VRT_{TRIP}			1.3		V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} **= 0V,** V_{BAT} **= 3.0V**, T_A = over the operating range, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BAT} Current (OSC On); T_A = +25°C, V_{BACKUP} = 3.0V	I_{BAT}	(Note 8)			500	nA
V_{BAT} Current (Oscillator Off)	I_{BATDR}	(Note 8)			100	nA

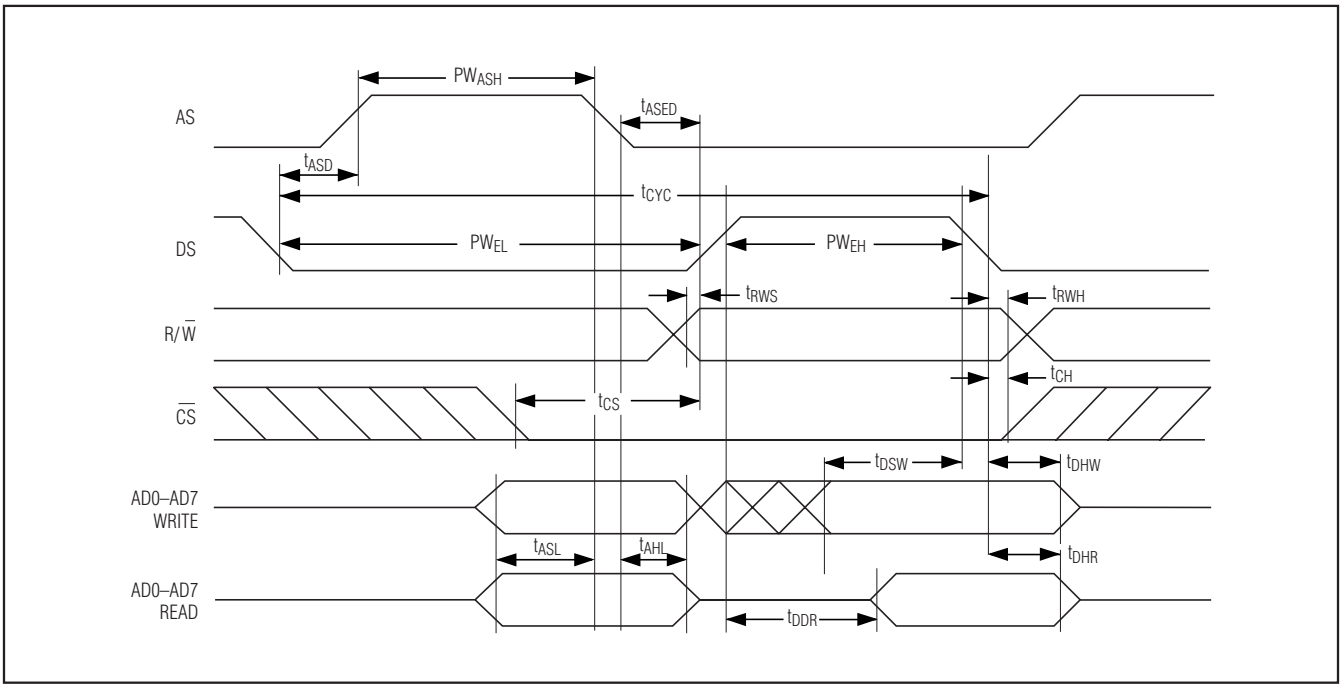
AC ELECTRICAL CHARACTERISTICS

(V_{CC} **= 4.5V to 5.5V**, T_A = over the operating range.) (Note 2)

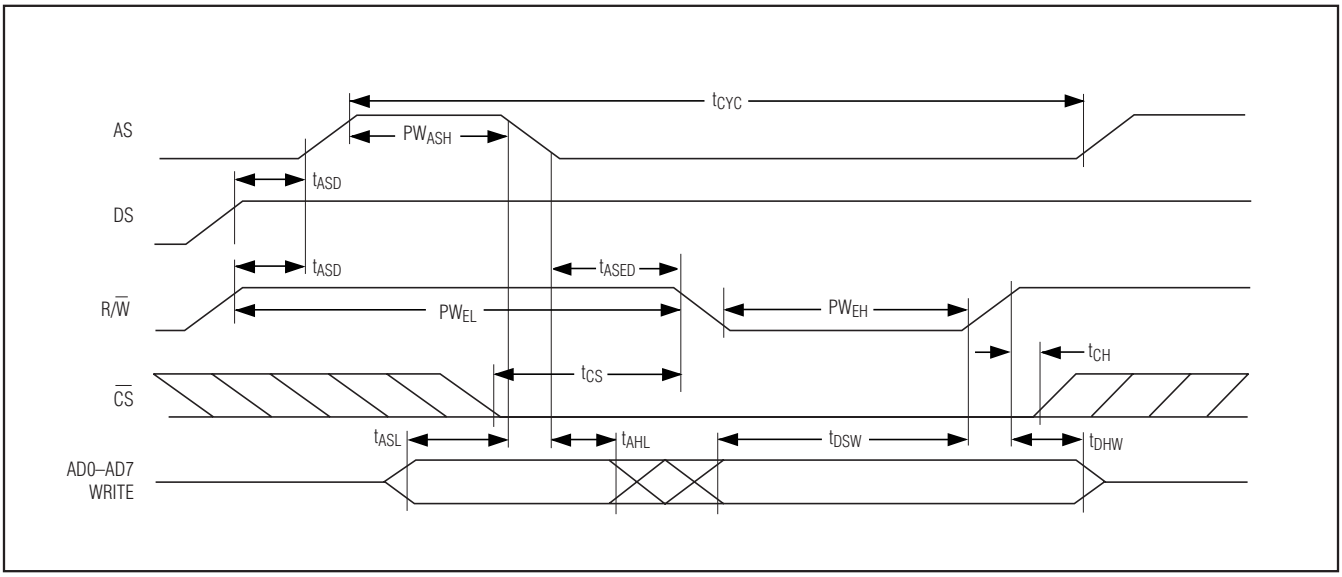
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time	t_{CYC}		385		DC	ns
Pulse Width, DS Low or R/$\overline{W}$ High	PW_{EL}		150			ns
Pulse Width, DS High or R/$\overline{W}$ Low	PW_{EH}		125			ns
Input Rise and Fall	t_R, t_F				30	ns
R/$\overline{W}$ Hold Time	t_{RWH}		10			ns
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}		50			ns
Chip-Select Setup Time Before DS or R/$\overline{W}$	t_{CS}		20			ns
Chip-Select Hold Time	t_{CH}		0			ns
Read-Data Hold Time	t_{DHR}		10		80	ns
Write-Data Hold Time	t_{DHW}		0			ns
Address Valid Time to AS Fall	t_{ASL}		30			ns
Address Hold Time to AS Fall	t_{AHL}		10			ns
Delay Time DS/E to AS Rise	t_{ASD}		20			ns
Pulse Width AS High	PW_{ASH}		60			ns
Delay Time, AS to DS/E Rise	t_{ASED}		40			ns
Output Data Delay Time from DS or R/$\overline{W}$	t_{DDR}		20		120	ns
Data Setup Time	t_{DSW}		100			ns
Reset Pulse Width	t_{RWL}		5			µs
$\overline{IRQ}$ Release from DS	t_{IRDS}				2	µs
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}				2	µs

Real-Time Clocks

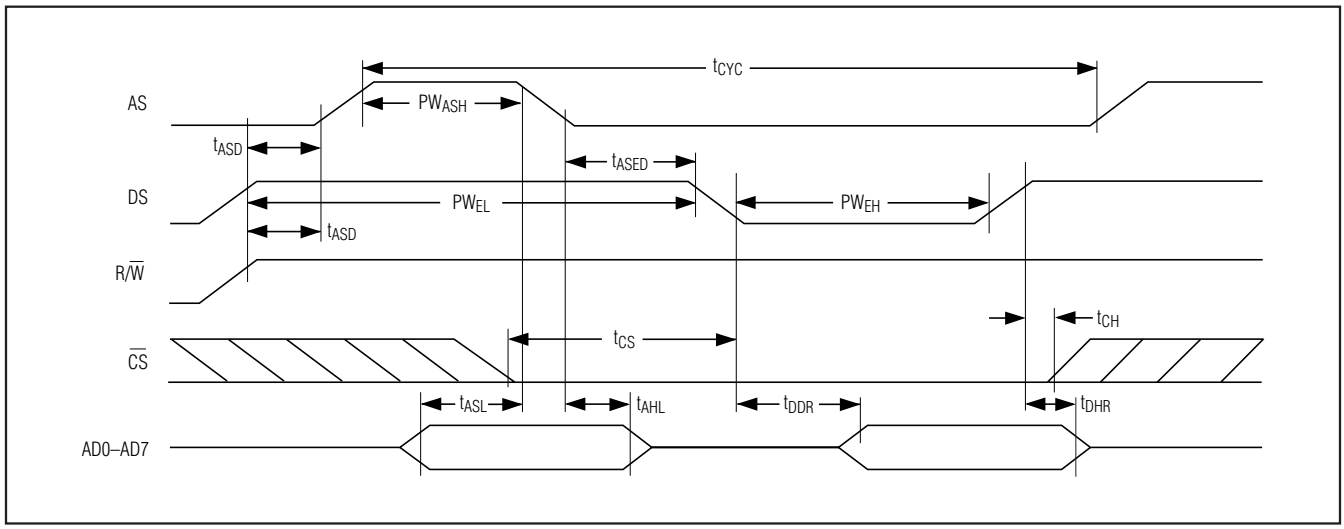
Motorola Bus Read/Write Timing



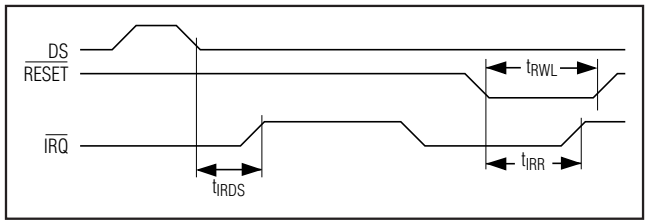
Intel Bus Write Timing



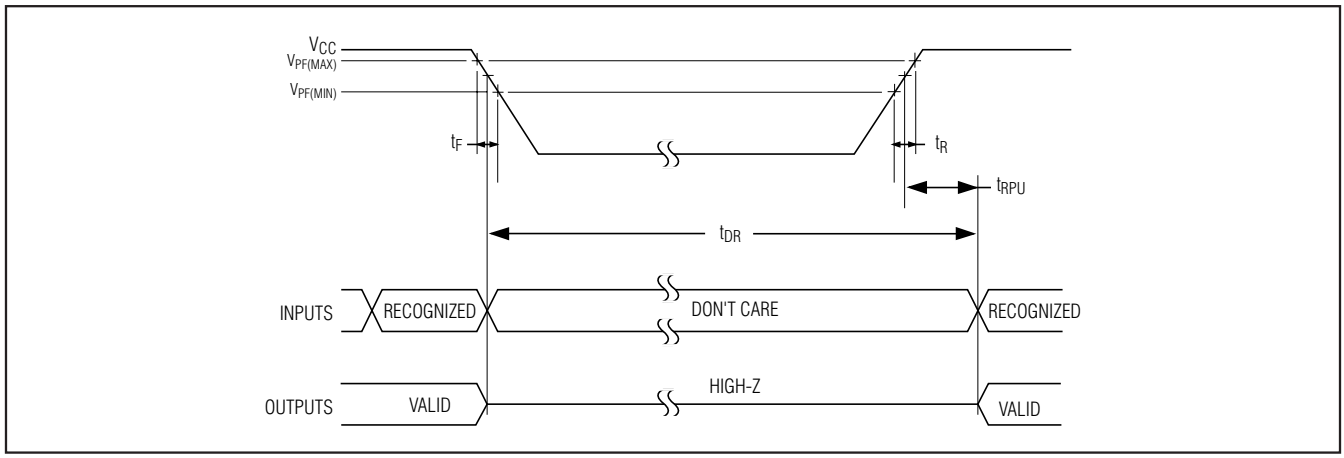
Intel Bus Read Timing



IRQ Release Delay Timing



Power-Up/Power-Down Timing



Real-Time Clocks

POWER-UP/POWER-DOWN CHARACTERISTICS

(T_A = -40°C to +85°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{RPU}		20		200	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R		0			µs

DATA RETENTION

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Expected Data Retention	t_{DR}		10			years

CAPACITANCE

(T_A = +25°C) (Note 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitance on All Input Pins Except X1 and X2	C_{IN}				5	pF
Capacitance on $\overline{IRQ}$, SQW, and DQ Pins	C_{IO}				7	pF

AC TEST CONDITIONS

PARAMETER	TEST CONDITIONS
Input Pulse Levels	0 to 3.0V
Output Load Including Scope and Jig	50pF + 1TTL Gate
Input and Output Timing Measurement Reference Levels	Input/Output: V_{IL} maximum and V_{IH} minimum
Input-Pulse Rise and Fall Times	5ns

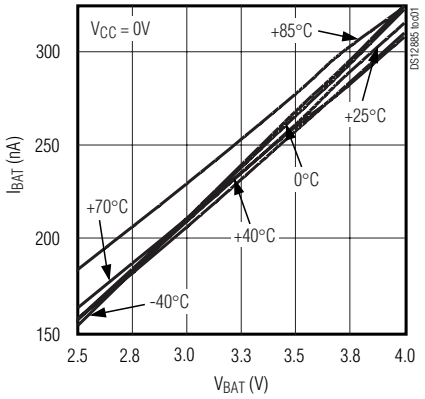
WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

Note 1: RTC modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. However, post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibrations are not used to prevent crystal damage.
Note 2: Limits at -40°C are guaranteed by design and not production tested.
Note 3: All voltages are referenced to ground.
Note 4: All outputs are open.
Note 5: Specified with $\overline{CS}$ = DS = R/$\overline{W}$ = $\overline{RESET}$ = V_{CC}; MOT, AS, AD0–AD7 = 0; V_{BACKUP} open.
Note 6: Applies to the AD0 to AD7 pins, the $\overline{IRQ}$ pin, and the SQW pin when each is in a high-impedance state.
Note 7: The MOT pin has an internal 20kΩ pulldown.
Note 8: Measured with a 32.768kHz crystal attached to X1 and X2.
Note 9: Guaranteed by design. Not production tested.
Note 10: Measured with a 50pF capacitance load.

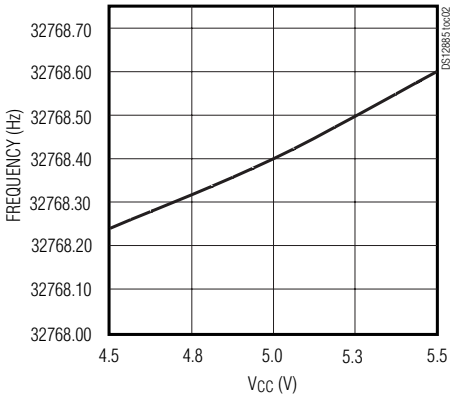
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

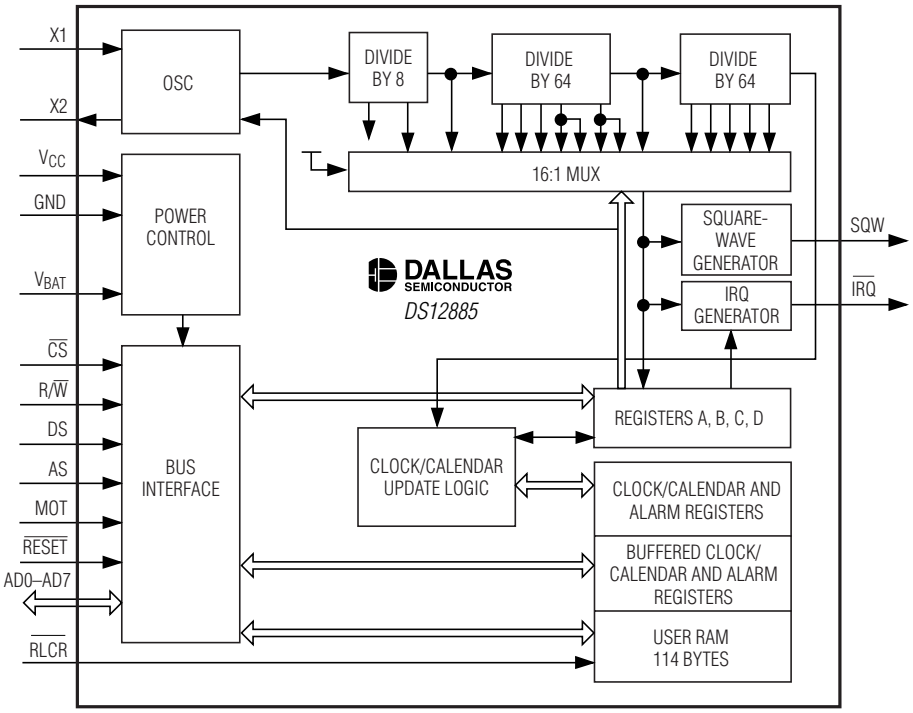
I_{BAT1} vs. V_{BAT} vs. TEMPERATURE



OSCILLATOR FREQUENCY vs. V_{CC}



Functional Diagram



Real-Time Clocks

Pin Description

PIN				NAME	FUNCTION
SO, PDIP	EDIP	PLCC	TQFP		
1	1	2	29	MOT	Motorola or Intel Bus Timing Selector. This pin selects one of two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pulldown resistor.
2	—	3	30	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a 6pF specified load capacitance (C_L). Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is left unconnected if an external oscillator is connected to pin X1.
3	—	4	31	X2	
4–11	4–11	5–10, 12, 14	1, 2, 3, 5, 7, 8, 9, 11	AD0–AD7	Multiplexed, Bidirectional Address/Data Bus. The addresses are presented during the first portion of the bus cycle and latched into the device by the falling edge of AS. Write data is latched by the falling edge of DS (Motorola timing) or the rising edge of R/$\overline{W}$ (Intel timing). In a read cycle, the device outputs data during the latter portion of DS (DS and R/$\overline{W}$ high for Motorola timing, DS low and R/$\overline{W}$ high for Intel timing). The read cycle is terminated and the bus returns to a high-impedance state as DS transitions low in the case of Motorola timing or as DS transitions high in the case of Intel timing.
12, 16	12	15, 20	12, 17	GND	Ground
13	13	16	13	$\overline{CS}$	Active-Low Chip-Select Input. The chip-select signal must be asserted low for a bus cycle in the device to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during DS and R/$\overline{W}$ for Intel timing. Bus cycles that take place without asserting $\overline{CS}$ will latch addresses, but no access occurs. When V_{CC} is below V_{PF} volts, the device inhibits access by internally disabling the $\overline{CS}$ input. This action protects the RTC data and the RAM data during power outages.
14	14	17	14	AS	Address Strobe Input. A positive-going address-strobe pulse serves to demultiplex the bus. The falling edge of AS causes the address to be latched within the device. The next rising edge that occurs on the AS bus clears the address regardless of whether $\overline{CS}$ is asserted. An address strobe must immediately precede each write or read access. If a write or read is performed with $\overline{CS}$ deasserted, another address strobe must be performed prior to a read or write access with $\overline{CS}$ asserted.
15	15	19	16	R/$\overline{W}$	Read/Write Input. The R/$\overline{W}$ pin has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is at a level that indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS. When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active-low signal. In this mode, the R/$\overline{W}$ pin operates in a similar fashion as the write-enable signal ($\overline{WE}$) on generic RAMs. Data are latched on the rising edge of the signal.

Pin Description (continued)

PIN				NAME	FUNCTION
SO, PDIP	EDIP	PLCC	TQFP		
22	2, 3, 16, 20, 21, 22	1, 11, 13, 18, 26	4, 6, 10, 15, 20, 23, 25, 27, 32	N.C.	No Connection. This pin should remain unconnected. Pin 21 is $\overline{RCLR}$ for the DS12887A/DS12C887A. On the EDIP, these pins are missing by design.
17	17	21	18	DS	Data Strobe or Read Input. The DS pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode, DS is a positive pulse during the latter portion of the bus cycle and is called data strobe. During read cycles, DS signifies the time that the device is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the device to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. DS identifies the time period when the device drives the bus with read data. In this mode, the DS pin operates in a similar fashion as the output-enable ($\overline{OE}$) signal on a generic RAM.
18	18	22	19	$\overline{RESET}$	Active-Low Reset Input. The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up, the $\overline{RESET}$ pin can be held low for a time to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power-up, the time $\overline{RESET}$ is low should exceed 200ms to ensure that the internal timer that controls the device on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above V_{PF}, the following occurs: A. Periodic interrupt-enable (PIE) bit is cleared to 0. B. Alarm interrupt-enable (AIE) bit is cleared to 0. C. Update-ended interrupt-enable (UIE) bit is cleared to 0. D. Periodic-interrupt flag (PF) bit is cleared to 0. E. Alarm-interrupt flag (AF) bit is cleared to 0. F. Update-ended interrupt flag (UF) bit is cleared to 0. G. Interrupt-request status flag (IRQF) bit is cleared to 0. H. $\overline{IRQ}$ pin is in the high-impedance state. I. The device is not accessible until $\overline{RESET}$ is returned high. J. Square-wave output-enable (SQWE) bit is cleared to 0. In a typical application, $\overline{RESET}$ can be connected to V_{CC}. This connection allows the device to go in and out of power fail without affecting any of the control registers.

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Pin Description (continued)

PIN				NAME	FUNCTION
SO, PDIP	EDIP	PLCC	TQFP		
19	19	23	21	$\overline{IRQ}$	Active-Low Interrupt Request Output. The $\overline{IRQ}$ pin is an active-low output of the device that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. The processor program normally reads the C register to clear the $\overline{IRQ}$ pin. The $\overline{RESET}$ pin also clears pending interrupts. When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus, provided that they are all open drain. The $\overline{IRQ}$ pin is an open-drain output and requires an external pullup resistor to V_{CC}.
20	—	24	22	V_{BAT}	Connection for a Primary Battery. (DS12885 Only.) Battery voltage must be held between the minimum and maximum limits for proper operation. If a backup supply is not supplied, V_{BAT} must be grounded. Connect the battery directly to the V_{BAT} pin. Diodes in series between the V_{BAT} pin and the battery may prevent proper operation. UL recognized to ensure against reverse charging when used with a lithium battery.
21	21 (DS12887A/ DS12C887A)	25	24	$\overline{RCLR}$	Active-Low RAM Clear. The $\overline{RCLR}$ pin is used to clear (set to logic 1) all the general-purpose RAM, but does not affect the RAM associated with the RTC. To clear the RAM, $\overline{RCLR}$ must be forced to an input logic 0 during battery-backup mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used through a human interface (shorting to ground manually or by a switch) and not to be driven with external buffers. This pin is internally pulled up. Do not use an external pullup resistor on this pin.
23	23	27	26	SQW	Square-Wave Output. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the RTC. The frequency of the SQW pin can be changed by programming Register A, as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than V_{PF}.
24	24	28	28	V_{CC}	DC Power Pin for Primary Power Supply. When V_{CC} is applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below V_{PF} reads and writes are inhibited.

Detailed Description

The DS12885 family of RTCs provide 14 bytes of real-time clock/calendar, alarm, and control/status registers and 114 bytes (113 bytes for DS12C887 and DS12C887A) of nonvolatile, battery-backed static RAM. A time-of-day alarm, three maskable interrupts with a common interrupt output, and a programmable square-wave output are available. The devices also operate in either 24-hour or 12-hour format with an AM/PM indicator. A precision temperature-compensated circuit monitors the status of V_{CC}. If a primary power-supply failure is detected, the devices automatically switch to a backup supply. The backup supply input supports a primary battery, such as lithium coin cell. The devices are accessed through a multiplexed address/data bus that supports Intel and Motorola modes.

Oscillator Circuit

The DS12885 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 1 shows a functional schematic of the oscillator circuit. An enable bit in the control register controls the oscillator. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within one second.

An external 32.768kHz oscillator can also drive the DS12885. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left unconnected.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

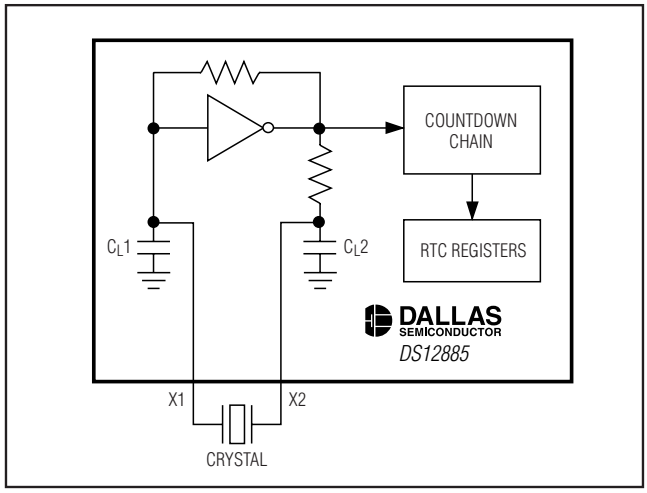


Figure 1. Oscillator Circuit Showing Internal Bias Network

Real-Time Clocks

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 2 shows a typical PC board layout for isolation of the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for more detailed information.

Clock Accuracy for DS12887, DS12887A, DS12C887, DS12C887A Only

The encapsulated DIP modules are trimmed at the factory to an accuracy of ±1 minute per month at +25°C.

Power-Down/Power-Up Considerations

The real-time clock continues to operate, and the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the V_{CC} input level. V_{BAT} must remain within the minimum and maximum limits when V_{CC} is not applied. When V_{CC} is applied and exceeds V_{PF} (power-fail trip point), the device becomes accessible after t_{REC}—if the oscillator is running and the oscillator countdown chain is not in reset (Register A). This time allows the system to stablize after power is applied. If the oscillator is not enabled, the oscillator-enable bit is enabled on power-up, and the device becomes immediately accessible.

Time, Calendar, and Alarm Locations

The time and calendar information is obtained by reading the appropriate register bytes. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. Invalid time or date entries result in undefined operation. The contents of the 10 time, calendar, and alarm bytes can be either binary or binary-coded decimal (BCD) format.

The day-of-week register increments at midnight, incrementing from 1 through 7. The day-of-week register is used by the daylight saving function, so the value 1 is defined as Sunday. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years.

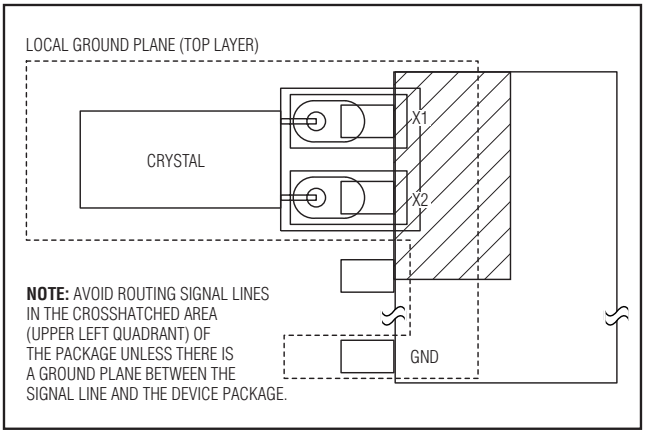


Figure 2. Layout Example

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to logic 1 to prevent updates from occurring while access is being attempted. In addition to writing the 10 time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All 10 time, calendar, and alarm bytes must use the same data mode. The SET bit in Register B should be cleared after the data mode bit has been written to allow the RTC to update the time and calendar bytes. Once initialized, the RTC makes all updates in the selected mode. The data mode cannot be changed without reinitializing the 10 data bytes. Tables 2A and 2B show the BCD and binary formats of the time, calendar, and alarm locations.

The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the higher-order bit of the hours byte represents PM when it is logic 1. The time, calendar, and alarm bytes are always accessible because they are double-buffered. Once per second the seven bytes are advanced by one second and checked for an alarm condition.

If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day, if the alarm-enable bit is high. In this mode, the "0" bits in the alarm registers and the corresponding time registers must always be written to 0 (Table 2A and 2B). Writing the 0 bits in the alarm and/or time registers to 1 can result in undefined operation.

The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The don't-care code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the don't-care condition when at logic 1. An alarm is generated each hour when the don't-care bits are set in the hours byte. Similarly, an alarm is generated every minute with don't-care codes in the hours and minute alarm bytes. The don't-care codes in all three alarm bytes create an interrupt every second.

All 128 bytes can be directly written or read, except for the following:

1) Registers C and D are read-only.
2) Bit 7 of register A is read-only.
3) The MSB of the seconds byte is read-only.

Table 2A. Time, Calendar, and Alarm Data Modes—BCD Mode (DM = 0)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	10 Seconds			Seconds				Seconds	00–59
01H	0	10 Seconds			Seconds				Seconds Alarm	00–59
02H	0	10 Minutes			Minutes				Minutes	00–59
03H	0	10 Minutes			Minutes				Minutes Alarm	00–59
04H	AM/PM	0	0	10 Hours	Hours				Hours	1–12 +AM/PM
	0		10 Hours							00–23
05H	AM/PM	0	0	10 Hours	Hours				Hours Alarm	1–12 +AM/PM
	0		10 Hours							00–23
06H	0	0	0	0	0	Day			Day	01–07
07H	0	0	10 Date		Date				Date	01–31
08H	0	0	0	10 Months	Month				Month	01–12
09H	10 Years				Year				Year	00–99
0AH	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	—
0BH	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	—
0CH	IRQF	PF	AF	UF	0	0	0	0	Control	—
0DH	VRT	0	0	0	0	0	0	0	Control	—
0EH-31H	X	X	X	X	X	X	X	X	RAM	—
32H	10 Century				Century				Century*	00–99
33H-7FH	X	X	X	X	X	X	X	X	RAM	—

X = Read/Write Bit.

**DS12C887, DS12C887A only. General-purpose RAM on DS12885, DS12887, and DS12887A.*

***Note:** Unless otherwise specified, the state of the registers is not defined when power is first applied. Except for the seconds register, 0 bits in the time and date registers can be written to 1, but may be modified when the clock updates. 0 bits should always be written to 0 except for alarm mask bits.*

Real-Time Clocks

Table 2B. Time, Calendar, and Alarm Data Modes—Binary Mode (DM = 1)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	0	Seconds						Seconds	00–3B
01H	0	0	Seconds						Seconds Alarm	00–3B
02H	0	0	Minutes						Minutes	00–3B
03H	0	0	Minutes						Minutes Alarm	00–3B
04H	AM/PM	0	0	0	Hours				Hours	01–0C +AM/PM
	0			Hours						00–17
05H	AM/PM	0	0	0	Hours				Hours Alarm	01–0C +AM/PM
	0			Hours						00–17
06H	0	0	0	0	0		Day		Day	01–07
07H	0	0	0	Date					Date	01–1F
08H	0	0	0	0	Month				Month	01–0C
09H	0	Year							Year	00–63
0AH	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	—
0BH	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	—
0CH	IRQF	PF	AF	UF	0	0	0	0	Control	—
0DH	VRT	0	0	0	0	0	0	0	Control	—
0EH-31H	X	X	X	X	X	X	X	X	RAM	—
32H	N/A				N/A				Century*	—
33H-7FH	X	X	X	X	X	X	X	X	RAM	—

X = Read/Write Bit.

**DS12C887, DS12C887A only. General-purpose RAM on DS12885, DS12887, and DS12887A.*

***Note:** Unless otherwise specified, the state of the registers is not defined when power is first applied. Except for the seconds register, 0 bits in the time and date registers can be written to 1, but may be modified when the clock updates. 0 bits should always be written to 0 except for alarm mask bits.*

Control Registers

The real-time clocks have four control registers that are accessible at all times, even during the update cycle.

Control Register A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Bit 7: Update-In-Progress (UIP). This bit is a status flag that can be monitored. When the UIP bit is a 1, the update transfer occurs soon. When UIP is a 0, the update transfer does not occur for at least 244µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read-only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a 1 inhibits any update transfer and clears the UIP status bit.

Bits 6, 5, and 4: DV2, DV1, DV0. These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that turn the oscillator on and allow the RTC to keep time. A pattern of 11x enables the oscillator but holds the countdown chain in reset. The next update occurs at 500ms after a pattern of 010 is written to DV0, DV1, and DV2.

Bits 3 to 0: Rate Selector (RS3, RS2, RS1, RS0). These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1) Enable the interrupt with the PIE bit;
2) Enable the SQW output pin with the SQWE bit;
3) Enable both at the same time and the same rate; or
4) Enable neither.

Table 3 lists the periodic interrupt rates and the square-wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

Real-Time Clocks

Control Register B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

Bit 7: SET. When the SET bit is 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to 1, any update transfer is inhibited, and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit and is not affected by $\overline{\text{RESET}}$ or internal functions of the device.

Bit 6: Periodic Interrupt Enable (PIE). The PIE bit is a read/write bit that allows the periodic interrupt flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3–RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the PF bit is still set at the periodic rate. PIE is not modified by any internal device functions, but is cleared to 0 on $\overline{\text{RESET}}$.

Bit 5: Alarm Interrupt Enable (AIE). This bit is a read/write bit that, when set to 1, permits the alarm flag (AF) bit in Register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes, including a don't-care alarm code of binary 11XXXXXX. The AF bit does not initiate the $\overline{\text{IRQ}}$ signal when the AIE bit is set to 0. The internal functions of the device do not affect the AIE bit, but is cleared to 0 on $\overline{\text{RESET}}$.

Bit 4: Update-Ended Interrupt Enable (UIE). This bit is a read/write bit that enables the update-end flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the UIE bit.

The internal functions of the device do not affect the UIE bit, but is cleared to 0 on $\overline{\text{RESET}}$.

Bit 3: Square-Wave Enable (SQWE). When this bit is set to 1, a square-wave signal at the frequency set by the rate-selection bits RS3–RS0 is driven out on the SQW pin. When the SQWE bit is set to 0, the SQW pin is held low. SQWE is a read/write bit and is cleared by $\overline{\text{RESET}}$. SQWE is low if disabled, and is high impedance when V_{CC} is below V_{PF}. SQWE is cleared to 0 on $\overline{\text{RESET}}$.

Bit 2: Data Mode (DM). This bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A 1 in DM signifies binary data, while a 0 in DM specifies BCD data.

Bit 1: 24/12. The 24/12 control bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write and is not affected by internal functions or $\overline{\text{RESET}}$.

Bit 0: Daylight Saving Enable (DSE). This bit is a read/write bit that enables two daylight saving adjustments when DSE is set to 1. On the first Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM, it changes to 1:00:00 AM. When DSE is enabled, the internal logic test for the first/last Sunday condition at midnight. If the DSE bit is not set when the test occurs, the daylight saving function does not operate correctly. These adjustments do not occur when the DSE bit is 0. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

Control Register C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

Bit 7: Interrupt Request Flag (IRQF). This bit is set to 1 when any of the following are true:

PF = PIE = 1

AF = AIE = 1

UF = UIE = 1

Any time the IRQF bit is 1, the $\overline{IRQ}$ pin is driven low. This bit can be cleared by reading Register C or with a $\overline{RESET}$.

Bit 6: Periodic Interrupt Flag (PF). This bit is read-only and is set to 1 when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to 1 independent of the state of the PIE bit. When both PF and PIE are 1s, the $\overline{IRQ}$ signal is active and sets the IRQF bit. This bit can be cleared by reading Register C or with a $\overline{RESET}$.

Bit 5: Alarm Interrupt Flag (AF). A 1 in the AF bit indicates that the current time has matched the alarm time. If the AIE bit is also 1, the $\overline{IRQ}$ pin goes low and a 1 appears in the IRQF bit. This bit can be cleared by reading Register C or with a $\overline{RESET}$.

Bit 5: Update-Ended Interrupt Flag (UF). This bit is set after each update cycle. When the UIE bit is set to 1, the 1 in UF causes the IRQF bit to be a 1, which asserts the $\overline{IRQ}$ pin. This bit can be cleared by reading Register C or with a $\overline{RESET}$.

Bits 3 to 0: Unused. These bits are unused in Register C. These bits always read 0 and cannot be written.

Control Register D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

Bit 7: Valid RAM and Time (VRT). This bit indicates the condition of the battery connected to the V_{BAT} pin. This bit is not writeable and should always be 1 when read. If a 0 is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RESET}$.

Bits 6 to 0: Unused. The remaining bits of Register D are not usable. They cannot be written and they always read 0.

Real-Time Clocks

Century Register (DS12C887/DS12C887A Only)

The century register at location 32h is a BCD register designed to automatically load the BCD value 20 as the year register changes from 99 to 00. The MSB of this register is not affected when the load of 20 occurs, and remains at the value written by the user.

Nonvolatile RAM (NV RAM)

The general-purpose NV RAM bytes are not dedicated to any special function within the device. They can be used by the processor program as battery-backed memory and are fully available during the update cycle.

Interrupts

The RTC family includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500ms to 122µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit that software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits that are set remain stable throughout the read cycle. All bits that are set (high) are cleared when read, and new interrupts that are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each used flag bit should be examined when Register C is read to ensure that no interrupts are lost.

The second flag bit method is used with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt-enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic 1 in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the device. The act of reading Register C clears all active flag bits and the IRQF bit.

Oscillator Control Bits

When the DS12887, DS12887A, DS12C887, and DS12C887A are shipped from the factory, the internal oscillator is turned off. This prevents the lithium energy cell from being used until the device is installed in a system.

A pattern of 010 in bits 4 to 6 of Register A turns the oscillator on and enables the countdown chain. A pattern of 11x (DV2 = 1, DV1 = 1, DV0 = X) turns the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 to 6 keep the oscillator off.

Square-Wave Output Selection

Thirteen of the 15 divider taps are made available to a 1-of-16 multiplexer, as shown in the functional diagram. The square-wave and periodic-interrupt generators share the output of the multiplexer. The RS0–RS3 bits in Register A establish the output frequency of the multiplexer (see Table 1). Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square-wave enable bit, SQWE.

Periodic Interrupt Selection

The periodic interrupt causes the $\overline{IRQ}$ pin to go to an active state from once every 500ms to once every 122µs. This function is separate from the alarm interrupt, which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits that select the square-wave frequency (Table 1). Changing the Register A bits affects the square-wave frequency and the periodic-interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square-wave output. Similarly, the PIE bit in Register B enables the periodic interrupt. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

Table 3. Periodic Interrupt Rate and Square-Wave Output Frequency

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625ms	256Hz
0	0	1	0	7.8125ms	128Hz
0	0	1	1	122.070µs	8.192kHz
0	1	0	0	244.141µs	4.096kHz
0	1	0	1	488.281µs	2.048kHz
0	1	1	0	976.5625µs	1.024kHz
0	1	1	1	1.953125ms	512Hz
1	0	0	0	3.90625ms	256Hz
1	0	0	1	7.8125ms	128Hz
1	0	1	0	15.625ms	64Hz
1	0	1	1	31.25ms	32Hz
1	1	0	0	62.5ms	16Hz
1	1	0	1	125ms	8Hz
1	1	1	0	250ms	4Hz
1	1	1	1	500ms	2Hz

Update Cycle

The device executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to 1, the user copy of the double-buffered time, calendar, and alarm bytes is frozen and does not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers, and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a don't-care code is present in all three positions.

There are three methods that can handle RTC access that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates over 999ms is available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit pulses once per second. After the UIP bit goes high, the update transfer occurs 244µs later. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data is changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (Figure 3). Periodic interrupts that occur at a rate greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within one ($t_{PI/2}$ + t_{BUC}) to ensure that data is not read during the update cycle.

Handling, PC Board Layout, and Assembly

The EDIP module can be successfully processed through conventional wave-soldering techniques so long as temperature exposure to the lithium energy source does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used. Such cleaning can damage the crystal.

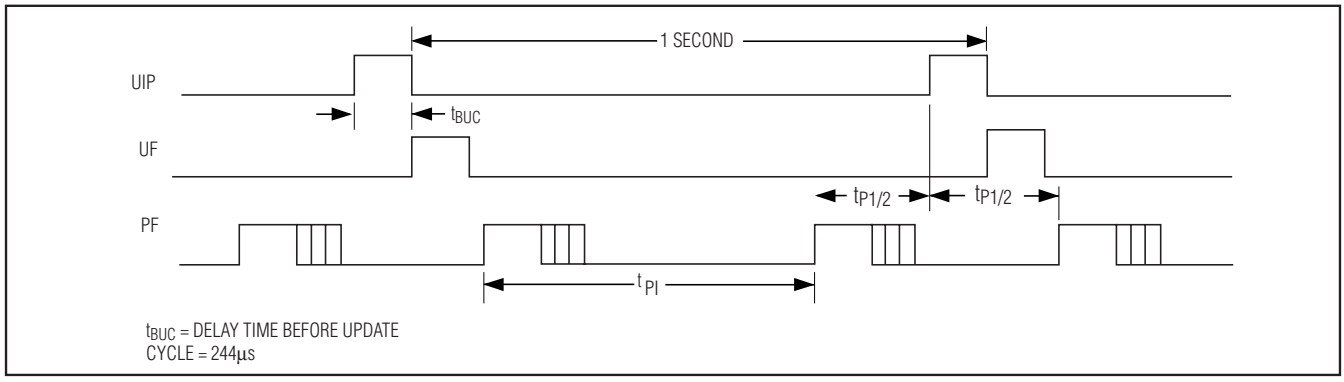
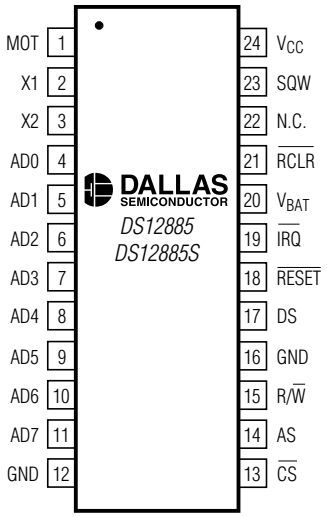


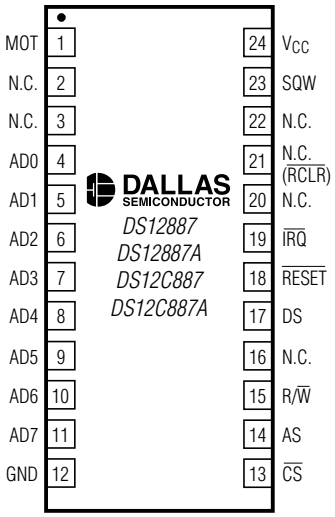
Figure 3. UIP and Periodic Interrupt Timing

Pin Configurations

TOP VIEW

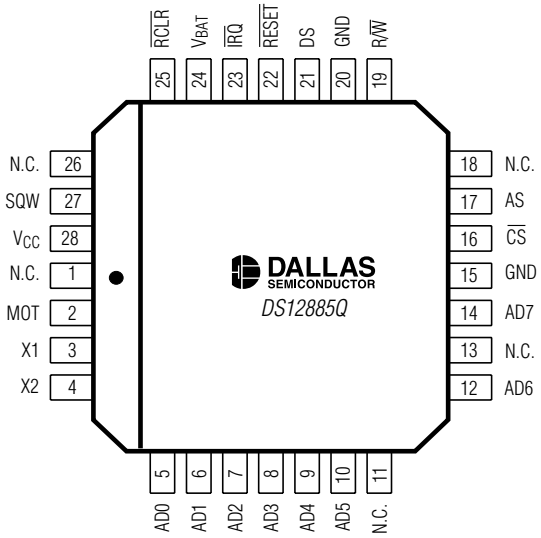


SO, PDIP



EDIP

( ) FOR THE DS12887A/DS12C887A.



PLCC

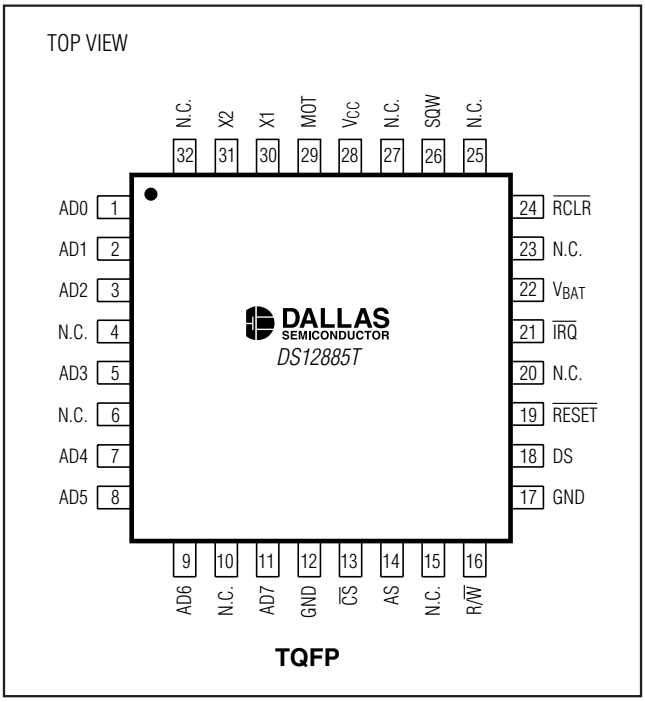
NOTE: THE DS12887A AND DS12C887A CANNOT BE STORED OR SHIPPED IN CONDUCTIVE MATERIAL THAT WILL GIVE A CONTINUITY PATH BETWEEN THE RAM CLEAR PIN AND GROUND.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK*
DS12885+	0°C to +70°C	24 PDIP	DS12885
DS12885N+	-40°C to +85°C	24 PDIP	DS12885
DS12885Q+	0°C to +70°C	28 PLCC	DS12885Q
DS12885QN+	-40°C to +85°C	28 PLCC	DS12885Q
DS12885Q+T&R	0°C to +70°C	28 PLCC	DS12885Q
DS12885QN+T&R	-40°C to +85°C	28 PLCC	DS12885Q
DS12885S+	0°C to +70°C	24 SO (300 mils)	DS12885S
DS12885SN+	-40°C to +85°C	24 SO (300 mils)	DS12885S
DS12885S+T&R	0°C to +70°C	24 SO (300 mils)	DS12885S
DS12885T+	0°C to +70°C	32 TQFP	DS12885
DS12885TN+	-40°C to +85°C	32 TQFP	DS12885
DS12887+	0°C to +70°C	24 EDIP	DS12887
DS12887A+	0°C to +70°C	24 EDIP	DS12887A
DS12C887+	0°C to +70°C	24 EDIP	DS12C887
DS12C887A+	0°C to +70°C	24 EDIP	DS12C887AA

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**A "+" anywhere on the top mark indicates a lead(Pb)-free device, and an "N" indicates an industrial temperature range device.*

Pin Configurations (continued)



Thermal Information

PACKAGE	THETA-JA (°C/W)	THETA-JC (°C/W)
PDIP	75	30
SO	105	22
PLCC	95	25

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 SO	W24+1	**21-0042**
24 PDIP	P24+4	**21-0044**
24 EDIP	MDP24+1	**21-0241**
28 PLCC	Q28+13	**21-0049**
32 TQFP	C32+3	**21-0292**

Chip Information

PROCESS: CMOS

SUBSTRATE CONNECTED TO GROUND

Real-Time Clocks

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/05	Initial release of combined data sheet	—
1	4/06	Corrected the *Intel Bus Write Timing*, *Intel Bus Read Timing*, *$\overline{IRQ}$ Release Delay Timing*, *Power-Up/Down Timing*, and *Functional Diagram* diagrams; added the *Handling, PC Board Layout*, and *Assembly* section.	4, 5, 7, 20
2	5/06	Corrected the *Intel Bus Write Timing* diagram; added PLCC pin description information; changed pin 16 from N.C. to GND for the SO and PDIP packages.	4, 8, 9, 10, 20
3	2/07	Corrected the *Intel Bus Write Timing* diagram; updated the *Ordering Information*; added the *Package Information* table; removed the package drawings.	4, 20, 22–27
4	4/10	Updated the storage temperature ranges, added the lead temperature, and updated the soldering temperature for all packages in the *Absolute Maximum Ratings*; removed leaded parts from the *Ordering Information* table.	2, 21

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