Preliminary Data Sheet

Hybrid Power Module

Integrated Power Stage for 230 VAC Motor Drives

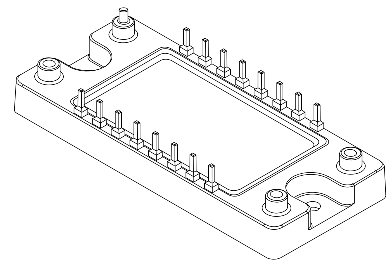
MHPM6B10A60D
MHPM6B20A60D

Motorola Preferred Devices

10, 20 AMP, 600 V
HYBRID POWER MODULES

These modules integrate a 3–phase inverter in a single convenient package. They are designed for 1.0 and 2.0 hp motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimum performance. The top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- UL Recognized



PRELIMINARY

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
IGBT Reverse Voltage		V_{CES}	600	V
Gate-Emitter Voltage		V_{GES}	± 20	V
Continuous IGBT Collector Current	10A60 20A60	I_{Cmax}	10 20	A
Peak Repetitive IGBT Collector Current (1)	10A60 20A60	$I_{C(pk)}$	20 40	A
Continuous Diode Current	10A60 20A60	I_{Fmax}	10 20	A
Peak Repetitive Diode Current (1)	10A60 20A60	$I_{F(pk)}$	20 40	A
IGBT Power Dissipation (T_C = 25°C)	10A60 20A60	P_D	52 78	W
Diode Power Dissipation (T_C = 25°C)	10A60 20A60	P_D	19 38	W
IGBT Power Dissipation (T_C = 95°C)	10A60 20A60	P_D	23 34	W
Diode Power Dissipation (T_C = 95°C)	10A60 20A60	P_D	8.3 17	W
Junction Temperature Range		T_J	– 40 to +150	°C
Short Circuit Duration (V_{CC} = 300 V, T_J = 125°C)		t_{sc}	10	µsec
Isolation Voltage		V_{ISO}	2500	V
Operating Case Temperature Range		T_C	– 40 to +95	°C
Storage Temperature Range		T_{stg}	– 40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes (#8 or M4 screws)		—	12	in–lb

(1) 1.0 ms = 1.0% duty cycle

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 125°C	I_{CES}	—	6.0 2000	100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	600	—	—	V
Collector-Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V) T_J = 125°C	$V_{CE(SAT)}$	— —	2.35 2.31	3.5 —	V
Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V) T_J = 125°C	V_F	— —	1.23 1.12	2.0 —	V
Input Capacitance (V_{CE} = 10 V, V_{GE} = 0 V, f = 1.0 Mhz) 10A60 20A60	C_{ies}	 — —	 2300 4400	 — —	pF
Input Gate Charge (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V) 10A60 20A60	Q_T	 — —	 75 135	 — —	nC

INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 25°C)

Recommended Gate Resistor Turn–On 10A60 20A60 Turn–Off	 $R_{G(on)}$ $R_{G(off)}$	 — — —	 180 47 20	 — — —	Ω
Turn-On Delay Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified) 10A60 20A60	$t_{d(on)}$	 — —	 375 215	 — —	ns
Rise Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified) 10A60 20A60	t_r	 — —	 160 125	 — —	ns
Turn–Off Delay Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	$t_{d(off)}$	—	219	—	ns
Fall Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	t_f	—	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified) 10A60 20A60	$E_{(on)}$	 — —	 0.85 1.6	 1.0 2.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified) 10A60 20A60	$E_{(off)}$	 — —	 0.13 0.3	 1.0 2.0	mJ
Diode Reverse Recovery Time (I_F = I_{Fmax}, V = 300 V, R_G as specified)	t_{rr}	—	150	—	ns
Peak Reverse Recovery Current (I_F = I_{Fmax}, V = 300 V, R_G as specified) 10A60 20A60	I_{rrm}	 — —	 6.8 12	 — —	A
Diode Stored Charge (I_F = I_{Fmax}, V = 300 V, R_G as specified) 10A60 20A60	Q_{rr}	 — —	 560 1060	 — —	nC

INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 125°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Turn–On Delay Time (V_{CE} = 300 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)	10A60 20A60	$t_{d(on)}$	— —	335 200	— —	ns
Rise Time (V_{CE} = 300 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)	10A60 20A60	t_r	— —	160 125	— —	ns
Turn–Off Delay Time (V_{CE} = 300 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)		$t_{d(off)}$	—	230	—	ns
Fall Time (V_{CE} = 300 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)		t_f	—	460	—	ns
Turn–On Energy (V_{CE} = 300 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)	10A60 20A60	$E_{(on)}$	— —	1.2 2.2	— —	mJ
Turn–Off Energy (V_{CE} = 300 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)	10A60 20A60	$E_{(off)}$	— —	0.44 0.82	— —	mJ
Diode Reverse Recovery Time ($I_F = I_{Fmax}$, V = 300 V, R_G as specified)		t_{rr}	—	240	—	ns
Peak Reverse Recovery Current ($I_F = I_{Fmax}$, V = 300 V, R_G as specified)	10A60 20A60	I_{rrm}	— —	10 18	— —	A
Diode Stored Charge ($I_F = I_{Fmax}$, V = 300 V, R_G as specified)	10A60 20A60	Q_{rr}	— —	1330 2400	— —	nC

THERMAL CHARACTERISTICS (Each Die)

Thermal Resistance — IGBT	10A60 20A60	$R_{\theta JC}$	— —	1.94 1.28	2.43 1.60	°C/W
Thermal Resistance — Free–Wheeling Diode	10A60 20A60	$R_{\theta JC}$	— —	5.28 2.61	6.60 3.26	°C/W

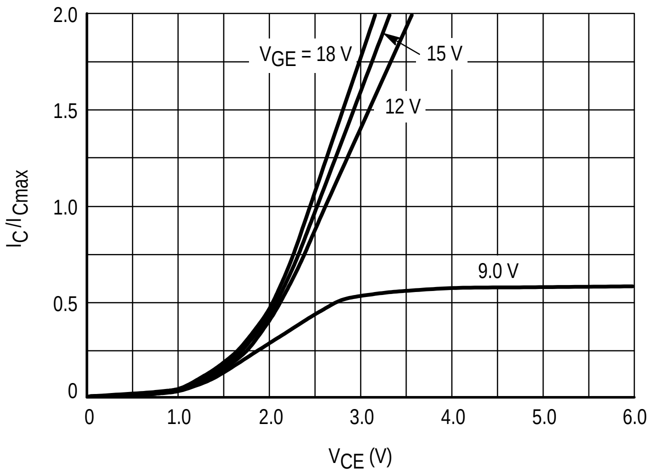


Figure 1. Normalized I_C versus V_{CE}, T_J = 25°C

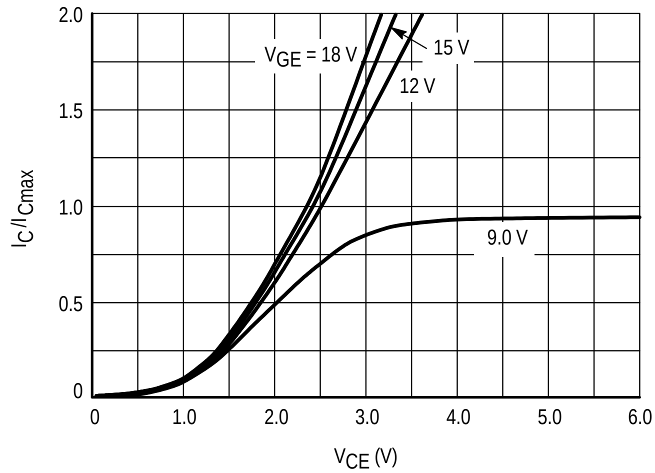


Figure 2. Normalized I_C versus V_{CE}, T_J = 125°C

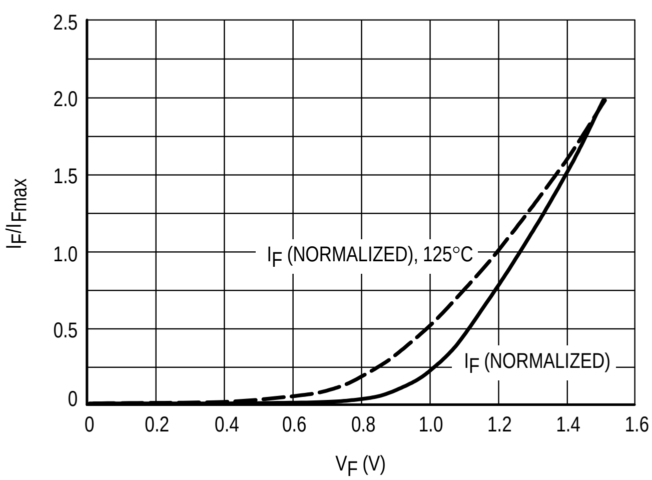


Figure 3. I_F versus V_F

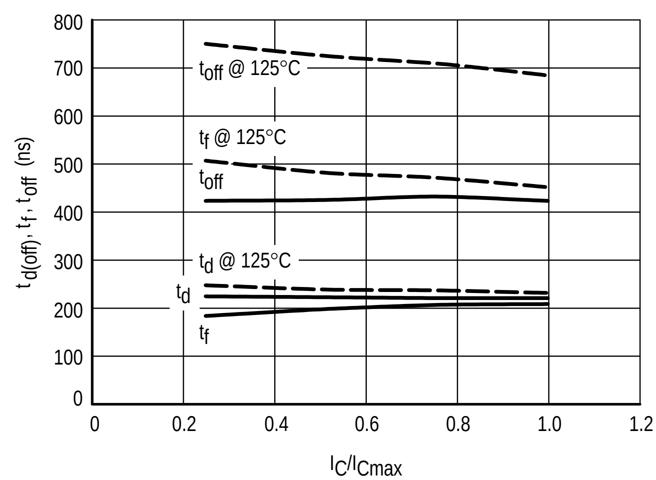


Figure 4. $t_{d(off)}$, t_f, t_{off} versus Normalized I_C

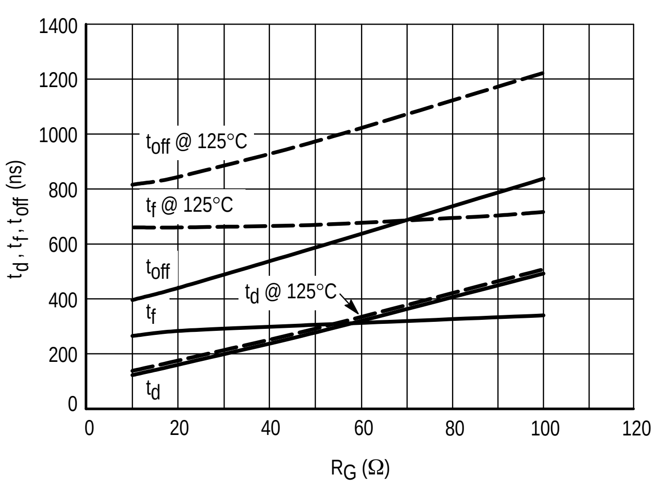


Figure 5. $t_{d(off)}$, t_f, t_{off}, versus R_G

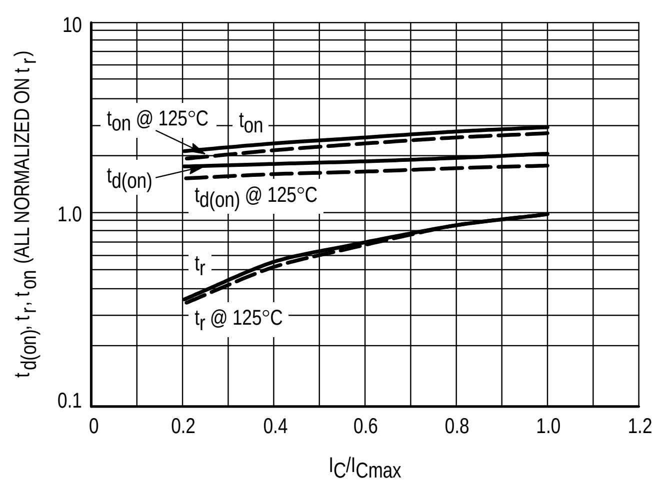


Figure 6. $t_{d(on)}$, t_r, t_{on} versus I_C

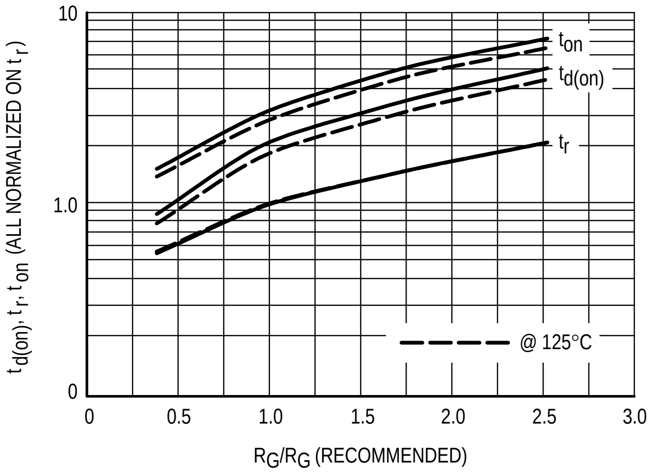


Figure 7. $t_{d(on)}$, t_r, t_{on} versus Normalized R_G

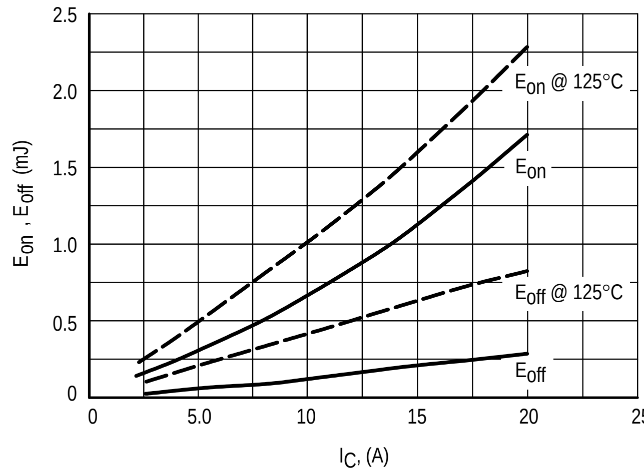


Figure 8. E_{on}, E_{off} versus I_C

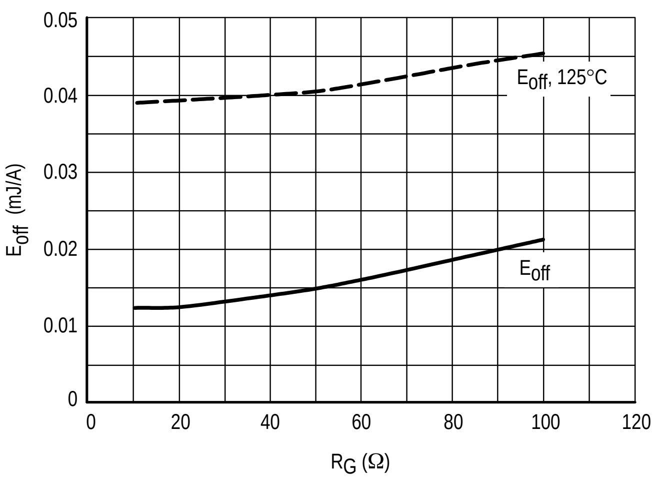


Figure 9. E_{off} versus $R_{G(off)}$ at Rated I_C

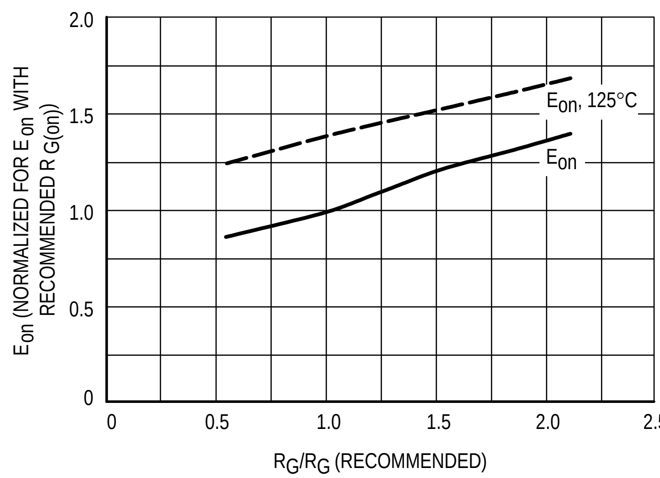


Figure 10. Normalized E_{on} versus Normalized $R_{G(on)}$

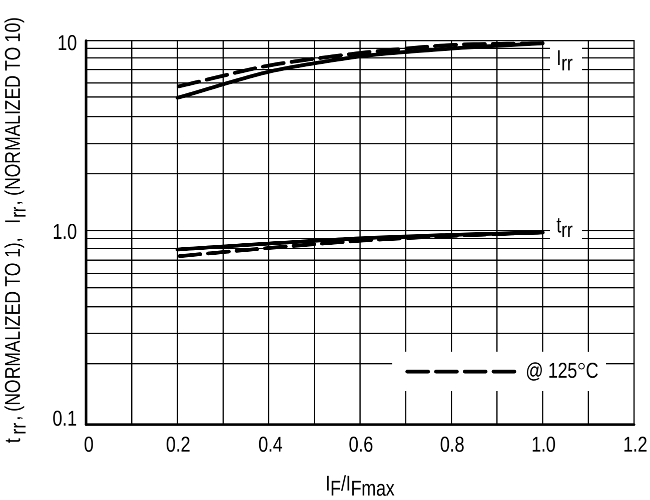


Figure 11. t_{rr}, I_{rr} versus I_F

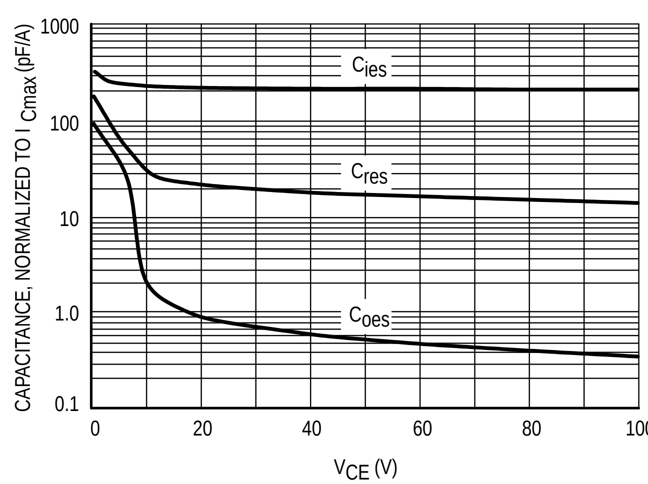


Figure 12. Capacitance Variation

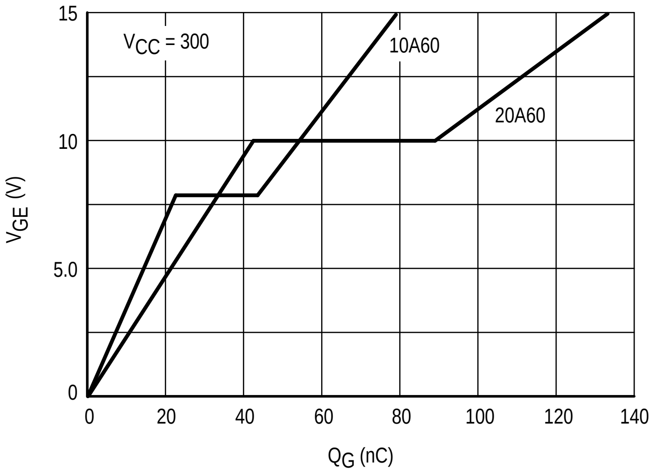


Figure 13. V_{GE} versus Q_G

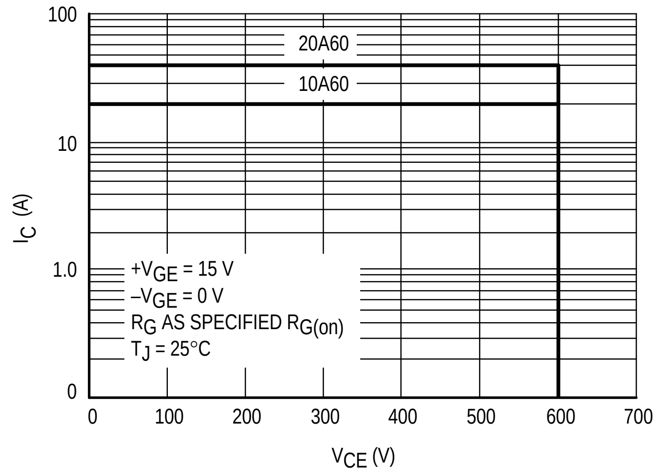


Figure 14. Reverse Biased Safe operating Area

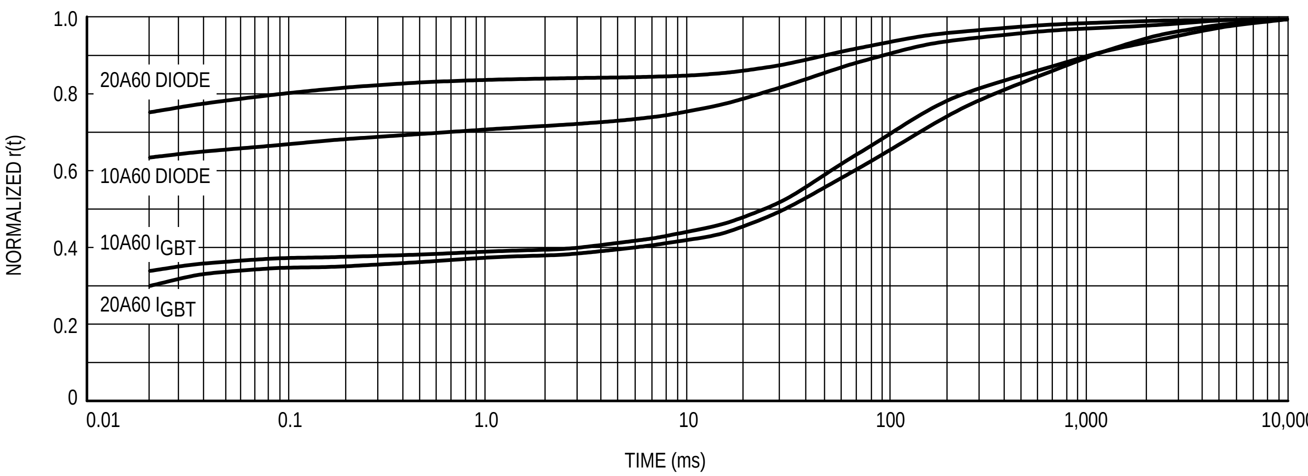


Figure 15. Normalized Transient Thermal Resistance

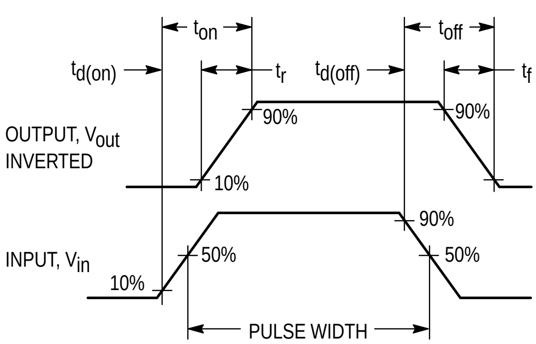


Figure 16. Switching Waveforms

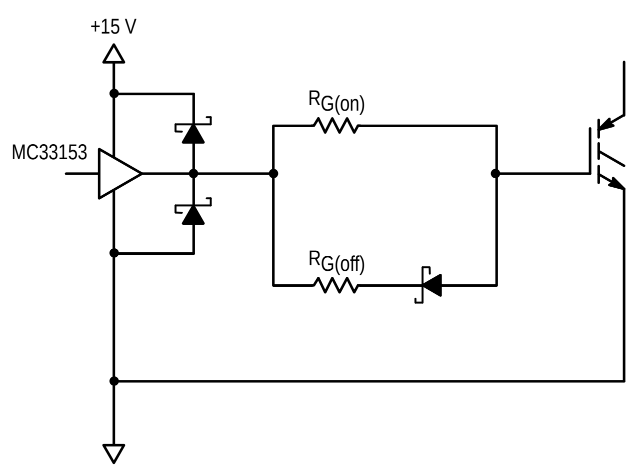


Figure 17. Typical Gate Drive Circuit

APPLICATION INFORMATION

These modules are designed to be used as the power stage of a three–phase AC induction motor drive. They may be used for up to 230 VAC applications. Switching frequencies up to 10 kHz have been considered in the design.

Gate resistance recommendations have been listed. Separate turn–on and turn–off resistors are listed, to be used in a circuit resembling Figure 17. All switching characteristics are given based on following these recommendations, but appropriate graphs are shown for operation with different gate resistance. In order to equalize across the two different module ratings, a normalization process was used. Actual typical values are listed in the second section of this specification sheet, "Electrical Specifications," but many of the graphs are given in normalized units.

The first three graphs, the DC characteristics, are normalized for current. The devices are designed to operate the same at rated maximum current (10 and 20 A). The curves extend to I_{Cpk}, the maximum allowable instantaneous current.

The next graph, turn–off times versus current, is again normalized to the rated maximum current. The following graph, turn–off times versus $R_{G(off)}$, is intentionally not normalized, as both modules behave similarly during turn–off.

Turn–on times have been normalized. Again, the graph showing variation due to current has been normalized for rated maximum current. The graph showing variation due to gate resistance normalizes against the recommended $R_{G(on)}$ for each module. In addition, the times are normalized to t_r at the appropriate temperature. For example, $t_{d(on)}$ for a 10 A module operating at 125°C at 4.0 A can be found by multiplying the typical t_r for a 10 A module at 125°C (160 ns) by the value shown on the graph at a normalized current of 0.4 (1.6) to get 256 ns. The most salient features demonstrated by these graphs are the general trends: rise time is a larger fraction of total turn–on time at 125°C, and in general, larger gate resistance results in slower switching.

Graphs of switching energies follow a similar structure. The first of these graphs, showing variation due to current, is not normalized, as any of these devices operating within its limits follows the same trend. E_{off} does not need to be normalized to show variation with $R_{G(off)}$, as both are specified with the same nominal resistance. E_{on}, however, has been appropriately normalized. Gate resistance has been normalized to the specified $R_{G(on)}$. In order to show the effect of elevated temperature, all energies were normalized to E_{on} at 25°C using the recommended $R_{G(on)}$.

Reverse recovery characteristics are also normalized. I_F is normalized to rated maximum current. I_{rrm} is normalized so that at maximum current at either 25°C or 125°C, the graph indicates "10", while t_{rr} is normalized to be "1" at maximum current at either temperature.

Capacitance values are normalized for I_{Cmax}. Due to poor scaling, gate charge and thermal characteristics are shown separately for each module.

Many issues must be considered when doing PCB layout. Figure 19 shows the footprint of a module, allowing for reasonable tolerances. A polarizing post is provided near pin 1 to ensure that the module is properly inserted during final assembly. When laying out traces, two issues are of primary importance: current carrying capacity and voltage clearance. Many techniques may be used to maximize both, including using traces on both sides of the PCB to double total copper thickness, providing cut–outs in high–current traces near high–voltage pins, and even removing portions of the board to increase "over–the–surface" creapage distance. Some additional advantage may be gained by potting the entire board assembly in a good dielectric. Consult appropriate regulatory standards, such as UL 840, for more details on high–voltage creapage and clearance.

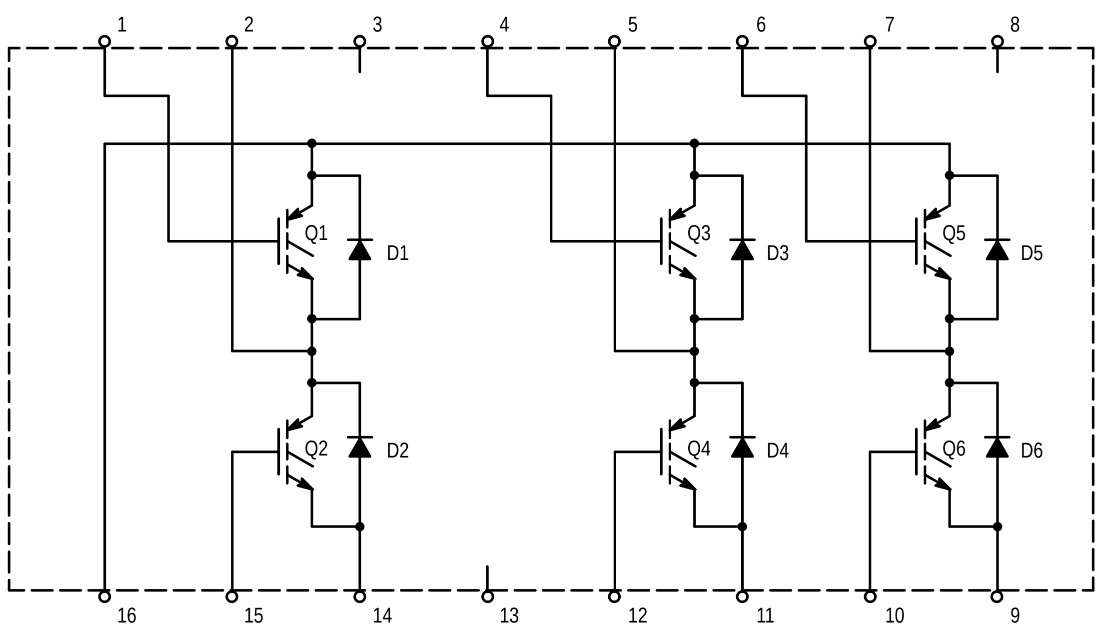


Figure 18. Schematic of Internal Circuit, Showing Package Pin–Out

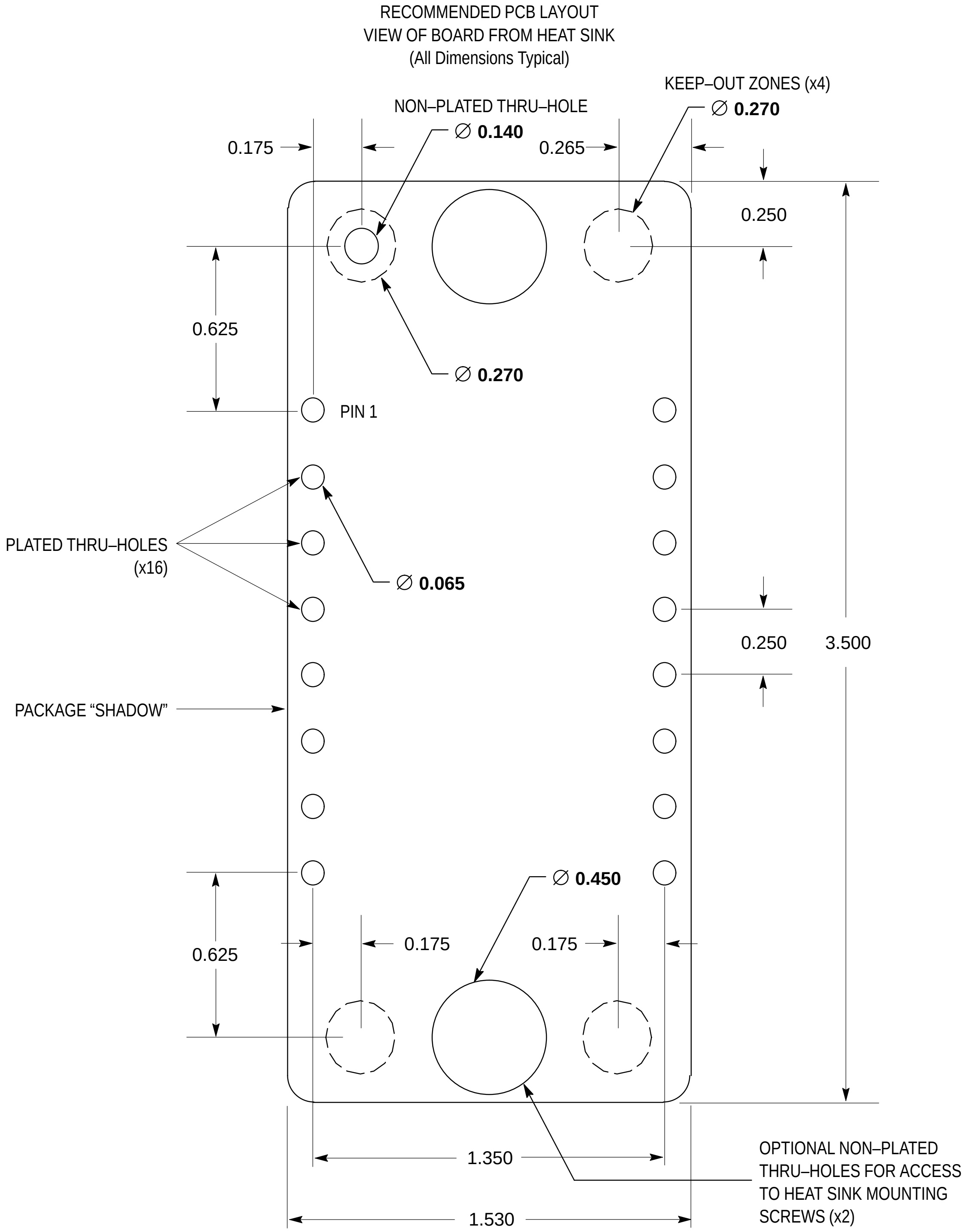
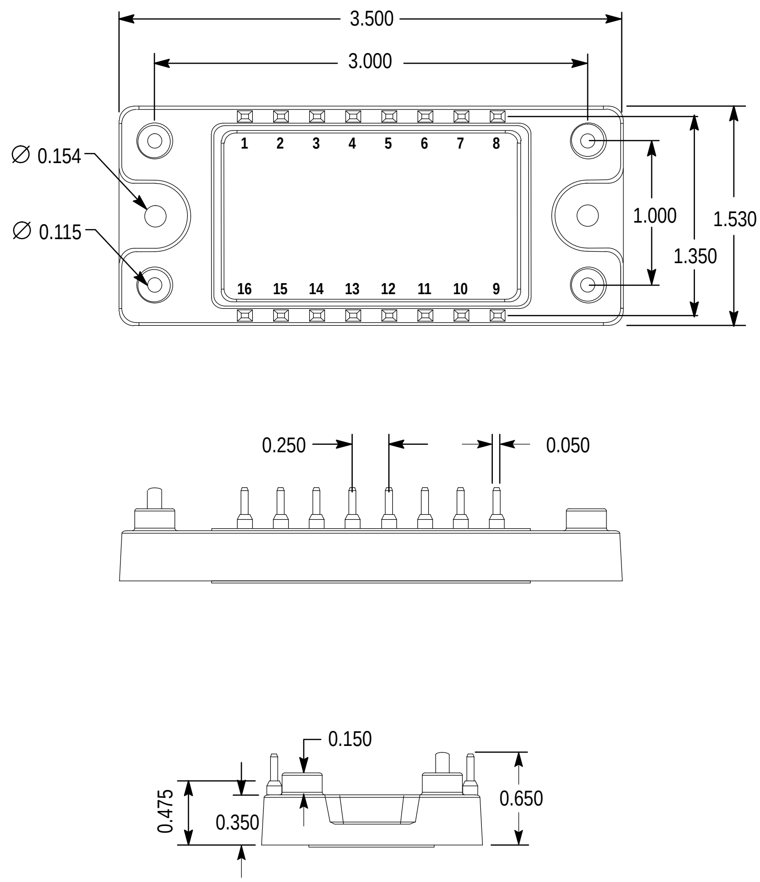


Figure 19. Package Footprint

NOTES:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates finished hole size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

PACKAGE DIMENSIONS



PRELIMINARY

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